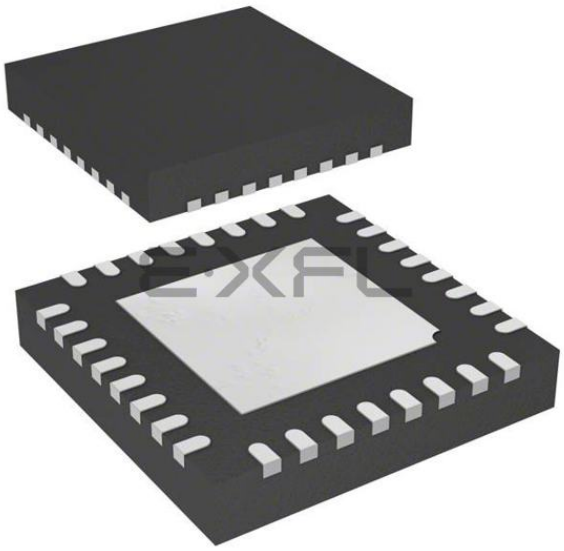

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## What is "Embedded - Microcontrollers"?

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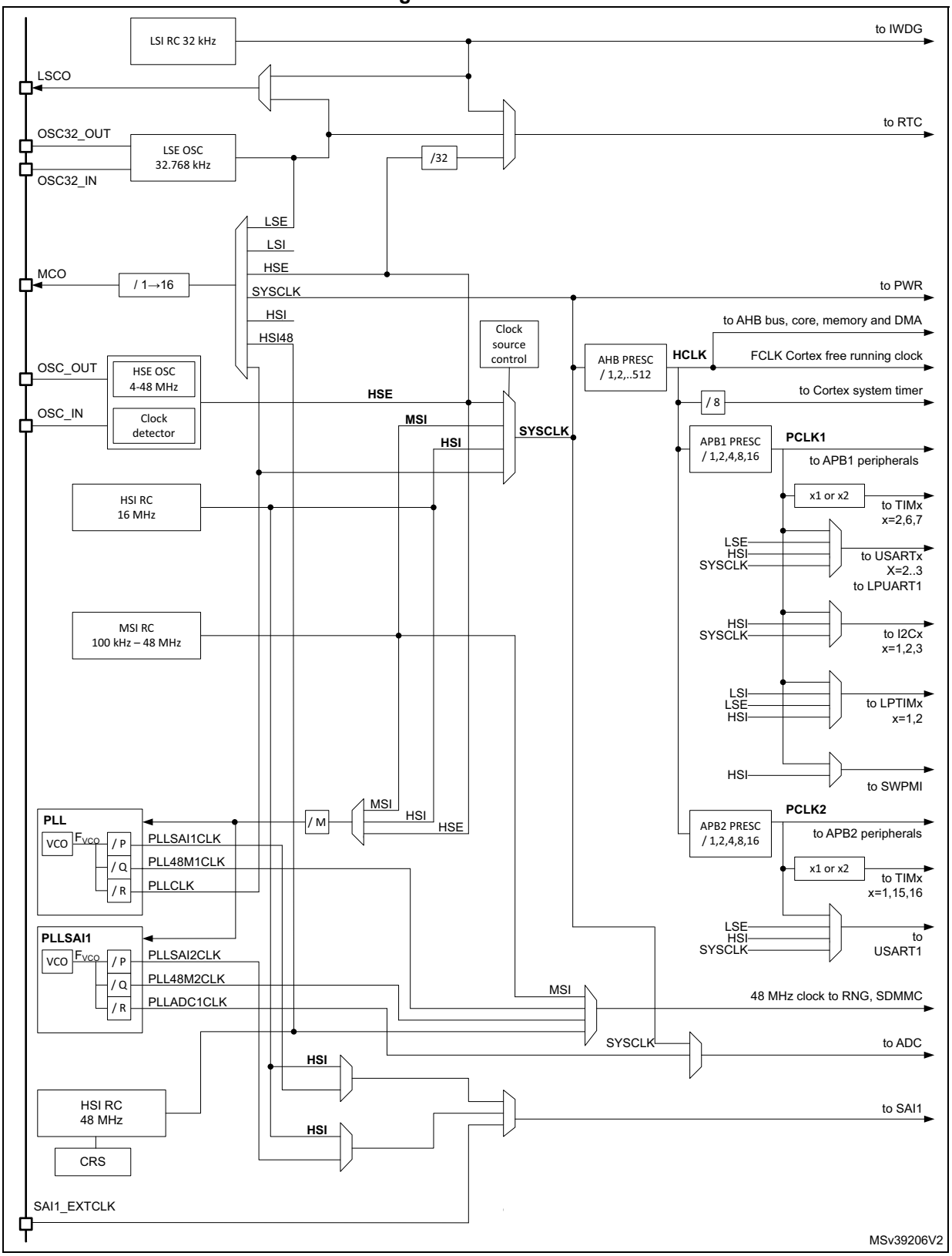
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, QSPI, SAI, SPI, SWPMI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 10x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-UFQFPN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l431kbu6 |

# Contents

**Figure 3. Clock tree**



- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

## 3.17 Voltage reference buffer (VREFBUF)

The STM32L431xx devices embed an voltage reference buffer which can be used as voltage reference for ADCs, DACs and also as voltage reference for external components through the VREF+ pin.

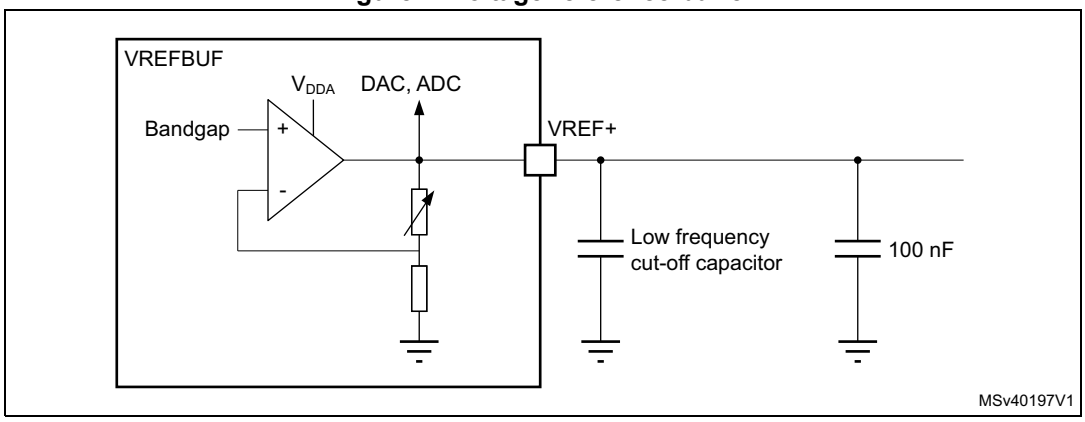
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

**Figure 4. Voltage reference buffer**




## 3.18 Comparators (COMP)

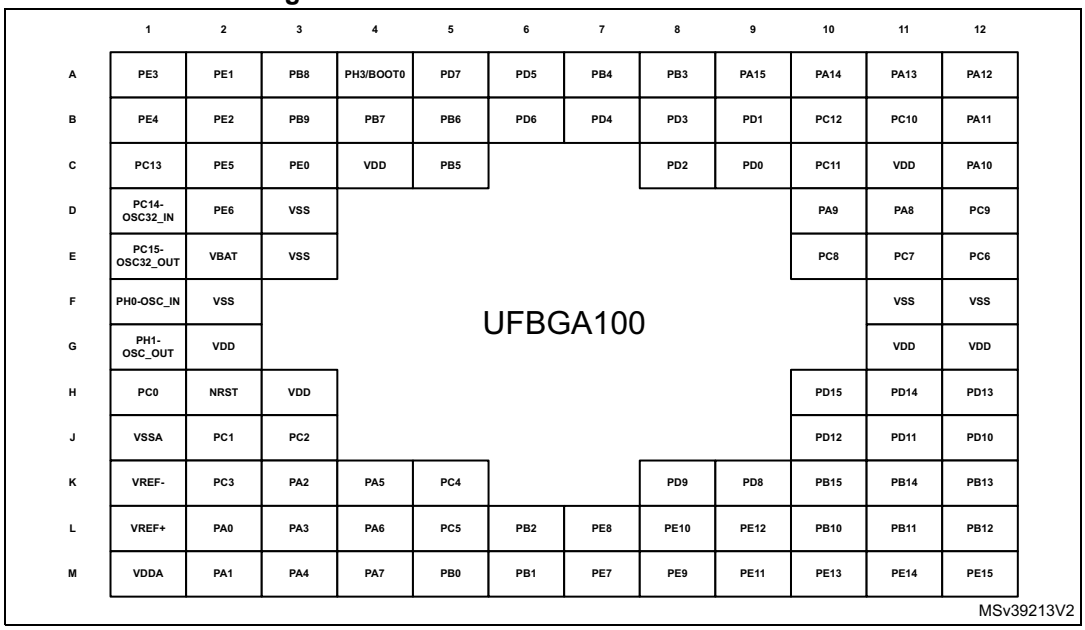
The STM32L431xx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

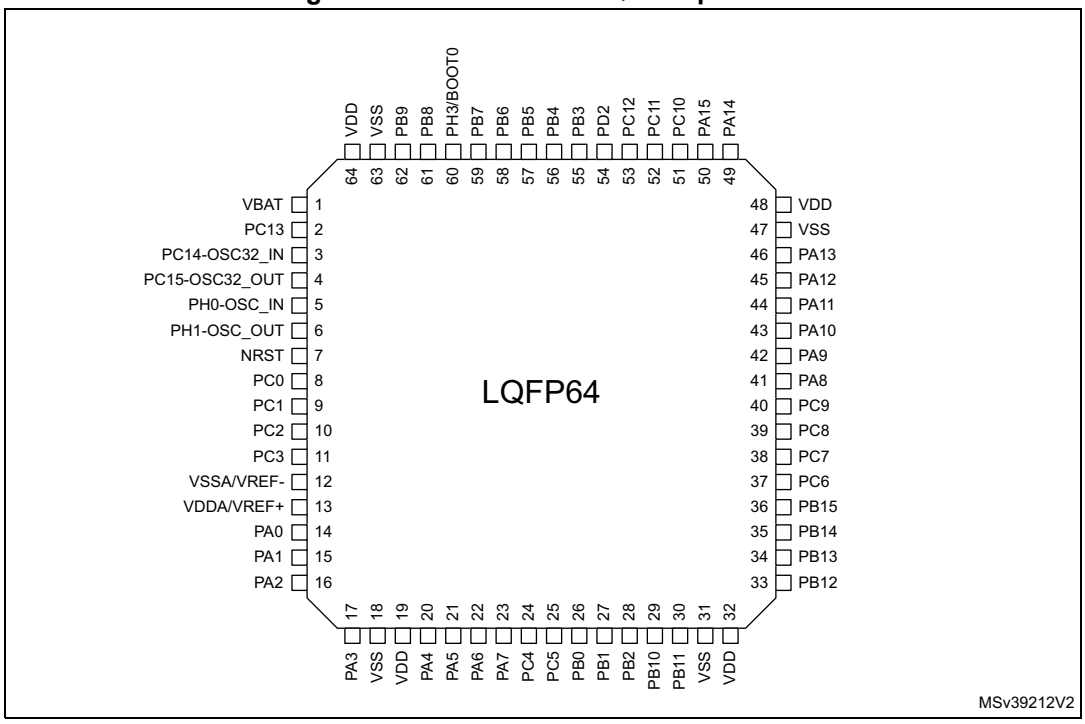
All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

**Figure 6. STM32L431Vx UFBGA100 ballout(1)**



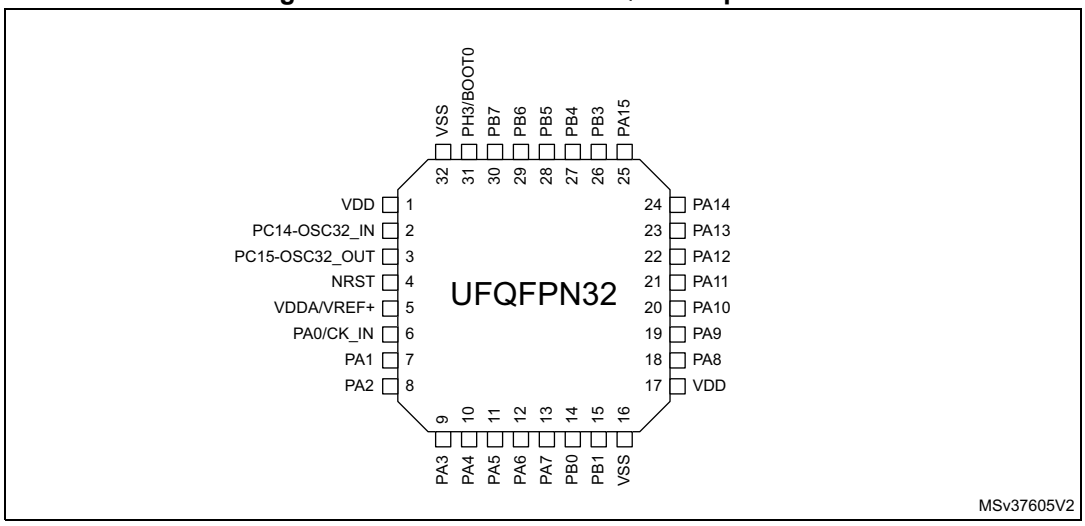

1. The above figure shows the package top view.

**Figure 7. STM32L431Rx LQFP64 pinout(1)**




1. The above figure shows the package top view.

**Figure 13. STM32L431Kx UFQFPN32 pinout(1)**




1. The above figure shows the package top view.

**Table 13. Legend/abbreviations used in the pinout table**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | | S | Supply pin |
| | | I | Input only pin |
| | | I/O | Input / output pin |
| I/O structure | | FT | 5 V tolerant I/O |
| | | TT | 3.6 V tolerant I/O |
| | | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| | | **Option for TT or FT I/Os** | |
| | | _f (1) | I/O, Fm+ capable |
| | | _a (2) | I/O, with Analog switch function supplied by $V_{DDA}$ |
| Notes | | Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset. | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

1. The related I/O structures in *Table 14* are: FT_f, FT_fa.
2. The related I/O structures in *Table 14* are: FT_a, FT_fa, TT_a.

Table 14. STM32L431xx pin definitions (continued)

| Pin Number | | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN32 | LQFP48 | UFQFPN48 | WLCSP49 | WLCSP64 | LQFP64 | UFBGA64 | LQFP100 | UFBGA100 | | | | | Alternate functions | Additional functions |
| 25 | 38 | 38 | B3 | A2 | 50 | A6 | 77 | A9 | PA15 (JTDI) | I/O | FT | (3) | JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS_DE, TSC_G3_IO1, SWPMI1_SUSPEND, EVENTOUT | - |
| - | - | - | - | C3 | 51 | B7 | 78 | B11 | PC10 | I/O | FT | - | SPI3_SCK, USART3_TX, TSC_G3_IO2, SDMMC1_D2, EVENTOUT | - |
| - | - | - | - | B3 | 52 | B6 | 79 | C10 | PC11 | I/O | FT | - | SPI3_MISO, USART3_RX, TSC_G3_IO3, SDMMC1_D3, EVENTOUT | - |
| - | - | - | - | A3 | 53 | C5 | 80 | B10 | PC12 | I/O | FT | - | SPI3_MOSI, USART3_CK, TSC_G3_IO4, SDMMC1_CK, EVENTOUT | - |
| - | - | - | - | - | - | - | 81 | C9 | PD0 | I/O | FT | - | SPI2_NSS, CAN1_RX, EVENTOUT | - |
| - | - | - | - | - | - | - | 82 | B9 | PD1 | I/O | FT | - | SPI2_SCK, CAN1_TX, EVENTOUT | - |
| - | - | - | - | A4 | 54 | B5 | 83 | C8 | PD2 | I/O | FT | - | USART3_RTS_DE, TSC_SYNC, SDMMC1_CMD, EVENTOUT | - |
| - | - | - | - | - | - | - | 84 | B8 | PD3 | I/O | FT | - | SPI2_MISO, USART2_CTS, QUADSPI_BK2_NCS, EVENTOUT | - |
| - | - | - | - | - | - | - | 85 | B7 | PD4 | I/O | FT | - | SPI2_MOSI, USART2_RTS_DE, QUADSPI_BK2_IO0, EVENTOUT | - |
| - | - | - | - | - | - | - | 86 | A6 | PD5 | I/O | FT | - | USART2_TX, QUADSPI_BK2_IO1, EVENTOUT | - |
| - | - | - | - | - | - | - | 87 | B6 | PD6 | I/O | FT | - | USART2_RX, QUADSPI_BK2_IO2, SAI1_SD_A, EVENTOUT | - |

Table 15. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 16*) (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM1/TIM2/ LPTIM1 | TIM1/TIM2 | USART2 | I2C1/I2C2/I2C3 | SPI1/SPI2 | SPI3 | USART1/ USART2/ USART3 |
| Port C | PC0 | - | LPTIM1_IN1 | - | - | I2C3_SCL | - | - | - |
| | PC1 | - | LPTIM1_OUT | - | - | I2C3_SDA | - | - | - |
| | PC2 | - | LPTIM1_IN2 | - | - | - | SPI2_MISO | - | - |
| | PC3 | - | LPTIM1_ETR | - | - | - | SPI2_MOSI | - | - |
| | PC4 | - | - | - | - | - | - | - | USART3_TX |
| | PC5 | - | - | - | - | - | - | - | USART3_RX |
| | PC6 | - | - | - | - | - | - | - | - |
| | PC7 | - | - | - | - | - | - | - | - |
| | PC8 | - | - | - | - | - | - | - | - |
| | PC9 | - | - | - | - | - | - | - | - |
| | PC10 | - | - | - | - | - | - | SPI3_SCK | USART3_TX |
| Port C | PC11 | - | - | - | - | - | - | SPI3_MISO | USART3_RX |
| | PC12 | - | - | - | - | - | - | SPI3_MOSI | USART3_CK |
| | PC13 | - | - | - | - | - | - | - | - |
| | PC14 | - | - | - | - | - | - | - | - |
| | PC15 | - | - | - | - | - | - | - | - |

Table 16. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 15*) (continued)

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | LPUART1 | CAN1/TSC | QUADSPI | | SDMMC1/ COMP1/ COMP2/ SWPMI1 | SAI1 | TIM2/TIM15/ TIM16/LPTIM2 | EVENTOUT |
| Port D | PD3 | - | - | QUADSPI_BK2_NCS | - | - | - | - | EVENTOUT |
| | PD4 | - | - | QUADSPI_BK2_IO0 | - | - | - | - | EVENTOUT |
| | PD5 | - | - | QUADSPI_BK2_IO1 | - | - | - | - | EVENTOUT |
| | PD6 | - | - | QUADSPI_BK2_IO2 | - | - | SAI1_SD_A | - | EVENTOUT |
| | PD7 | - | - | QUADSPI_BK2_IO3 | - | - | - | - | EVENTOUT |
| | PD8 | - | - | - | | - | - | - | EVENTOUT |
| | PD9 | - | - | - | | - | - | - | EVENTOUT |
| | PD10 | - | TSC_G6_IO1 | - | | - | - | - | EVENTOUT |
| | PD11 | - | TSC_G6_IO2 | - | | - | - | LPTIM2_ETR | EVENTOUT |
| | PD12 | - | TSC_G6_IO3 | - | | - | - | LPTIM2_IN1 | EVENTOUT |
| | PD13 | - | TSC_G6_IO4 | - | | - | - | LPTIM2_OUT | EVENTOUT |
| | PD14 | - | - | - | | - | - | - | EVENTOUT |
| | PD15 | - | - | - | | - | - | - | EVENTOUT |
| Port E | PE0 | - | - | - | | - | - | TIM16_CH1 | EVENTOUT |
| | PE1 | - | - | - | | - | - | - | EVENTOUT |
| | PE2 | - | TSC_G7_IO1 | - | | - | SAI1_MCLK_A | - | EVENTOUT |
| | PE3 | - | TSC_G7_IO2 | - | | - | SAI1_SD_B | - | EVENTOUT |
| | PE4 | - | TSC_G7_IO3 | - | - | - | SAI1_FS_A | - | EVENTOUT |

**Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable**

| Symbol | Parameter | Conditions | | | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | Voltage scaling | $f_{HCLK}$ | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | |
| $I_{DD}$(Run) | Supply current in Run mode | $f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable | Range 2 | 26 MHz | 2.66 | 2.68 | 2.73 | 2.81 | 2.96 | 3.0 | 3.1 | 3.2 | 3.3 | 3.6 | mA |
| | | | | 16 MHz | 1.88 | 1.9 | 1.94 | 2.02 | 2.17 | 2.1 | 2.2 | 2.3 | 2.4 | 2.7 | |
| | | | | 8 MHz | 1.05 | 1.06 | 1.11 | 1.18 | 1.33 | 1.2 | 1.2 | 1.3 | 1.4 | 1.7 | |
| | | | | 4 MHz | 0.6 | 0.62 | 0.66 | 0.73 | 0.87 | 0.7 | 0.7 | 0.8 | 0.9 | 1.2 | |
| | | | | 2 MHz | 0.36 | 0.37 | 0.34 | 0.48 | 0.62 | 0.4 | 0.4 | 0.5 | 0.6 | 0.9 | |
| | | | | 1 MHz | 0.23 | 0.25 | 0.25 | 0.36 | 0.5 | 0.3 | 0.3 | 0.4 | 0.5 | 0.8 | |
| | | | | 100 kHz | 0.12 | 0.14 | 0.17 | 0.25 | 0.39 | 0.1 | 0.2 | 0.2 | 0.4 | 0.7 | |
| | | | Range 1 | 80 MHz | 8.56 | 8.61 | 8.69 | 8.79 | 8.97 | 9.6 | 9.7 | 9.8 | 10.0 | 10.3 | |
| | | | | 72 MHz | 7.74 | 7.79 | 7.86 | 7.96 | 8.14 | 8.7 | 8.7 | 8.8 | 9.0 | 9.4 | |
| | | | | 64 MHz | 7.63 | 7.68 | 7.75 | 7.85 | 8.04 | 8.6 | 8.6 | 8.7 | 8.9 | 9.3 | |
| | | | | 48 MHz | 6.36 | 6.4 | 6.48 | 6.58 | 6.76 | 7.2 | 7.3 | 7.4 | 7.6 | 7.9 | |
| | | | | 32 MHz | 4.56 | 4.6 | 4.66 | 4.76 | 4.93 | 5.2 | 5.2 | 5.3 | 5.5 | 5.8 | |
| | | | | 24 MHz | 3.45 | 3.48 | 3.54 | 3.64 | 3.8 | 3.9 | 4.0 | 4.1 | 4.2 | 4.6 | |
| | | | | 16 MHz | 2.48 | 2.51 | 2.56 | 2.65 | 2.82 | 2.8 | 2.9 | 3.0 | 3.1 | 3.5 | |
| $I_{DD}$(LPRun) | Supply current in Low-power run | $f_{HCLK} = f_{MSI}$ all peripherals disable | | 2 MHz | 310 | 317 | 364 | 440 | 593 | 375.3 | 400.9 | 456.7 | 595.3 | 909.6 | µA |
| | | | | 1 MHz | 157 | 173 | 226 | 296 | 448 | 204.8 | 234.2 | 298.2 | 445.8 | 758.9 | |
| | | | | 400 kHz | 72.6 | 89 | 130 | 206 | 356 | 99.7 | 131.2 | 199.7 | 349.3 | 663.7 | |
| | | | | 100 kHz | 32.3 | 46 | 89.7 | 164 | 314 | 52.4 | 82.1 | 153.3 | 301.2 | 616.9 | |

1. Guaranteed by characterization results, unless otherwise specified.

**Table 34. Current consumption in Stop 1 mode**

| Symbol | Parameter | Conditions | | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | - | $V_{DD}$ | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | |
| $I_{DD}$ (Stop 1) | Supply current in Stop 1 mode, RTC disabled | - | 1.8 V | 4.34 | 12.4 | 43.6 | 96.4 | 204 | 9.3 | 27.4 | 98.9 | 198.7 | 397.5 | µA |
| | | | 2.4 V | 4.35 | 12.5 | 43.8 | 97 | 205 | 9.4 | 27.6 | 99.5 | 199.0 | 398.0 | |
| | | | 3 V | 4.41 | 12.6 | 44.1 | 97.7 | 207 | 9.5 | 27.8 | 100.3 | 200.4 | 400.8 | |
| | | | 3.6 V | 4.56 | 12.9 | 44.8 | 98.9 | 210 | 9.7 | 28.3 | 101.7 | 202.1 | 404.2 | |
| $I_{DD}$ (Stop 1 with RTC) | Supply current in stop 1 mode, RTC enabled | RTC clocked by LSI | 1.8 V | 4.63 | 12.7 | 43.9 | 96.8 | 205 | 9.9 | 28.0 | 99.5 | 198.9 | 397.8 | µA |
| | | | 2.4 V | 4.78 | 12.8 | 44.2 | 97.4 | 206 | 10.1 | 28.3 | 100.3 | 199.5 | 399.0 | |
| | | | 3 V | 4.93 | 13 | 44.6 | 98.1 | 207 | 10.4 | 28.7 | 101.2 | 200.9 | 401.9 | |
| | | | 3.6 V | 5.05 | 13.4 | 45.3 | 99.5 | 210 | 10.8 | 29.4 | 102.8 | 202.5 | 405.0 | |
| | | RTC clocked by LSE bypassed, at 32768 Hz | 1.8 V | 4.7 | 12.8 | 44 | 96.9 | 205 | - | - | - | - | - | |
| | | | 2.4 V | 4.95 | 13 | 44.4 | 97.6 | 206 | - | - | - | - | - | |
| | | | 3 V | 5.33 | 13.6 | 45.4 | 99.1 | 209 | - | - | - | - | - | |
| | | | 3.6 V | 6.91 | 16.1 | 48.8 | 103 | 216 | - | - | - | - | - | |
| | | RTC clocked by LSE quartz(2) in low drive mode | 1.8 V | 4.76 | 12.3 | 43.7 | 99.1 | - | - | - | - | - | - | |
| | | | 2.4 V | 4.95 | 12.4 | 43.8 | 99.3 | - | - | - | - | - | - | |
| | | | 3 V | 5.1 | 12.6 | 44.1 | 99.6 | - | - | - | - | - | - | |
| | | | 3.6 V | 5.65 | 13 | 44.8 | 101 | - | - | - | - | - | - | |
| $I_{DD}$ (wakeup from Stop1) | Supply current during wakeup from Stop 1 | Wakeup clock MSI = 48 MHz, voltage Range 1. See (3). | 3 V | 1.14 | - | - | - | - | - | - | - | - | - | mA |
| | | Wakeup clock MSI = 4 MHz, voltage Range 2. See (3). | 3 V | 1.22 | - | - | - | - | - | - | - | - | - | |
| | | Wakeup clock HSI16 = 16 MHz, voltage Range 1. See (3). | 3 V | 1.20 | - | - | - | - | - | - | - | - | - | |

1. Guaranteed based on test during characterization, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 40: Low-power mode wakeup timings*.

**Table 35. Current consumption in Stop 0**

| Symbol | Parameter | Conditions | TYP | | | | | MAX(1) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | 25 °C | 55 °C | 85 °C | 105 °C | 125 °C | |
| $I_{DD}$ (Stop 0) | Supply current in Stop 0 mode, RTC disabled | 1.8 V | 108 | 119 | 158 | 221 | 347 | 133 | 158 | 244 | 395 | 704 | µA |
| | | 2.4 V | 110 | 121 | 160 | 223 | 349 | 136 | 161 | 248 | 399 | 710 | |
| | | 3 V | 111 | 123 | 161 | 224 | 352 | 139 | 164 | 251 | 403 | 716 | |
| | | 3.6 V | 114 | 125 | 163 | 227 | 355 | 142 | 167 | 254 | 408 | 722(2) | |

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

**Table 39. Peripheral current consumption (continued)**

| Peripheral | | Range 1 | Range 2 | Low-power run and sleep | Unit |
|---|---|---|---|---|---|
| APB2 | FW | 0.2 | 0.2 | 0.2 | µA/MHz |
| | SAI1 independent clock domain | 2.3 | 1.8 | 1.9 | |
| | SAI1 clock domain | 2.1 | 1.8 | 2.0 | |
| | SDMMC1 independent clock domain | 4.7 | 3.9 | 3.9 | |
| | SDMMC1 clock domain | 2.5 | 1.9 | 1.9 | |
| | SPI1 | 1.8 | 1.6 | 1.7 | |
| | SYSCFG/VREFBUF/COMP | 0.6 | 0.5 | 0.6 | |
| | TIM1 | 8.1 | 6.5 | 7.6 | |
| | TIM15 | 3.7 | 3.0 | 3.4 | |
| | TIM16 | 2.7 | 2.1 | 2.6 | |
| | USART1 independent clock domain | 4.8 | 4.2 | 4.6 | |
| | USART1 clock domain | 1.5 | 1.3 | 1.7 | |
| | All APB2 on | 24.2 | 19.9 | 22.6 | |
| ALL | | 94.8 | 76.5 | 94.0 | |

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The GPIOx (x= A…H) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).
3. The AHB to APB1 Bridge is automatically active when at least one peripheral is ON on the APB1.
4. The AHB to APB2 Bridge is automatically active when at least one peripheral is ON on the APB2.

### 6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 40* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

**Table 40. Low-power mode wakeup timings(1)**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{WUSLEEP}$ | Wakeup time from Sleep mode to Run mode | - | 6 | 6 | Nb of CPU cycles |
| $t_{WULPSLEEP}$ | Wakeup time from Low-power sleep mode to Low-power run mode | Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz | 6 | 8.3 | |

## 6.3.7 External clock source characteristics

### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 20: High-speed external clock source AC timing diagram*.

**Table 43. High-speed external user clock characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | User external clock source frequency | Voltage scaling Range 1 | - | 8 | 48 | MHz |
| | | Voltage scaling Range 2 | - | 8 | 26 | |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | - | 0.7 $V_{DDIOx}$ | - | $V_{DDIOx}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | - | $V_{SS}$ | - | 0.3 $V_{DDIOx}$ | |
| $t_{w(HSEH)}$ $t_{w(HSEL)}$ | OSC_IN high or low time | Voltage scaling Range 1 | 7 | - | - | ns |
| | | Voltage scaling Range 2 | 18 | - | - | |

1. Guaranteed by design.

**Figure 20. High-speed external clock source AC timing diagram**

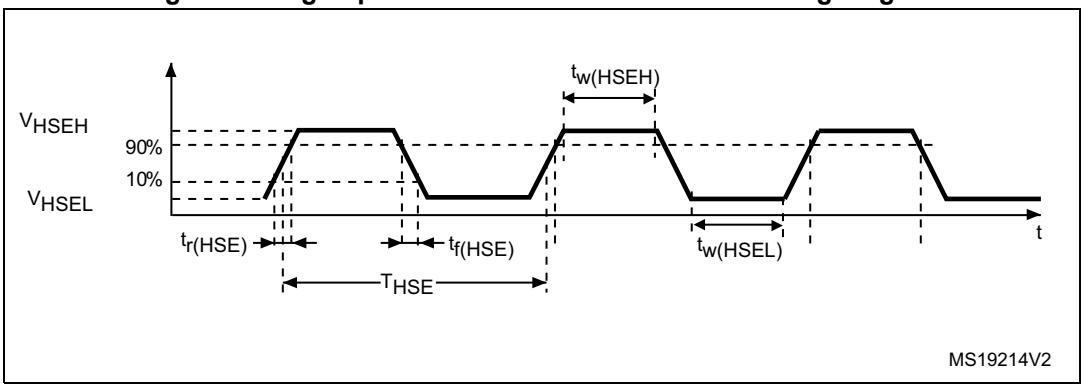


**Table 67. ADC accuracy - limited test conditions 2(1)(2)(3) (continued)**

| Symbol | Parameter | Conditions(4) | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| THD | Total harmonic distortion | ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ $V_{DDA}$ | Single ended | Fast channel (max speed) | - | -74 | -65 | dB |
| | | | | Slow channel (max speed) | - | -74 | -67 | |
| | | | Differential | Fast channel (max speed) | - | -79 | -70 | |
| | | | | Slow channel (max speed) | - | -79 | -71 | |

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA}$ < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA}$ < 2.4 V). It is disable when $V_{DDA}$ ≥ 2.4 V. No oversampling.

### 6.3.19 Voltage reference buffer characteristics

**Table 72. VREFBUF characteristics(1)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | Normal mode | $V_{RS}$ = 0 | 2.4 | - | 3.6 | V |
| | | | $V_{RS}$ = 1 | 2.8 | - | 3.6 | |
| | | Degraded mode(2) | $V_{RS}$ = 0 | 1.65 | - | 2.4 | |
| | | | $V_{RS}$ = 1 | 1.65 | - | 2.8 | |
| $V_{REFBUF\_OUT}$ | Voltage reference output | Normal mode | $V_{RS}$ = 0 | 2.046(3) | 2.048 | 2.049(3) | |
| | | | $V_{RS}$ = 1 | 2.498(3) | 2.5 | 2.502(3) | |
| | | Degraded mode(2) | $V_{RS}$ = 0 | $V_{DDA}$-150 mV | - | $V_{DDA}$ | |
| | | | $V_{RS}$ = 1 | $V_{DDA}$-150 mV | - | $V_{DDA}$ | |
| TRIM | Trim step resolution | - | - | - | ±0.05 | ±0.1 | % |
| CL | Load capacitor | - | - | 0.5 | 1 | 1.5 | µF |
| esr | Equivalent Serial Resistor of Cload | - | - | - | - | 2 | Ω |
| $I_{load}$ | Static load current | - | - | - | - | 4 | mA |
| $I_{line\_reg}$ | Line regulation | 2.8 V ≤ $V_{DDA}$ ≤ 3.6 V | $I_{load}$ = 500 µA | - | 200 | 1000 | ppm/V |
| | | | $I_{load}$ = 4 mA | - | 100 | 500 | |
| $I_{load\_reg}$ | Load regulation | 500 µA ≤ $I_{load}$ ≤4 mA | Normal mode | - | 50 | 500 | ppm/mA |
| $T_{Coeff}$ | Temperature coefficient | -40 °C < $T_J$ < +125 °C | | - | - | $T_{coeff\_vrefint}$ + 50 | ppm/ °C |
| | | 0 °C < $T_J$ < +50 °C | | - | - | $T_{coeff\_vrefint}$ + 50 | |
| PSRR | Power supply rejection | DC | | 40 | 60 | - | dB |
| | | 100 kHz | | 25 | 40 | - | |
| $t_{START}$ | Start-up time | CL = 0.5 µF(4) | | - | 300 | 350 | µs |
| | | CL = 1.1 µF(4) | | - | 500 | 650 | |
| | | CL = 1.5 µF(4) | | - | 650 | 800 | |
| $I_{INRUSH}$ | Control of maximum DC current drive on VREFBUF_OUT during start-up phase (5) | - | - | - | 8 | - | mA |

### 6.3.20 Comparator characteristics

**Table 73. COMP characteristics(1)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | 1.62 | - | 3.6 | V |
| $V_{IN}$ | Comparator input voltage range | - | | 0 | - | $V_{DDA}$ | V |
| $V_{BG}$(2) | Scaler input voltage | - | | $V_{REFINT}$ | | | V |
| $V_{SC}$ | Scaler offset voltage | - | | - | ±5 | ±10 | mV |
| $I_{DDA}$(SCALER) | Scaler static consumption from $V_{DDA}$ | BRG_EN=0 (bridge disable) | | - | 200 | 300 | nA |
| | | BRG_EN=1 (bridge enable) | | - | 0.8 | 1 | µA |
| $t_{START\_SCALER}$ | Scaler startup time | - | | - | 100 | 200 | µs |
| $t_{START}$ | Comparator startup time to reach propagation delay specification | High-speed mode | $V_{DDA} \geq 2.7$ V | - | - | 5 | µs |
| | | | $V_{DDA} < 2.7$ V | - | - | 7 | |
| | | Medium mode | $V_{DDA} \geq 2.7$ V | - | - | 15 | |
| | | | $V_{DDA} < 2.7$ V | - | - | 25 | |
| | | Ultra-low-power mode | | - | - | 40 | |
| $t_D$(3) | Propagation delay with 100 mV overdrive | High-speed mode | $V_{DDA} \geq 2.7$ V | - | 55 | 80 | ns |
| | | | $V_{DDA} < 2.7$ V | - | 65 | 100 | |
| | | Medium mode | | - | 0.55 | 0.9 | µs |
| | | Ultra-low-power mode | | - | 4 | 7 | |
| $V_{offset}$ | Comparator offset error | Full common mode range | - | - | ±5 | ±20 | mV |
| $V_{hys}$ | Comparator hysteresis | No hysteresis | | - | 0 | - | mV |
| | | Low hysteresis | | - | 8 | - | |
| | | Medium hysteresis | | - | 15 | - | |
| | | High hysteresis | | - | 27 | - | |
| $I_{DDA}$(COMP) | Comparator consumption from $V_{DDA}$ | Ultra-low-power mode | Static | - | 400 | 600 | nA |
| | | | With 50 kHz ±100 mV overdrive square signal | - | 1200 | - | |
| | | Medium mode | Static | - | 5 | 7 | µA |
| | | | With 50 kHz ±100 mV overdrive square signal | - | 6 | - | |
| | | High-speed mode | Static | - | 70 | 100 | |
| | | | With 50 kHz ±100 mV overdrive square signal | - | 75 | - | |

1. Guaranteed by design, unless otherwise specified.

**Table 82. SPI characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{v(SO)}$ | Data output valid time | Slave mode 2.7 < $V_{DD}$ < 3.6 V Voltage Range 1 | - | 12.5 | 13.5 | ns |
| | | Slave mode 1.71 < $V_{DD}$ < 3.6 V Voltage Range 1 | - | 12.5 | 24 | |
| | | Slave mode 1.71 < $V_{DD}$ < 3.6 V Voltage Range 2 | - | 12.5 | 33 | |
| $t_{v(MO)}$ | | Master mode | - | 4.5 | 6 | |
| $t_{h(SO)}$ | Data output hold time | Slave mode | 7 | - | - | ns |
| $t_{h(MO)}$ | | Master mode | 0 | - | - | |

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.

**Figure 33. SPI timing diagram - slave mode and CPHA = 0**

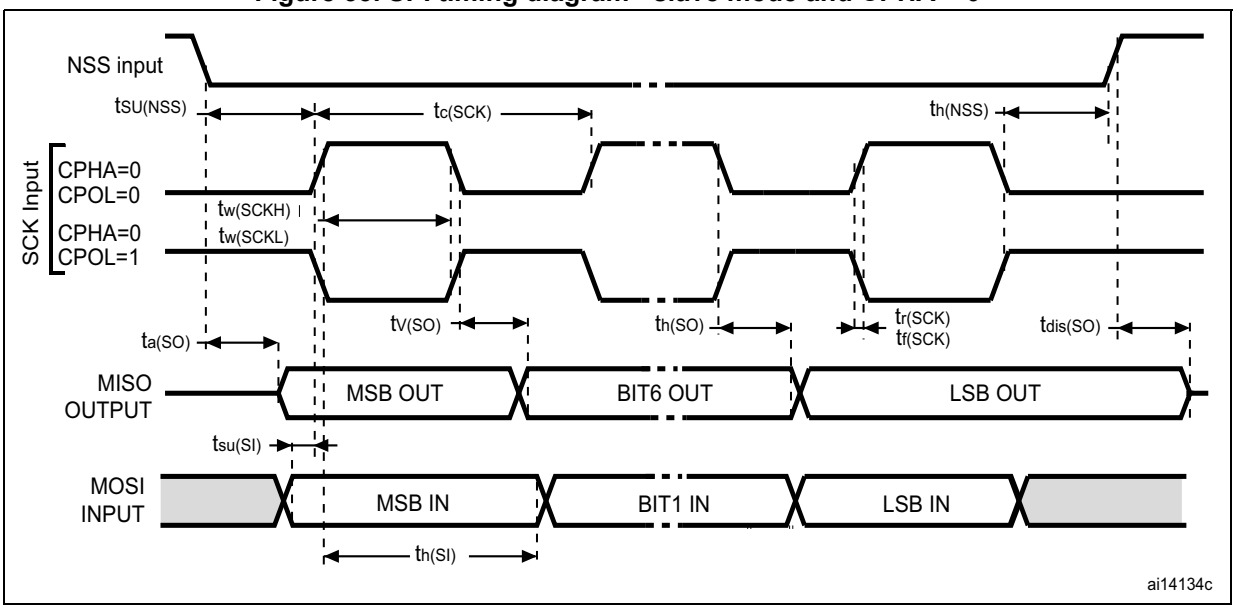
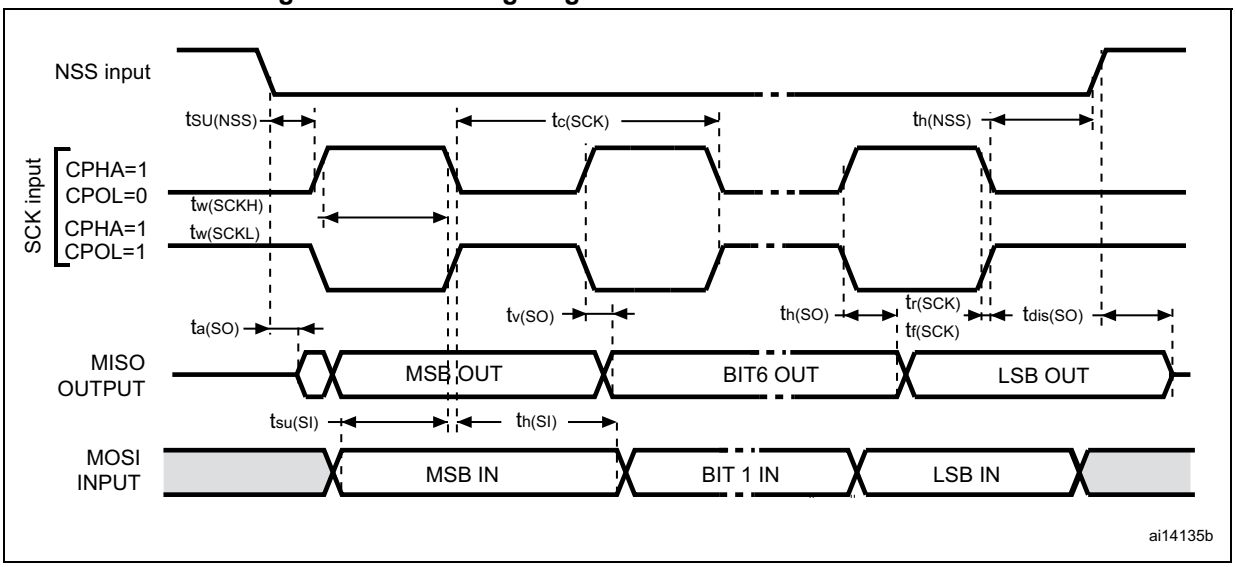
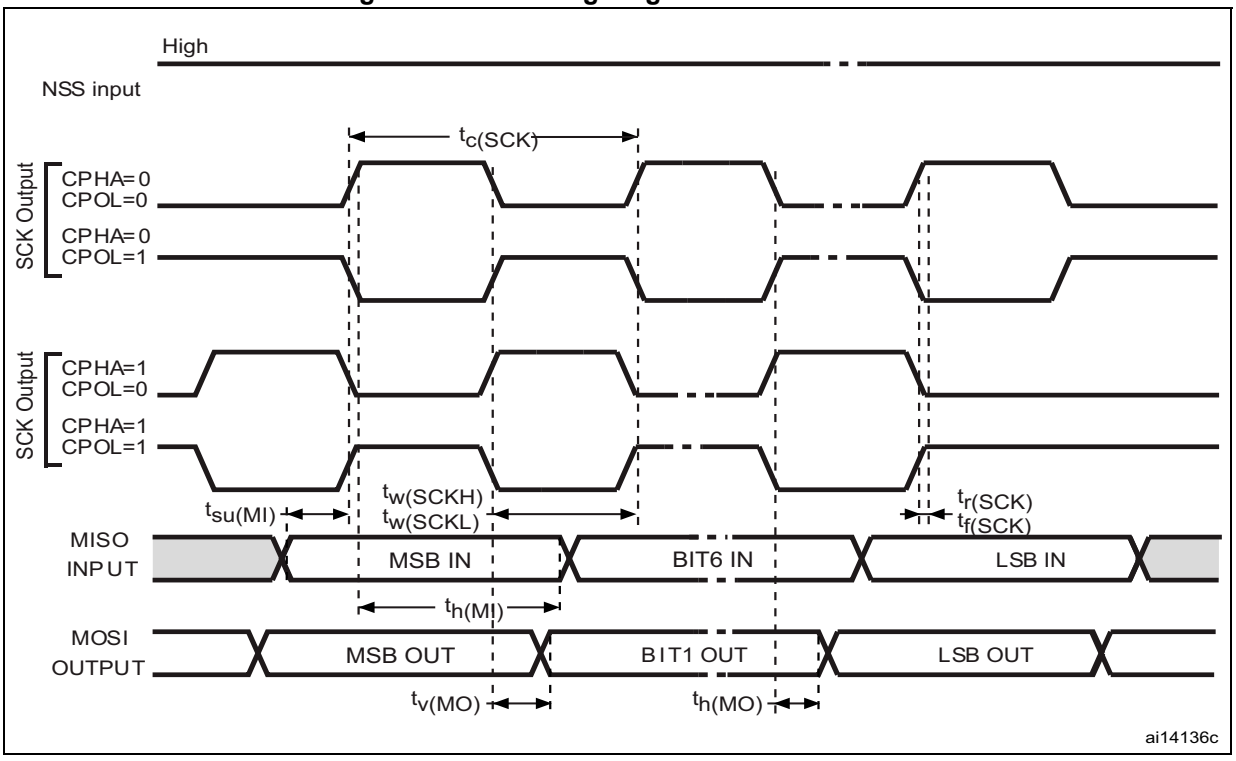


**Figure 34. SPI timing diagram - slave mode and CPHA = 1**



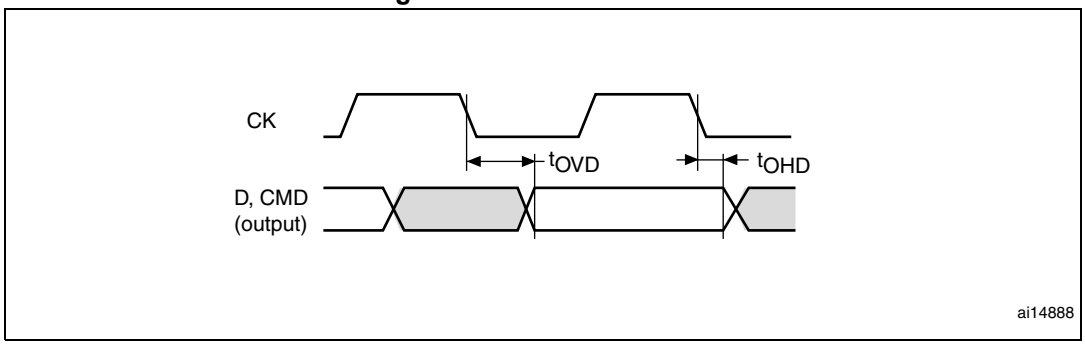

1. Measurement points are done at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**Figure 35. SPI timing diagram - master mode**




1. Measurement points are done at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**Figure 41. SD default mode**




## CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

## SWPMI characteristics

The Single Wire Protocol Master Interface (SWPMI) and the associated SWPMI_IO transceiver are compliant with the ETSI TS 102 613 technical specification.

**Table 88. SWPMI electrical characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{SWPSTART}$ | SWPMI regulator startup time | SWP Class B<br>2.7 V ≤ $V_{DD}$ ≤ 3,3V | - | - | 300 | µs |
| $t_{SWPBIT}$ | SWP bit duration | $V_{CORE}$ voltage range 1 | 500 | - | - | ns |
| | | $V_{CORE}$ voltage range 2 | 620 | - | - | |

# 8 Part numbering

**Table 103. STM32L431xx ordering information scheme**

Example: STM32 L 431 C C T 6 TR

**Device family**

STM32 = ARM® based 32-bit microcontroller

**Product type**

L = ultra-low-power

**Device subfamily**

431: STM32L431xx

**Pin count**

K = 32 pins

C = 48 pins

R = 64 pins

V = 100 pins

**Flash memory size**

B = 128 kB of Flash memory

C = 256 KB of Flash memory

**Package**

T = LQFP ECOPACK®2

U = QFN ECOPACK®2

I = UFBGA ECOPACK®2

Y = CSP ECOPACK®2

**Temperature range**

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

7 = Industrial temperature range, -40 to 105 °C (125 °C junction)

3 = Industrial temperature range, -40 to 125 °C (130 °C junction)

**Packing**

TR = tape and reel

xxx = programmed parts