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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l431rbt6tr

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Table 5. STM32L431xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y ⁽¹⁾
	ADCx DACx	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

3.34 Development support

3.34.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.34.2 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L431xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 15. Alternate function AF0 to AF7 (for AF8 to AF15 see [Table 16](#))

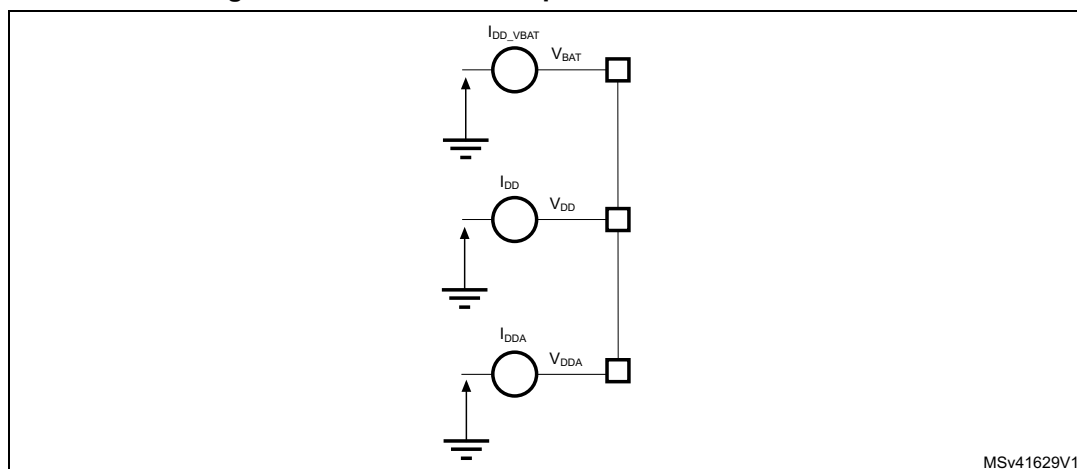
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3	USART1/ USART2/ USART3
Port A	PA0	-	TIM2_CH1	-	-	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	-	-	I2C1_SMBA	SPI1_SCK	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	-	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	-	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	-	-	-	SPI1_MISO	COMP1_OUT	USART3_CTS
	PA7	-	TIM1_CH1N	-	-	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	-	I2C1_SCL	-	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	I2C1_SDA	-	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	COMP1_OUT	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	-	USART1_RTS_ DE
	PA13	JTMS-SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK-SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_RTS_ DE

Table 17. STM32L431xx memory map and peripheral register boundary addresses ⁽¹⁾

Bus	Boundary address	Size(bytes)	Peripheral
AHB2	0x5006 0800 - 0x5006 0BFF	1 KB	RNG
	0x5004 0400 - 0x5006 07FF	158 KB	Reserved
	0x5004 0000 - 0x5004 03FF	1 KB	ADC
	0x5000 0000 - 0x5003 FFFF	16 KB	Reserved
	0x4800 2000 - 0x4FFF FFFF	~127 MB	Reserved
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH
	0x4800 1400 - 0x4800 1BFF	2 KB	Reserved
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~127 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH registers
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
APB2	0x4001 5800 - 0x4001 FFFF	42 KB	Reserved
	0x4001 5400 - 0x4000 57FF	1 KB	SAI1
	0x4001 4800 - 0x4000 53FF	3 KB	Reserved
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved

6.1.7 Current consumption measurement

Figure 18. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 18: Voltage characteristics](#), [Table 19: Current characteristics](#) and [Table 20: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 18. Voltage characteristics⁽¹⁾

Symbol	Ratings	Min	Max	Unit
$V_{DDX} - V_{SS}$	External main supply voltage (including V_{DD} , V_{DDA} , V_{BAT})	-0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT_XXX pins	$V_{SS}-0.3$	$\min(V_{DD}, V_{DDA}) + 4.0^{(3)(4)}$	V
	Input voltage on TT_XX pins	$V_{SS}-0.3$	4.0	
	Input voltage on any other pins	$V_{SS}-0.3$	4.0	
$ \Delta V_{DDx} $	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$ V_{SSx}-V_{SS} $	Variations between all the different ground pins ⁽⁵⁾	-	50	mV

1. All main power (V_{DD} , V_{DDA} , V_{BAT}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 19: Current characteristics](#) for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

6.3 Operating conditions

6.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f _{HCLK}	Internal AHB clock frequency	-	0	80	MHz
f _{PCLK1}	Internal APB1 clock frequency	-	0	80	
f _{PCLK2}	Internal APB2 clock frequency	-	0	80	
V _{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
V _{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	V
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V _{BAT}	Backup operating voltage	-	1.55	3.6	V
V _{IN}	I/O input voltage	TT_xx I/O	-0.3	V _{DDIOx} +0.3	V
		All I/O except TT_xx	-0.3	MIN(MIN(V _{DD} , V _{DDA})+3.6 V, 5.5 V) ⁽²⁾⁽³⁾	
P _D	Power dissipation at T _A = 85 °C for suffix 6 or T _A = 105 °C for suffix 7 ⁽⁴⁾	LQFP100	-	476	mW
		LQFP64	-	444	
		LQFP48	-	350	
		UFBGA100	-	350	
		UFBGA64	-	307	
		UFQFPN48	-	606	
		UFQFPN32	-	523	
		WLCSP64	-	434	
		WLCSP49	-	416	
T _A	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	°C
		Low-power dissipation ⁽⁵⁾	-40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	105	
		Low-power dissipation ⁽⁵⁾	-40	125	
	Ambient temperature for the suffix 3 version	Maximum power dissipation	-40	125	
		Low-power dissipation ⁽⁵⁾	-40	130	
T _J	Junction temperature range	Suffix 6 version	-40	105	°C
		Suffix 7 version	-40	125	
		Suffix 3 version	-40	130	

6.3.4 Embedded voltage reference

The parameters given in [Table 24](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

Table 24. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +130\text{ }^{\circ}\text{C}$	1.182	1.212	1.232	V
$t_{S_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage	-	4 ⁽²⁾	-	-	μs
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12 ⁽²⁾	μs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20 ⁽²⁾	μA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	$V_{DD} = 3\text{ V}$	-	5	7.5 ⁽²⁾	mV
T_{Coeff}	Temperature coefficient	$-40\text{ }^{\circ}\text{C} < T_A < +130\text{ }^{\circ}\text{C}$	-	30	50 ⁽²⁾	ppm/ $^{\circ}\text{C}$
A_{Coeff}	Long term stability	1000 hours, $T = 25\text{ }^{\circ}\text{C}$	-	-	TBD ⁽²⁾	ppm
$V_{DDCoeff}$	Voltage coefficient	$3.0\text{ V} < V_{DD} < 3.6\text{ V}$	-	250	1200 ⁽²⁾	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.



Table 27. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions			TYP					MAX ⁽¹⁾					Unit
		-	Voltage scaling	f _{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I _{DD} (Run)	Supply current in Run mode	f _{HCLK} = f _{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.42	2.43	2.49	2.56	2.71	2.7	2.7	2.8	3.0	3.3	mA
				16 MHz	1.54	1.55	1.6	1.67	1.82	1.7	1.7	1.8	2.0	2.3	
				8 MHz	0.82	0.84	0.88	0.95	1.1	0.9	1.0	1.0	1.2	1.5	
				4 MHz	0.47	0.48	0.52	0.59	0.73	0.5	0.6	0.6	0.8	1.1	
				2 MHz	0.29	0.3	0.34	0.41	0.55	0.3	0.4	0.4	0.6	0.9	
				1 MHz	0.2	0.21	0.25	0.32	0.46	0.2	0.3	0.3	0.5	0.8	
				100 kHz	0.12	0.13	0.17	0.24	0.38	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	8.63	8.68	8.74	8.84	9.01	9.5	9.6	9.7	9.9	10.2	
				72 MHz	7.79	7.83	7.9	7.99	8.17	8.6	8.6	8.8	8.9	9.3	
				64 MHz	6.95	6.99	7.05	7.15	7.32	7.7	7.7	7.9	8.0	8.4	
				48 MHz	5.19	5.22	5.29	5.38	5.55	5.8	5.8	5.9	6.1	6.5	
				32 MHz	3.51	3.53	3.6	3.68	3.85	3.9	4.0	4.1	4.2	4.6	
				24 MHz	2.66	2.68	2.74	2.83	2.99	3.0	3.0	3.1	3.3	3.6	
				16 MHz	1.82	1.84	1.89	1.98	2.14	2.0	2.1	2.2	2.3	2.7	
I _{DD} (LPRun)	Supply current in low-power run mode	f _{HCLK} = f _{MSI} all peripherals disable FLASH in power-down		2 MHz	205	228	275	352	501	276.5	302.3	358.4	502.5	816.4	μA
				1 MHz	111	126	175	248	397	151.3	180.9	245.3	390.7	703.4	
				400 kHz	49.2	62.7	108	181	330	73.3	104.0	170.8	321.0	632.4	
				100 kHz	21.5	33.3	76.6	151	299	36.4	67.7	137.2	287.8	600.8	

1. Guaranteed by characterization results, unless otherwise specified.

Table 39. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB1	RTCA	1.7	1.1	2.1	μA/MHz
	CRS	0.3	0.3	0.6	
	I2C1 independent clock domain	3.5	2.8	3.4	
	I2C1 clock domain	1.1	0.9	1.0	
	I2C2 independent clock domain	3.5	3.0	3.4	
	I2C2 clock domain	1.1	0.7	0.9	
	I2C3 independent clock domain	2.9	2.3	2.5	
	I2C3 clock domain	0.9	0.4	0.8	
	LPUART1 independent clock domain	1.9	1.6	1.8	
	LPUART1 clock domain	0.6	0.6	0.6	
	LPTIM1 independent clock domain	2.9	2.4	2.8	
	LPTIM1 clock domain	0.8	0.4	0.7	
	LPTIM2 independent clock domain	3.1	2.7	3.9	
	LPTIM2 clock domain	0.8	0.7	0.8	
	OPAMP	0.4	0.2	0.4	
	PWR	0.4	0.1	0.4	
	SPI2	1.8	1.6	1.6	
	SPI3	1.7	1.3	1.6	
	SWPMI1 independent clock domain	1.9	1.6	1.9	
	SWPMI1 clock domain	0.9	0.7	0.8	
	TIM2	6.2	5.0	5.9	
	TIM6	1.0	0.6	0.9	
	TIM7	1.0	0.6	0.6	
	USART2 independent clock domain	4.1	3.6	3.8	
	USART2 clock domain	1.3	0.9	1.1	
	USART3 independent clock domain	4.3	3.5	4.2	
	USART3 clock domain	1.5	1.1	1.3	
	WWDG	0.5	0.5	0.5	
	All APB1 on	45.4	35	47.8	
APB2	AHB to APB2 ⁽⁴⁾	1.0	0.9	0.9	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 59](#) are derived from tests performed under the conditions summarized in [Table 21: General operating conditions](#). All I/Os are designed as CMOS- and TTL-compliant.

Table 59. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}^{(1)}$	I/O input low level voltage	$1.62\text{ V} < V_{DDIOx} < 3.6\text{ V}$	-	-	$0.3 \times V_{DDIOx}^{(2)}$	V
	I/O input low level voltage	$1.62\text{ V} < V_{DDIOx} < 3.6\text{ V}$	-	-	$0.39 \times V_{DDIOx} - 0.06^{(3)}$	
	I/O input low level voltage	$1.08\text{ V} < V_{DDIOx} < 1.62\text{ V}$	-	-	$0.43 \times V_{DDIOx} - 0.1^{(3)}$	
$V_{IH}^{(1)}$	I/O input high level voltage	$1.62\text{ V} < V_{DDIOx} < 3.6\text{ V}$	$0.7 \times V_{DDIOx}^{(2)}$	-	-	V
	I/O input high level voltage	$1.62\text{ V} < V_{DDIOx} < 3.6\text{ V}$	$0.49 \times V_{DDIOx} + 0.26^{(3)}$	-	-	
	I/O input high level voltage	$1.08\text{ V} < V_{DDIOx} < 1.62\text{ V}$	$0.61 \times V_{DDIOx} + 0.05^{(3)}$	-	-	
$V_{hys}^{(3)}$	TT_xx, FT_XXX and NRST I/O input hysteresis	$1.62\text{ V} < V_{DDIOx} < 3.6\text{ V}$	-	200	-	mV
	FT_sx	$1.08\text{ V} < V_{DDIOx} < 1.62\text{ V}$	-	150	-	
I_{lkg}	FT_xx input leakage current ⁽³⁾	$V_{IN} \leq \text{Max}(V_{DDXXX})^{(4)}$	-	-	± 100	nA
		$\text{Max}(V_{DDXXX}) \leq V_{IN} \leq \text{Max}(V_{DDXXX}) + 1\text{ V}^{(4)(5)}$	-	-	$650^{(3)(6)}$	
		$\text{Max}(V_{DDXXX}) + 1\text{ V} < V_{IN} \leq 5.5\text{ V}^{(3)(5)}$	-	-	$200^{(6)}$	
	FT_u and PC3 IO	$V_{IN} \leq \text{Max}(V_{DDXXX})^{(4)}$	-	-	± 150	
		$\text{Max}(V_{DDXXX}) \leq V_{IN} \leq \text{Max}(V_{DDXXX}) + 1\text{ V}^{(4)}$	-	-	$2500^{(3)(7)}$	
		$\text{Max}(V_{DDXXX}) + 1\text{ V} < V_{IN} \leq 5.5\text{ V}^{(4)(5)(7)}$	-	-	$250^{(7)}$	
	TT_xx input leakage current	$V_{IN} \leq \text{Max}(V_{DDXXX})^{(6)}$	-	-	± 150	
		$\text{Max}(V_{DDXXX}) \leq V_{IN} < 3.6\text{ V}^{(6)}$	-	-	$2000^{(3)}$	
R_{PU}	Weak pull-up equivalent resistor ⁽⁸⁾	$V_{IN} = V_{SS}$	25	40	55	k Ω
R_{PD}	Weak pull-down equivalent resistor ⁽⁸⁾	$V_{IN} = V_{DDIOx}$	25	40	55	k Ω
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Refer to [Figure 27: I/O input characteristics](#).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#). All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 60. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.4$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	1.3	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx} - 1.3$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 4 \text{ mA}$ $V_{DDIOx} \geq 1.62 \text{ V}$	-	0.45	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.45$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 2 \text{ mA}$ $1.62 \text{ V} \geq V_{DDIOx} \geq 1.08 \text{ V}$	-	$0.35 \times V_{DDIOx}$	
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$0.65 \times V_{DDIOx}$	-	
$V_{OLFM+}^{(3)}$	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	
		$ I_{IO} = 10 \text{ mA}$ $V_{DDIOx} \geq 1.62 \text{ V}$	-	0.4	
		$ I_{IO} = 2 \text{ mA}$ $1.62 \text{ V} \geq V_{DDIOx} \geq 1.08 \text{ V}$	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 18: Voltage characteristics](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 28](#) and [Table 61](#), respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

6.3.18 Digital-to-Analog converter characteristics

Table 70. DAC characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DDA}	Analog supply voltage for DAC ON	-		1.8	-	3.6	V
V _{REF+}	Positive reference voltage	-		1.8	-	V _{DDA}	
V _{REF-}	Negative reference voltage	-		V _{SSA}			
R _L	Resistive load	DAC output buffer ON	connected to V _{SSA}	5	-	-	kΩ
			connected to V _{DDA}	25	-	-	
R _O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R _{BON}	Output impedance sample and hold mode, output buffer ON	V _{DD} = 2.7 V		-	-	2	kΩ
		V _{DD} = 2.0 V		-	-	3.5	
R _{BOFF}	Output impedance sample and hold mode, output buffer OFF	V _{DD} = 2.7 V		-	-	16.5	kΩ
		V _{DD} = 2.0 V		-	-	18.0	
C _L	Capacitive load	DAC output buffer ON		-	-	50	pF
C _{SH}		Sample and hold mode		-	0.1	1	μF
V _{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V _{REF+} – 0.2	V
		DAC output buffer OFF		0	-	V _{REF+}	
t _{SETTLING}	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	μs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t _{WAKEUP} ⁽²⁾	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	μs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V _{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

SAI characteristics

Unless otherwise specified, the parameters given in [Table 85](#) for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 21: General operating conditions](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitive load $C = 30$ pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 85. SAI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency ⁽²⁾	Master transmitter $2.7 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	18.5	MHz
		Master transmitter $1.71 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	12.5	
		Master receiver Voltage Range 1	-	25	
		Slave transmitter $2.7 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	22.5	
		Slave transmitter $1.71 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	14.5	
		Slave receiver Voltage Range 1	-	25	
		Voltage Range 2	-	12.5	
$t_{V(FS)}$	FS valid time	Master mode $2.7 \leq V_{DD} \leq 3.6$	-	22	ns
		Master mode $1.71 \leq V_{DD} \leq 3.6$	-	40	
$t_{h(FS)}$	FS hold time	Master mode	10	-	ns
$t_{su(FS)}$	FS setup time	Slave mode	1	-	ns
$t_{h(FS)}$	FS hold time	Slave mode	2	-	ns
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	2	-	ns
$t_{su(SD_B_SR)}$		Slave receiver	1.5	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	5	-	ns
$t_{h(SD_B_SR)}$		Slave receiver	2.5	-	

Table 93. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 52. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package recommended footprint

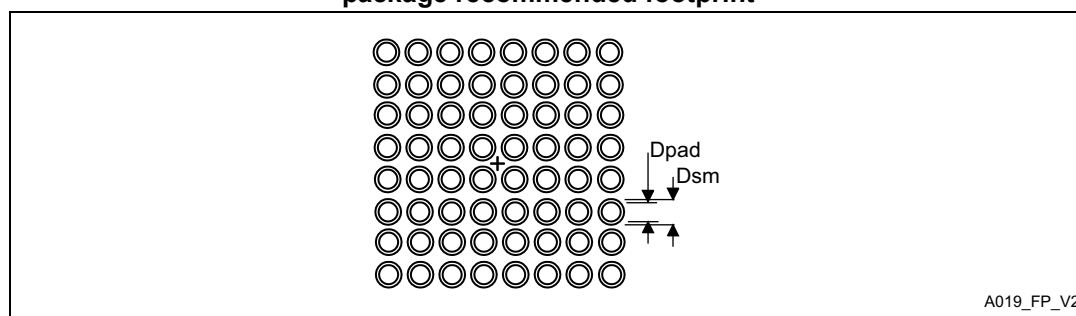


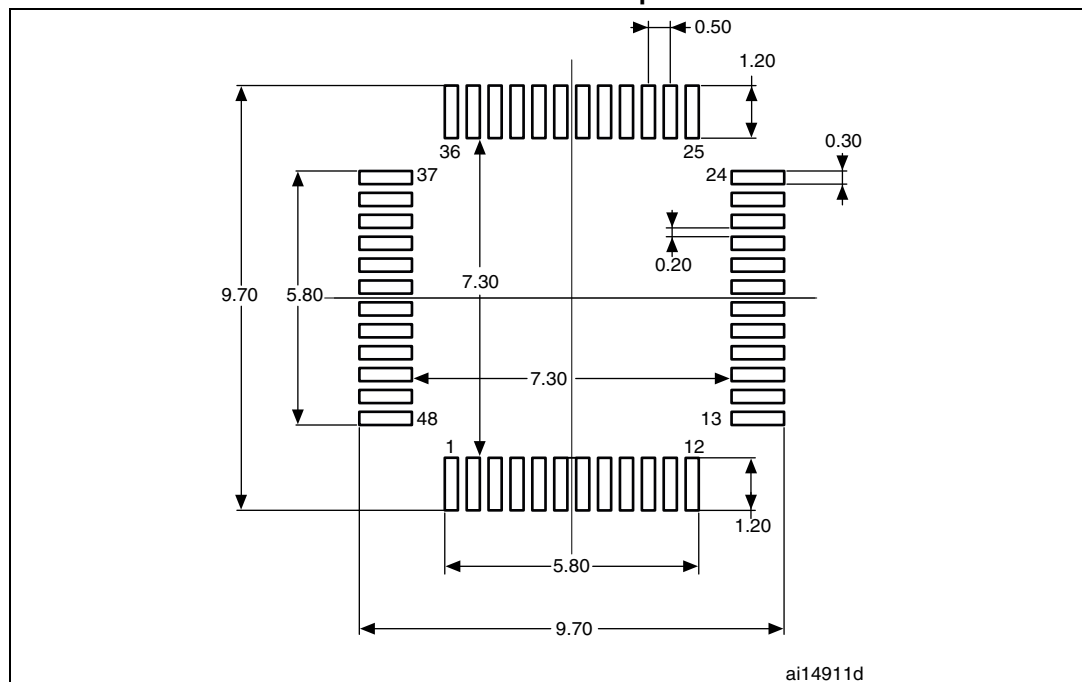
Table 94. UFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 61. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

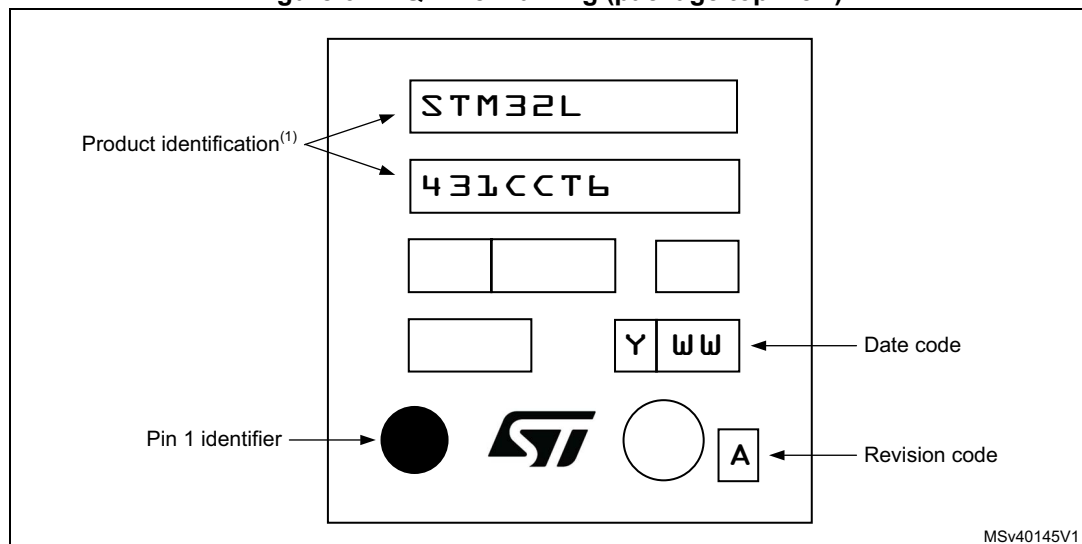


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 62. LQFP48 marking (package top view)



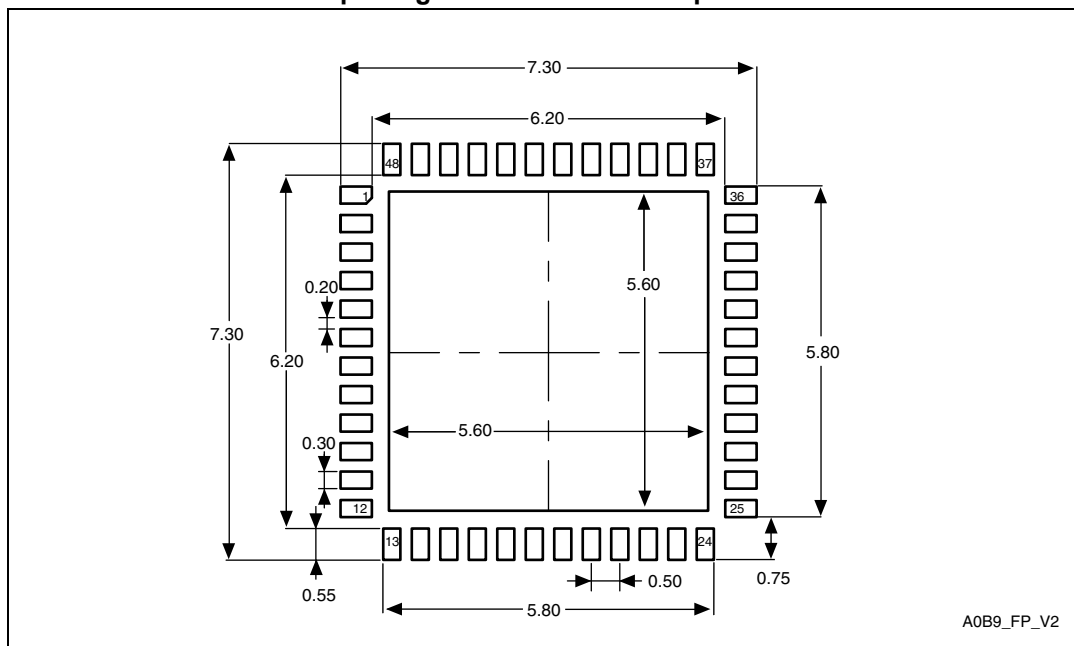
MSv40145V1

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 100. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 64. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

9 Revision history

Table 104. Document revision history

Date	Revision	Changes
31-May-2016	1	Initial release.

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