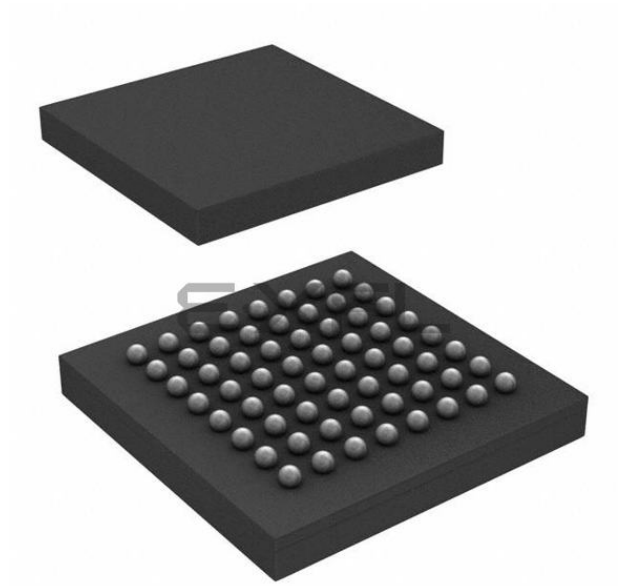

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (3.14x3.13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l431rby6tr

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32L431xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32L431xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.10 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, low-power run and sleep, Stop 0, Stop 1 and Stop 2 modes.

Table 5. STM32L431xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADCx DACx	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
TIM15/TIM16	IRTIM	Infrared interface output generation	Y	Y	Y	Y	-	-
COMPx	TIM1 TIM2	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y (1)
ADCx	TIM1	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y (1)
All clocks sources (internal and external)	TIM2 TIM15, 16	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1 TIM15,16	Timer break	Y	Y	Y	Y	-	-

Table 5. STM32L431xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y (1)
	ADCx DACx	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

3.22 Timers and watchdogs

The STM32L431xx includes one advanced control timers, up to five general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 9. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.22.1 Advanced-control timer (TIM1)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.22.2*) using the same architecture, so the advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.23 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

Table 12. SAI implementation

SAI features	Support[1]
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X
Mute mode	X
Stereo/Mono audio frame capability.	X
16 slots	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X
FIFO Size	X (8 Word)
SPDIF	X

1. X: supported

3.29 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

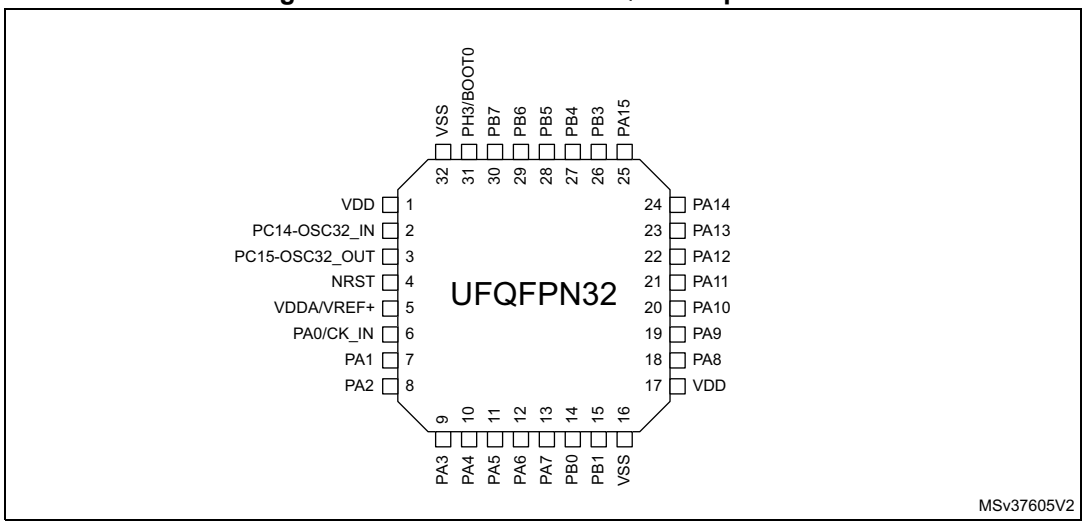
3.30 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

The CAN peripheral supports:

- Supports CAN protocol version 2.0 A, B Active
- Bit rates up to 1 Mbit/s

Figure 13. STM32L431Kx UFQFPN32 pinout(1)



1. The above figure shows the package top view.

Table 13. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os	
		_f (1)	I/O, Fm+ capable
		_a (2)	I/O, with Analog switch function supplied by V_{DDA}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 14* are: FT_f, FT_fa.
2. The related I/O structures in *Table 14* are: FT_a, FT_fa, TT_a.

Table 14. STM32L431xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN32	LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
8	12	12	E5	F6	16	F3	25	K3	PA2	I/O	FT_a	-	TIM2_CH3, USART2_TX, LPUART1_TX, QUADSPI_BK1_NCS, COMP2_OUT, TIM15_CH1, EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4, LSCO
9	13	13	E4	G6	17	G3	26	L3	PA3	I/O	TT_a	-	TIM2_CH4, USART2_RX, LPUART1_RX, QUADSPI_CLK, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_ VOUT, COMP2_INP, ADC1_IN8
-	-	-	-	H8	18	C2	27	E3	VSS	S	-	-	-	-
-	-	-	-	H7	19	D2	28	H3	VDD	S	-	-	-	-
10	14	14	G6	E5	20	H3	29	M3	PA4	I/O	TT_a	-	SPI1_NSS, SPI3_NSS, USART2_CK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9, DAC1_OUT1
11	15	15	F5	F5	21	F4	30	K4	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, LPTIM2_ETR, EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10, DAC1_OUT2
12	16	16	F4	G5	22	G4	31	L4	PA6	I/O	FT_a	-	TIM1_BKIN, SPI1_MISO, COMP1_OUT, USART3_CTS, LPUART1_CTS, QUADSPI_BK1_IO3, TIM1_BKIN_COMP2, TIM16_CH1, EVENTOUT	ADC1_IN11
13	17	17	F3	H6	23	H4	32	M4	PA7	I/O	FT_fa	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, COMP2_OUT, EVENTOUT	ADC1_IN12
-	-	-	-	D4	24	H5	33	K5	PC4	I/O	FT_a	-	USART3_TX, EVENTOUT	COMP1_INM, ADC1_IN13
-	-	-	-	E4	25	H6	34	L5	PC5	I/O	FT_a	-	USART3_RX, EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5

Table 15. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 16*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3	USART1/ USART2/ USART3
Port B	PB0	-	TIM1_CH2N	-	-	-	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	-	-	-	-	-	USART3_RTS_ DE
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-	-	-
	PB3	JTDO-TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_ DE
	PB4	NJTRST	-	-	-	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS
Port B	PB5	-	LPTIM1_IN1	-	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	-	-	I2C1_SCL	-	-	USART1_TX
	PB7	-	LPTIM1_IN2	-	-	I2C1_SDA	-	-	USART1_RX
	PB8	-	-	-	-	I2C1_SCL	-	-	-
	PB9	-	IR_OUT	-	-	I2C1_SDA	SPI2_NSS	-	-
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK	-	USART3_TX
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN_ COMP2	I2C2_SMBA	SPI2_NSS	-	USART3_CK
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	-	USART3_CTS
	PB14	-	TIM1_CH2N	-	-	I2C2_SDA	SPI2_MISO	-	USART3_RTS_ DE
	PB15	RTC_REFIN	TIM1_CH3N	-	-	-	SPI2_MOSI	-	-

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA})+3.6 V and 5.5V.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.10: Thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.10: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 22* are derived from tests performed under the ambient temperature condition summarized in *Table 21*.

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		10	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature conditions summarized in *Table 21: General operating conditions*.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	

Table 37. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	63	133	522	1 490	4 270	-	-	-	-	-	nA
			2.4 V	165	253	710	1 830	4 980	-	-	-	-	-	
			3 V	316	423	990	2 340	6 050	-	-	-	-	-	
			3.6 V	649	787	1 530	3 220	7 710	-	-	-	-	-	
		RTC clocked by LSE quartz (2) in low drive mode	1.8 V	203	293	700	1 675	-	-	-	-	-	-	
			2.4 V	303	411	880	2 001	-	-	-	-	-	-	
			3 V	448	567	1 136	2 479	-	-	-	-	-	-	
			3.6 V	744	887	1 609	3 256	-	-	-	-	-	-	
I_{DD}(wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz. See (3).	3 V	0.780	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 40: Low-power mode wakeup timings*.

Table 61. I/O AC characteristics(1)(2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	52	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	140	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	110	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	10	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	15	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	16	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	40	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	9	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	21	

Table 64. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 80 MHz	0.03125	-	8.00625	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	0.1875	-	8.1625	µs
		Resolution = 12 bits	ts + 12.5 cycles for successive approximation = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 5 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	-	260	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

Table 66. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+}$ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	-74	-73	dB
				Slow channel (max speed)	-	-74	-73	
			Differential	Fast channel (max speed)	-	-79	-76	
				Slow channel (max speed)	-	-79	-76	

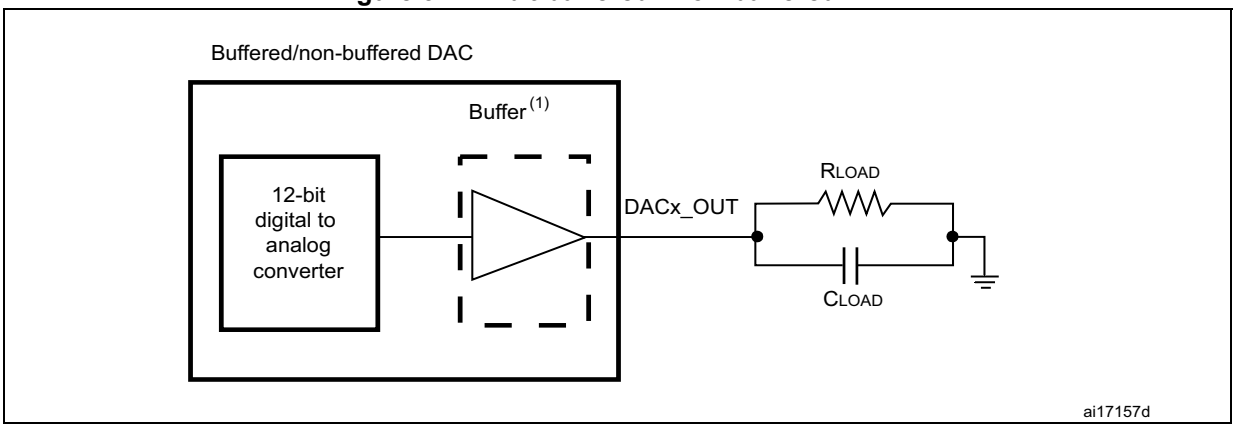
1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 68. ADC accuracy - limited test conditions 3(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

3. Refer to *Table 59: I/O static characteristics*.
4. Ton is the Refresh phase duration. Toff is the Hold phase duration. Refer to RM0392 reference manual for more details.

Figure 32. 12-bit buffered / non-buffered DAC

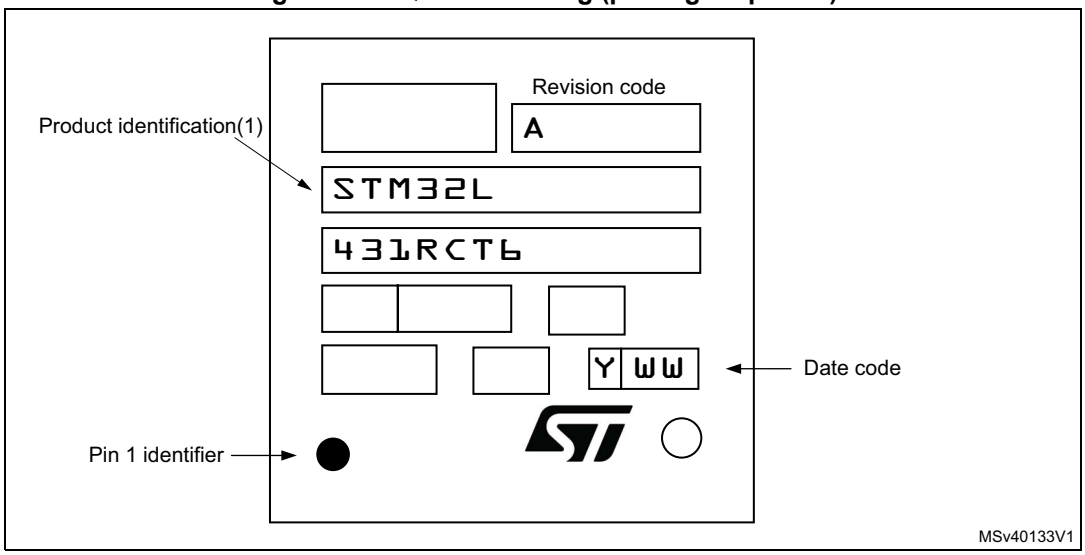


1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 71. DAC accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	

Figure 50. LQFP64 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 93. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 52. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package recommended footprint

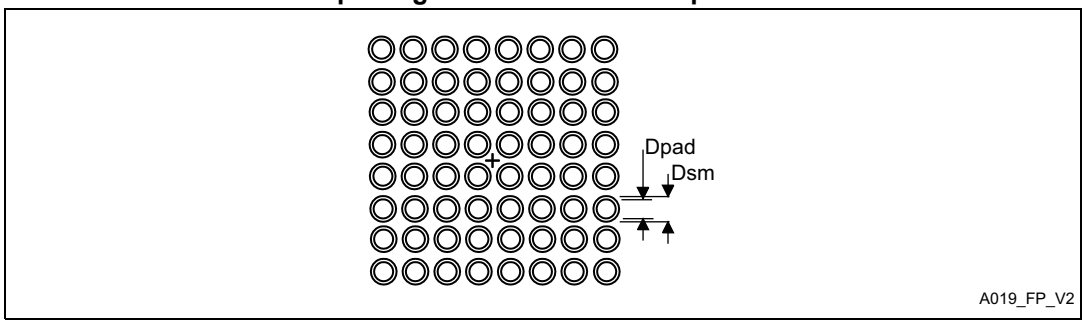


Table 94. UFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

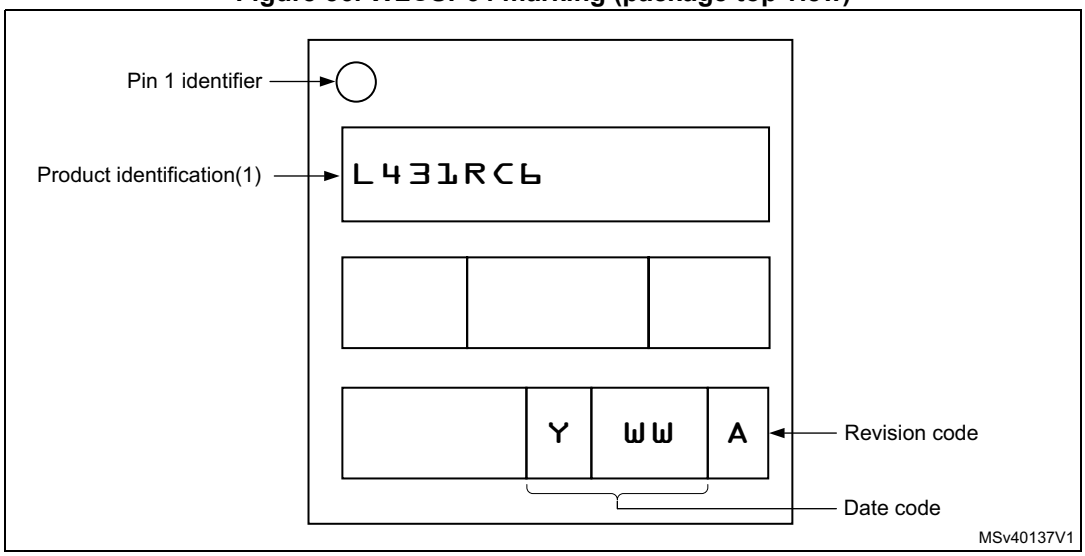
Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 56. WLCSP64 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.