Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

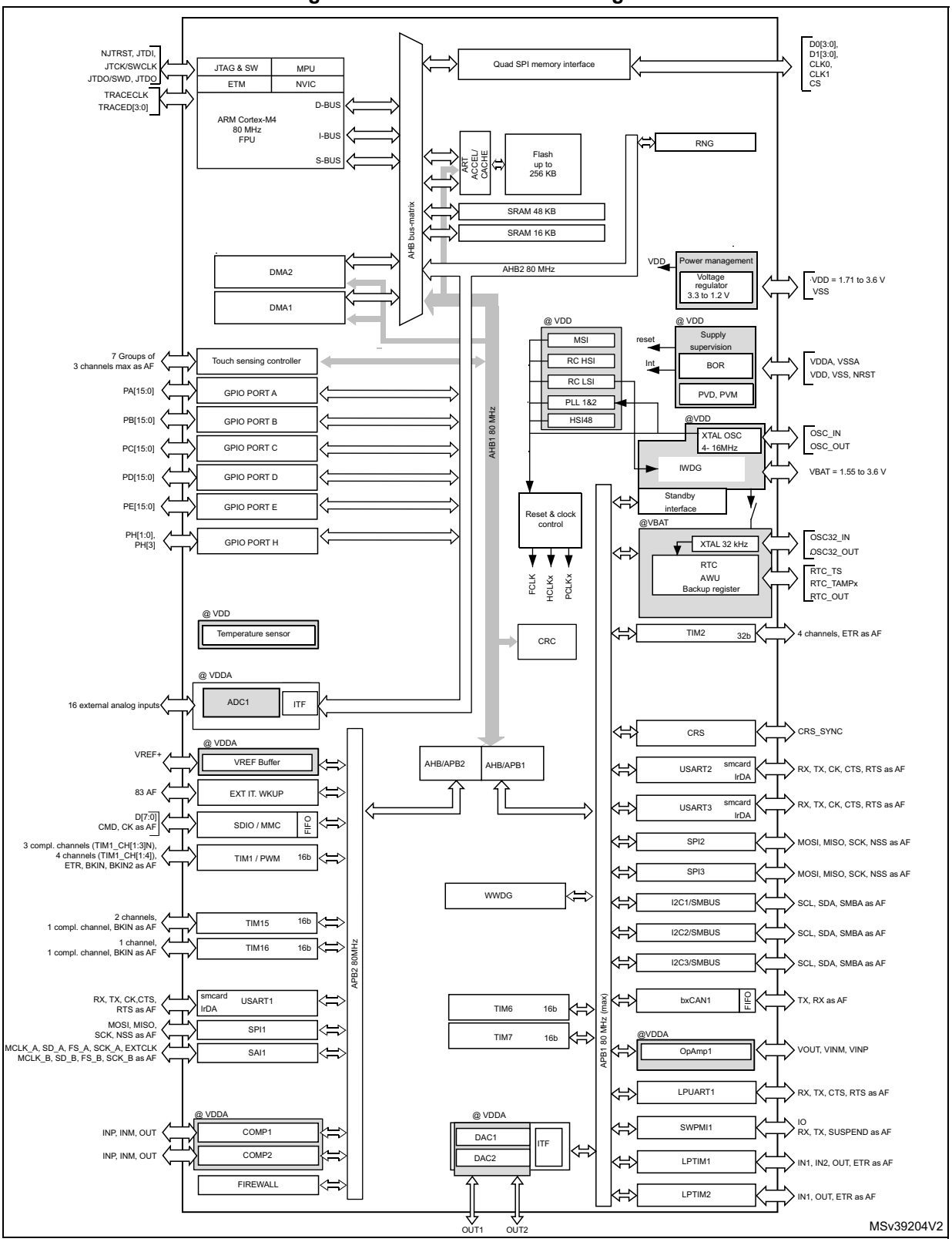
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l431rct6

Table 2. STM32L431xx family device features and peripheral counts (continued)

Peripheral		STM32L431Vx	STM32L431Rx	STM32L431Cx	STM32L431Kx
Timers	Advanced control	1 (16-bit)			
	General purpose	2 (16-bit) 1 (32-bit)			
	Basic	2 (16-bit)			
	Low -power	2 (16-bit)			
	SysTick timer	1			
	Watchdog timers (independent, window)	2			
Comm. interfaces	SPI	3			2
	I^2C	3			2
	USART LPUART	3 1			2 1
	SAI	1			
	CAN	1			
	SDMMC	Yes		No	
	SWPMI	Yes			
RTC		Yes			
Tamper pins		3	2	2	1
Random generator		Yes			
GPIOs Wakeup pins		83 5	52 4	38 or 39(1) 3	26 2
Capacitive sensing Number of channels		21	12	6	3
12-bit ADCs Number of channels		1 16	1 16	1 10	1 10
12-bit DAC channels		2			
Internal voltage reference buffer		Yes	No		
Analog comparator		2			
Operational amplifiers		1			
Max. CPU frequency		80 MHz			
Operating voltage		1.71 to 3.6 V			
Operating temperature		Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C			
Packages		LQFP100 UFBGA100	WLCSP64 LQFP64 UFBGA64	WLCSP49 LQFP48 UFQFPN48	UFQFPN32

1. For WLCSP49 package.

Figure 1. STM32L431xx block diagram



Note: AF: alternate function on I/O pins.

- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.17 Voltage reference buffer (VREFBUF)

The STM32L431xx devices embed an voltage reference buffer which can be used as voltage reference for ADCs, DACs and also as voltage reference for external components through the VREF+ pin.

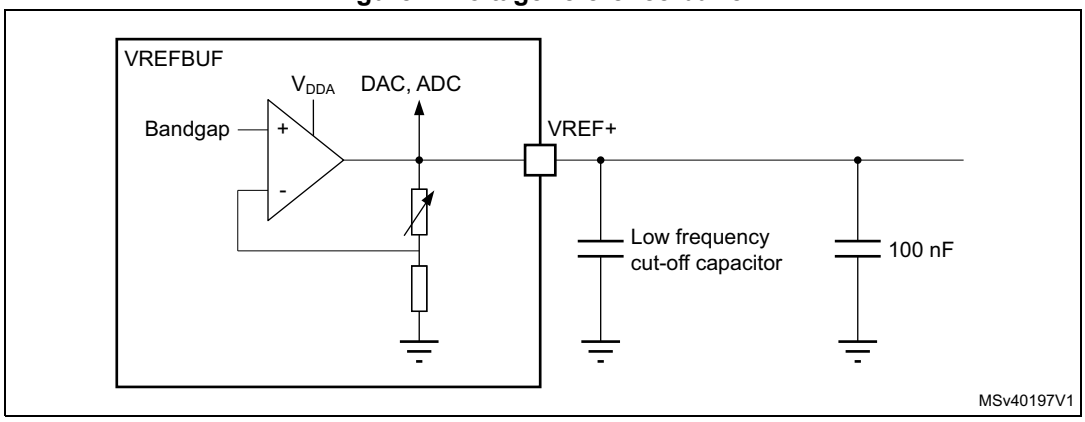
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 4. Voltage reference buffer



3.18 Comparators (COMP)

The STM32L431xx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

3.22.5 Infrared interface (IRTIM)

The STM32L431xx includes one infrared interface (IRTIM). It can be used with an infrared LED to perform remote control functions. It uses TIM15 and TIM16 output channels to generate output signal waveforms on IR_OUT pin.

3.22.6 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.22.7 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.22.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

Table 14. STM32L431xx pin definitions

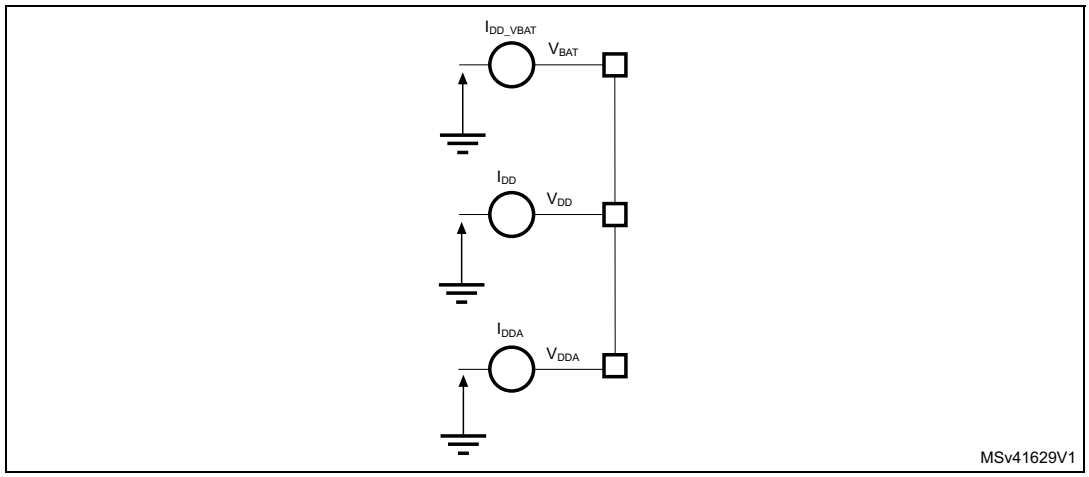
Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN32	LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	-	-	1	B2	PE2	I/O	FT	-	TRACECK, TSC_G7_IO1, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	-	2	A1	PE3	I/O	FT	-	TRACED0, TSC_G7_IO2, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	-	-	3	B1	PE4	I/O	FT	-	TRACED1, TSC_G7_IO3, SAI1_FS_A, EVENTOUT	-
-	-	-	-	-	-	-	4	C2	PE5	I/O	FT	-	TRACED2, TSC_G7_IO4, SAI1_SCK_A, EVENTOUT	-
-	-	-	-	-	-	-	5	D2	PE6	I/O	FT	-	TRACED3, SAI1_SD_A, EVENTOUT	RTC_TAMP3, WKUP3
-	1	1	B6	B7	1	B2	6	E2	VBAT	S	-	-	-	-
-	2	2	B7	B8	2	A2	7	C1	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
2	3	3	C7	C8	3	A1	8	D1	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
3	4	4	C6	C7	4	B1	9	E1	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	-	10	F2	VSS	S	-	-	-	-
-	-	-	-	-	-	-	11	G2	VDD	S	-	-	-	-
-	5	5	D7	D8	5	C1	12	F1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
-	6	6	D6	D7	6	D1	13	G1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
4	7	7	D5	D6	7	E1	14	H2	NRST	I/O	RST	-	-	-

Table 15. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 16*)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3	USART1/ USART2/ USART3
Port A	PA0	-	TIM2_CH1	-	-	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	-	-	I2C1_SMBA	SPI1_SCK	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	-	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	-	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	-	-	-	SPI1_MISO	COMP1_OUT	USART3_CTS
	PA7	-	TIM1_CH1N	-	-	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	-	I2C1_SCL	-	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	I2C1_SDA	-	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	COMP1_OUT	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	-	USART1_RTS_ DE
	PA13	JTMS-SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK-SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_RTS_ DE

6.1.7 Current consumption measurement

Figure 18. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18: Voltage characteristics*, *Table 19: Current characteristics* and *Table 20: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 18. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{BAT})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}) + 4.0(3)(4)	V
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins(5)	-	50	mV

1. All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 19: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA})+3.6 V and 5.5V.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.10: Thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.10: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 22* are derived from tests performed under the ambient temperature condition summarized in *Table 21*.

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		10	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature conditions summarized in *Table 21: General operating conditions*.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	

Table 31. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.68	0.69	0.74	0.81	0.95	0.8	0.8	0.9	1.0	1.3	mA
				16 MHz	0.46	0.48	0.52	0.59	0.73	0.5	0.6	0.6	0.8	1.1	
				8 MHz	0.29	0.30	0.34	0.41	0.55	0.3	0.4	0.4	0.6	0.9	
				4 MHz	0.20	0.21	0.25	0.32	0.46	0.2	0.3	0.3	0.5	0.8	
				2 MHz	0.16	0.17	0.21	0.28	0.42	0.2	0.2	0.3	0.4	0.7	
				1 MHz	0.13	0.15	0.19	0.26	0.40	0.1	0.2	0.3	0.4	0.7	
				100 kHz	0.11	0.13	0.17	0.24	0.38	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	2.23	2.25	2.30	2.38	2.54	2.5	2.5	2.6	2.8	3.1	
				72 MHz	2.02	2.04	2.10	2.18	2.34	2.2	2.3	2.4	2.5	2.9	
				64 MHz	1.82	1.84	1.89	1.98	2.14	2.0	2.1	2.1	2.3	2.6	
				48 MHz	1.34	1.36	1.42	1.50	1.66	1.5	1.6	1.7	1.8	2.2	
				32 MHz	0.93	0.95	1.01	1.09	1.25	1.1	1.1	1.2	1.4	1.7	
				24 MHz	0.73	0.75	0.80	0.88	1.04	0.8	0.9	1.0	1.1	1.4	
				16 MHz	0.53	0.55	0.60	0.68	0.84	0.6	0.6	0.7	0.9	1.2	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	71.8	80.7	125	200	350	91.1	122.7	191.3	341.5	653.5	µA
				1 MHz	45.0	57.3	101	176	325	63.2	95.4	165.4	316.5	628.7	
				400 kHz	27.0	40.7	84.6	158	308	43.9	75.8	147.2	297.6	609.2	
				100 kHz	22.8	30.9	63.3	113.2	207.7	35.2	67.9	140.9	290.8	602.4	

1. Guaranteed by characterization results, unless otherwise specified.

Table 32. Current consumption in Low-power sleep modes, Flash in power-down

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	58.7	70.7	103.2	153.7	248.5	80	113	180	330	641	µA
				1 MHz	39.4	47.2	79.3	129.6	224.8	53	86	154	304	616	
				400 kHz	20.8	30.8	62.1	112.5	207.8	35	67	137	286	597	
				100 kHz	14.3	23.1	55.1	105.7	201.5	27	58	130	279	590	

1. Guaranteed by characterization results, unless otherwise specified.

Table 33. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	1	2.54	8.74	19.8	43.4	2.0	5.6	21.1	50.8	116.0	µA
			2.4 V	1.02	2.59	8.89	20.2	44.3	2.1	5.8	21.6	52.3	119.6	
			3 V	1.06	2.67	9.11	20.7	45.5	2.1	5.9	22.2	53.7	123.2	
			3.6 V	1.23	2.88	9.56	21.6	47.3	2.3	6.1	23.0	55.8	127.9	
I_{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	1.3	2.82	9.02	20.1	43.6	2.5	6.2	21.6	51.3	116.3	µA
			2.4 V	1.39	2.95	9.24	20.5	44.6	2.8	6.4	22.3	52.8	120.0	
			3 V	1.5	3.11	9.55	21.1	45.8	3.0	6.8	23.0	54.5	123.8	
			3.6 V	1.76	3.42	10.1	22.1	47.8	3.3	7.2	24.1	56.7	128.7	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	1.36	2.9	9.1	20.1	43.7	-	-	-	-	-	
			2.4 V	1.48	3.09	9.44	20.8	45	-	-	-	-	-	
			3 V	1.83	3.67	10.4	22.3	47.3	-	-	-	-	-	
			3.6 V	3.58	6.17	13.9	26.6	53	-	-	-	-	-	
		RTC clocked by LSE quartz(2) in low drive mode	1.8 V	1.28	2.81	9.13	20.8	-	-	-	-	-	-	
			2.4 V	1.39	2.93	9.34	21.3	-	-	-	-	-	-	
			3 V	1.59	3.1	9.64	21.8	-	-	-	-	-	-	
			3.6 V	1.86	3.45	10.2	22.8	-	-	-	-	-	-	

Table 36. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(SRAM2) (4)	Supply current to be added in Standby mode when SRAM2 is retained	-	1.8 V	173	349	1 009	2 158	4 542	249	527	1604	3402	6908	nA
			2.4 V	174	345	1 015	2 163	4 535	271	589	1623	3438	6924	
			3 V	178	350	1 019	2 148	4 419	277	594	1628	3467	6935	
			3.6 V	184	352	1 033	2 208	4 610	293	611	1631	3480	6948	
I_{DD}(wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is MSI = 4 MHz. See (5).	3 V	1.23	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. The supply current in Standby with SRAM2 mode is: I_{DD}(Standby) + I_{DD}(SRAM2). The supply current in Standby with RTC with SRAM2 mode is: I_{DD}(Standby + RTC) + I_{DD}(SRAM2).
5. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 40: Low-power mode wakeup timings*.

Table 37. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	7.82	190	386	1 286	3 854	25.0	255	1721	5052	15543	nA
			2.4 V	23	229	485	1 517	4 431	34.9	270	2085	5878	17639	
			3 V	44.3	290	634	1 878	5 310	70.1	345	2454	6755	19984	
			3.6 V	212	397	977	2 516	6 656	119.1	496	2992	7939	22860	

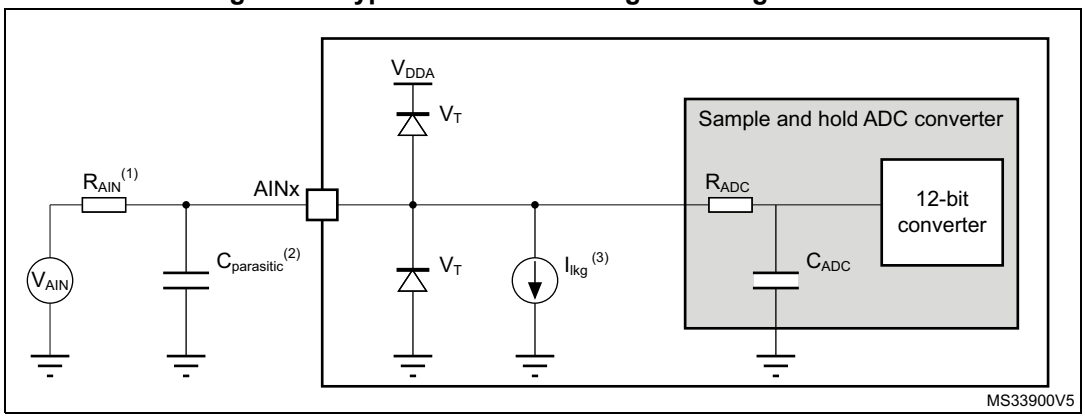
Table 39. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB1	RTCA	1.7	1.1	2.1	µA/MHz
	CRS	0.3	0.3	0.6	
	I2C1 independent clock domain	3.5	2.8	3.4	
	I2C1 clock domain	1.1	0.9	1.0	
	I2C2 independent clock domain	3.5	3.0	3.4	
	I2C2 clock domain	1.1	0.7	0.9	
	I2C3 independent clock domain	2.9	2.3	2.5	
	I2C3 clock domain	0.9	0.4	0.8	
	LPUART1 independent clock domain	1.9	1.6	1.8	
	LPUART1 clock domain	0.6	0.6	0.6	
	LPTIM1 independent clock domain	2.9	2.4	2.8	
	LPTIM1 clock domain	0.8	0.4	0.7	
	LPTIM2 independent clock domain	3.1	2.7	3.9	
	LPTIM2 clock domain	0.8	0.7	0.8	
	OPAMP	0.4	0.2	0.4	
	PWR	0.4	0.1	0.4	
	SPI2	1.8	1.6	1.6	
	SPI3	1.7	1.3	1.6	
	SWPMI1 independent clock domain	1.9	1.6	1.9	
	SWPMI1 clock domain	0.9	0.7	0.8	
	TIM2	6.2	5.0	5.9	
	TIM6	1.0	0.6	0.9	
	TIM7	1.0	0.6	0.6	
	USART2 independent clock domain	4.1	3.6	3.8	
	USART2 clock domain	1.3	0.9	1.1	
	USART3 independent clock domain	4.3	3.5	4.2	
	USART3 clock domain	1.5	1.1	1.3	
	WWDG	0.5	0.5	0.5	
	All APB1 on	45.4	35	47.8	
APB2	AHB to APB2[4]	1.0	0.9	0.9	

Table 66. ADC accuracy - limited test conditions 1(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Figure 31. Typical connection diagram using the ADC



1. Refer to *Table 64: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 59: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 59: I/O static characteristics* for the values of Ilkg.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 17: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Table 82. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 < V_{DD} < 3.6 V Voltage Range 1	-	12.5	13.5	ns
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 1	-	12.5	24	
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 2	-	12.5	33	
$t_{v(MO)}$		Master mode	-	4.5	6	
$t_{h(SO)}$	Data output hold time	Slave mode	7	-	-	ns
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.

Figure 33. SPI timing diagram - slave mode and CPHA = 0

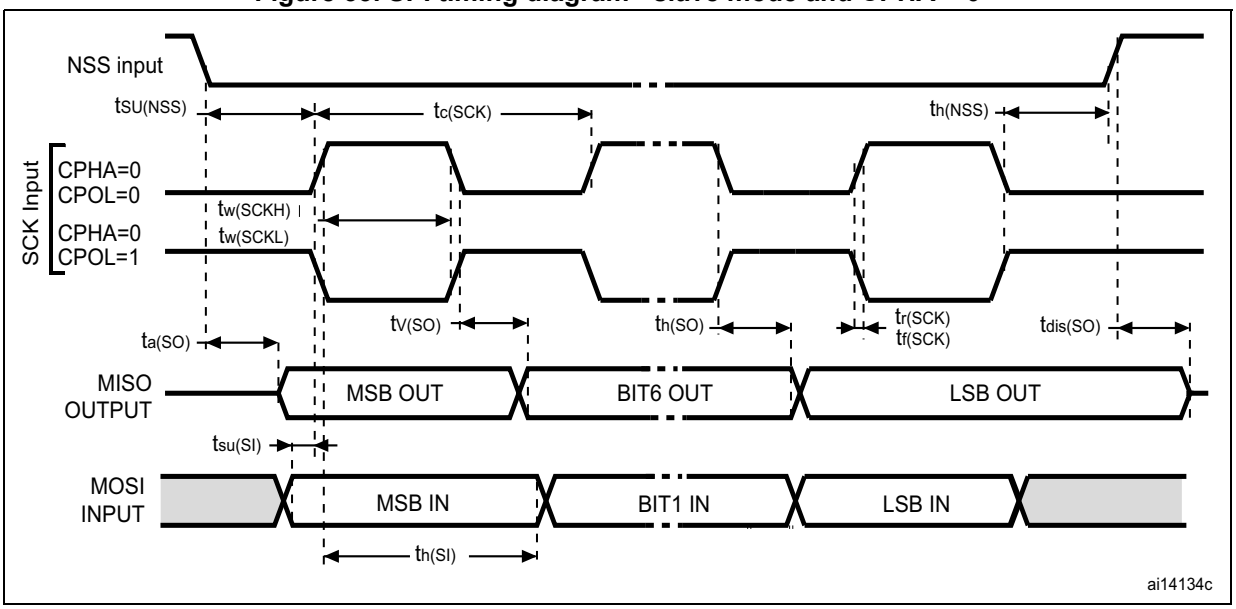
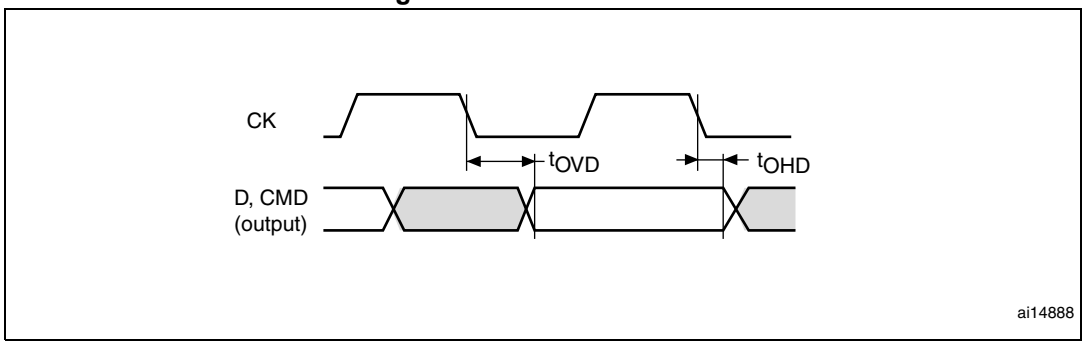


Figure 41. SD default mode



CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

SWPMI characteristics

The Single Wire Protocol Master Interface (SWPMI) and the associated SWPMI_IO transceiver are compliant with the ETSI TS 102 613 technical specification.

Table 88. SWPMI electrical characteristics

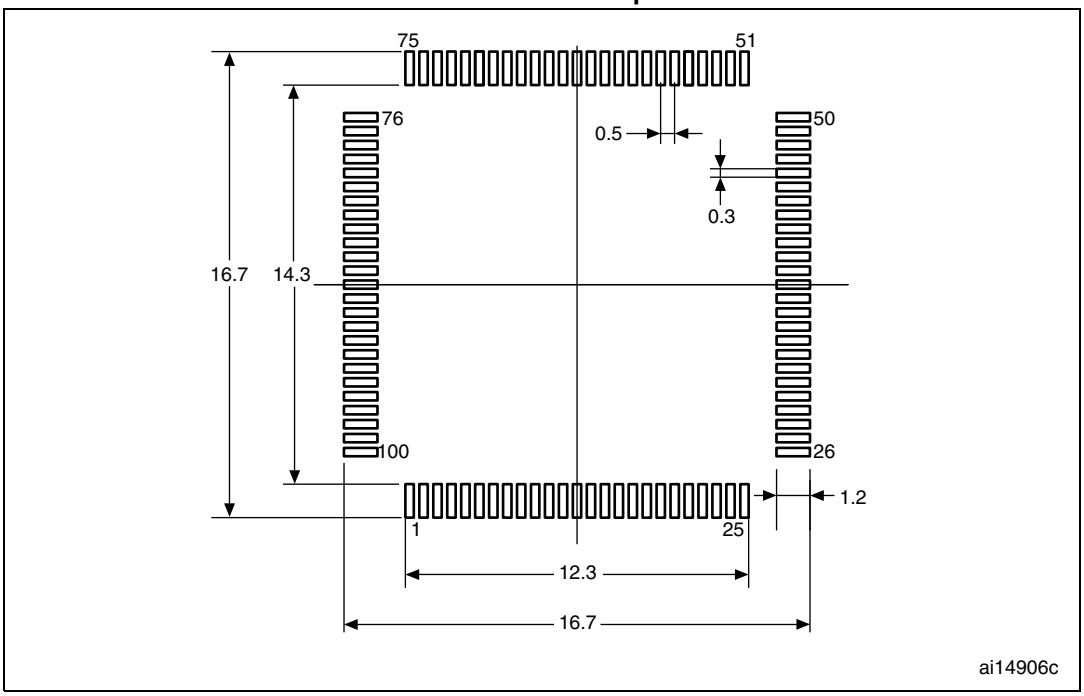
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SWPSTART}$	SWPMI regulator startup time	SWP Class B 2.7 V ≤ V_{DD} ≤ 3,3V	-	-	300	µs
t_{SWPBIT}	SWP bit duration	V_{CORE} voltage range 1	500	-	-	ns
		V_{CORE} voltage range 2	620	-	-	

Table 89. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 43. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

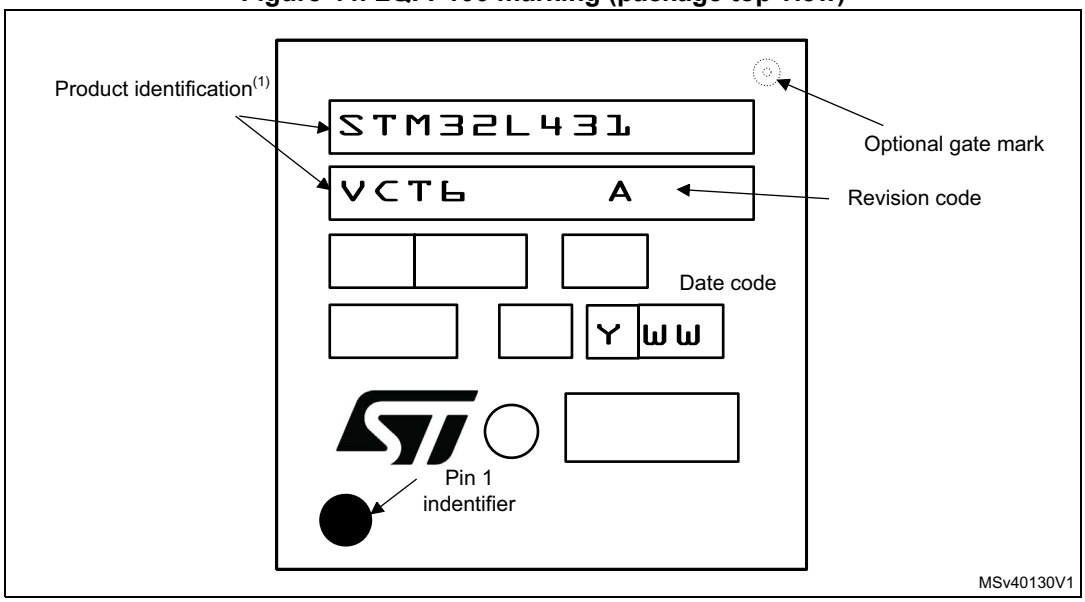


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 44. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 90. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

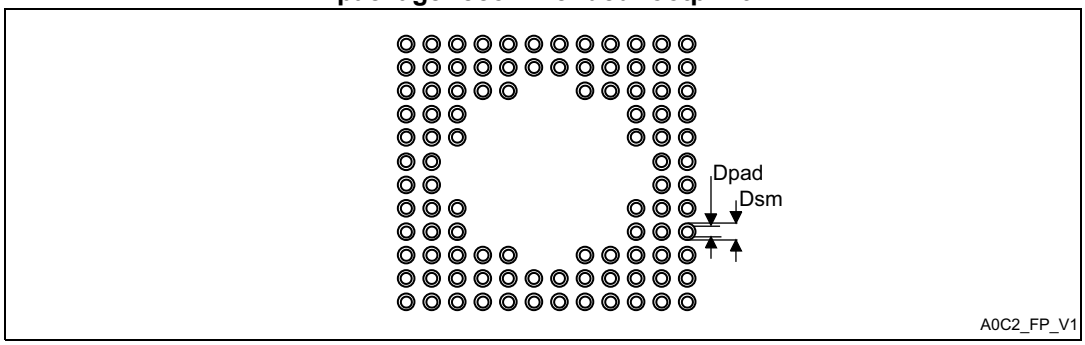


Table 91. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.