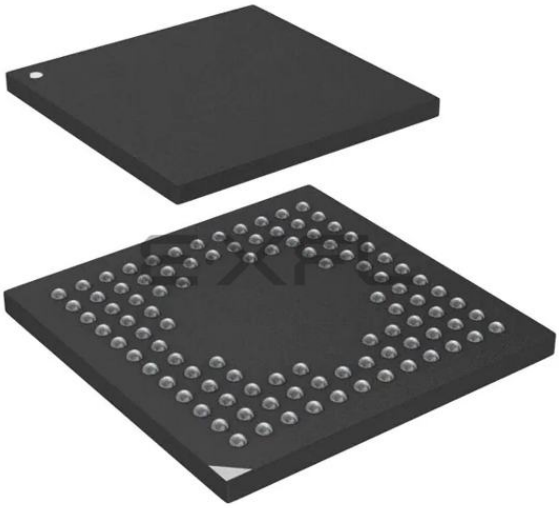

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l431vci6

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32L431xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32L431xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

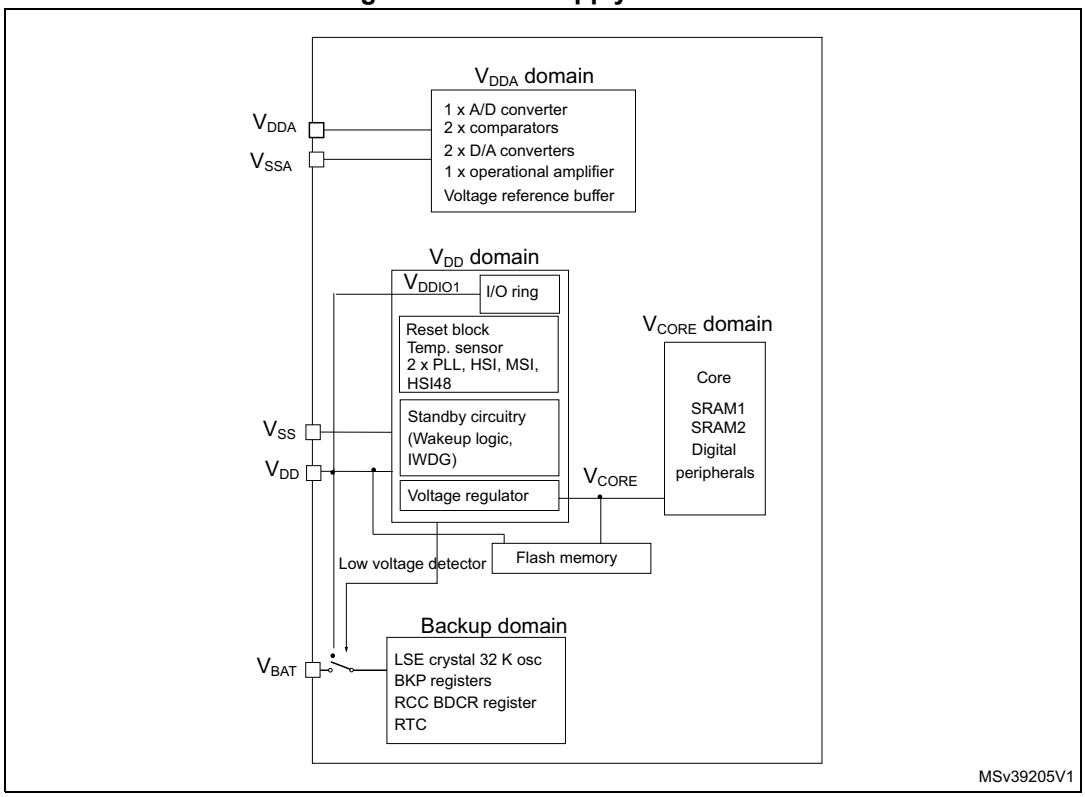
3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

Figure 2. Power supply overview



3.9.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a Peripheral Voltage Monitor which compares the independent supply voltage V_{DDA} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
  - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes (except VBAT).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 80 MHz.

3.15 Analog to digital converter (ADC)

The device embeds a successive approximation analog-to-digital converter with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 16 external channels.
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs.
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - ADC supports multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.15.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.17 Voltage reference buffer (VREFBUF)

The STM32L431xx devices embed an voltage reference buffer which can be used as voltage reference for ADCs, DACs and also as voltage reference for external components through the VREF+ pin.

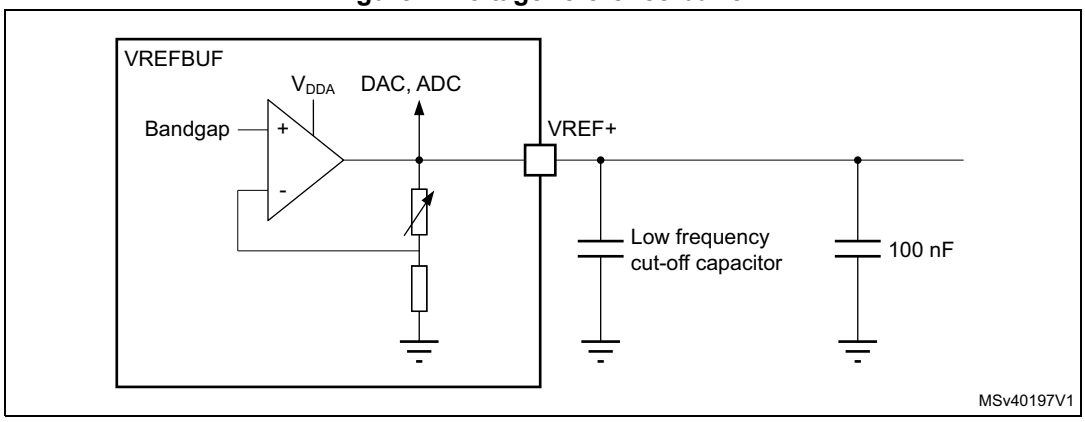
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 4. Voltage reference buffer



3.18 Comparators (COMP)

The STM32L431xx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.22 Timers and watchdogs

The STM32L431xx includes one advanced control timers, up to five general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 9. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.22.1 Advanced-control timer (TIM1)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.22.2*) using the same architecture, so the advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.25 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L431xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1, USART2 and USART3 also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3) to wake up the MCU from Stop mode using baudrates up to 200 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 11. STM32L431xx USART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	LPUART1
Hardware flow control for modem	X	X	X	X
Continuous communication using DMA	X	X	X	X
Multiprocessor communication	X	X	X	X
Synchronous mode	X	X	X	-
Smartcard mode	X	X	X	-
Single-wire half-duplex communication	X	X	X	X
IrDA SIR ENDEC block	X	X	X	-
LIN mode	X	X	X	-
Dual clock domain	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	X
Receiver timeout interrupt	X	X	X	-
Modbus communication	X	X	X	-
Auto baud rate detection	X (4 modes)			-
Driver Enable	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits			

1. X = supported.

Table 14. STM32L431xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
UFQFPN32	LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
14	18	18	G5	F4	26	F5	35	M5	PB0	I/O	FT_a	-	TIM1_CH2N, SPI1_NSS, USART3_CK, QUADSPI_BK1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	ADC1_IN15
15	19	19	G4	H5	27	G5	36	M6	PB1	I/O	FT_a	-	TIM1_CH3N, USART3_RTS_DE, LPUART1_RTS_DE, QUADSPI_BK1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC1_IN16
-	20	20	G3	G4	28	G6	37	L6	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, EVENTOUT	COMP1_INP
-	-	-	-	-	-	-	38	M7	PE7	I/O	FT	-	TIM1_ETR, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	-	-	39	L7	PE8	I/O	FT	-	TIM1_CH1N, SAI1_SCK_B, EVENTOUT	-
-	-	-	-	-	-	-	40	M8	PE9	I/O	FT	-	TIM1_CH1, SAI1_FS_B, EVENTOUT	-
-	-	-	-	-	-	-	41	L8	PE10	I/O	FT	-	TIM1_CH2N, TSC_G5_IO1, QUADSPI_CLK, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	-	42	M9	PE11	I/O	FT	-	TIM1_CH2, TSC_G5_IO2, QUADSPI_BK1_NCS, EVENTOUT	-
-	-	-	-	-	-	-	43	L9	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, TSC_G5_IO3, QUADSPI_BK1_IO0, EVENTOUT	-
-	-	-	-	-	-	-	44	M10	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, TSC_G5_IO4, QUADSPI_BK1_IO1, EVENTOUT	-
-	-	-	-	-	-	-	45	M11	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, EVENTOUT	-

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA})+3.6 V and 5.5V.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.10: Thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.10: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 22* are derived from tests performed under the ambient temperature condition summarized in *Table 21*.

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		10	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature conditions summarized in *Table 21: General operating conditions*.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	

Table 33. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (wakeup from Stop2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1. See (3).	3 V	1.85	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See (3).	3 V	1.52	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI16 = 16 MHz, voltage Range 1. See (3).	3 V	1.54	-	-	-	-	-	-	-	-	-	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 40: Low-power mode wakeup timings*.

Table 35. Current consumption in Stop 0

Symbol	Parameter	Conditions	TYP					MAX(1)					Unit
		V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (Stop 0)	Supply current in Stop 0 mode, RTC disabled	1.8 V	108	119	158	221	347	133	158	244	395	704	µA
		2.4 V	110	121	160	223	349	136	161	248	399	710	
		3 V	111	123	161	224	352	139	164	251	403	716	
		3.6 V	114	125	163	227	355	142	167	254	408	722(2)	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 39*. The MCU is placed under the following conditions:

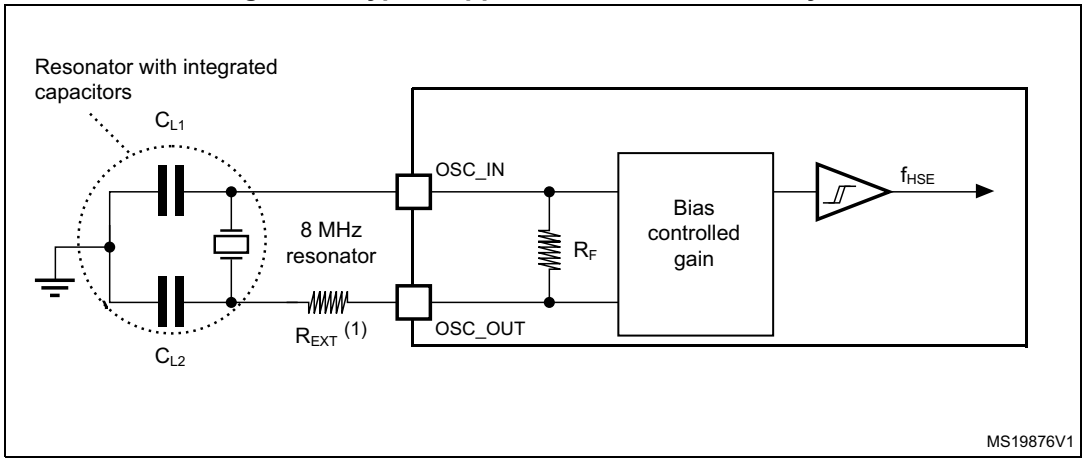
- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 18: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 39*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 39. Peripheral current consumption

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix(1)	3.2	2.9	3.1	µA/MHz
	ADC independent clock domain	0.4	0.1	0.2	
	ADC clock domain	2.1	1.9	1.9	
	CRC	0.4	0.2	0.3	
	DMA1	1.4	1.3	1.4	
	DMA2	1.5	1.3	1.4	
	FLASH	6.2	5.2	5.8	
	GPIOA(2)	1.7	1.4	1.6	
	GPIOB(2))	1.6	1.3	1.6	
	GPIOC(2)	1.7	1.5	1.6	
	GPIOD(2)	1.8	1.6	1.7	
	GPIOE(2)	1.7	1.6	1.6	
	GPIOH(2)	0.6	0.6	0.5	
	QSPI	7.0	5.8	7.3	
	RNG independent clock domain	2.2	NA	NA	
	RNG clock domain	0.5	NA	NA	
	SRAM1	0.8	0.9	0.7	
	SRAM2	1.0	0.8	0.8	
	TSC	1.6	1.3	1.3	
	All AHB Peripherals	25.2	21.7	23.6	
APB1	AHB to APB1 bridge(3)	0.9	0.7	0.9	
	CAN1	4.1	3.2	3.9	
	DAC1	2.4	1.8	2.2	

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 22. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 46*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 46. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

Table 64. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 80 MHz	0.03125	-	8.00625	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	0.1875	-	8.1625	µs
		Resolution = 12 bits	ts + 12.5 cycles for successive approximation = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 5 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	-	260	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 65. Maximum ADC RAIN(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	RAIN max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000

Table 72. VREFBUF characteristics(1) (continued)

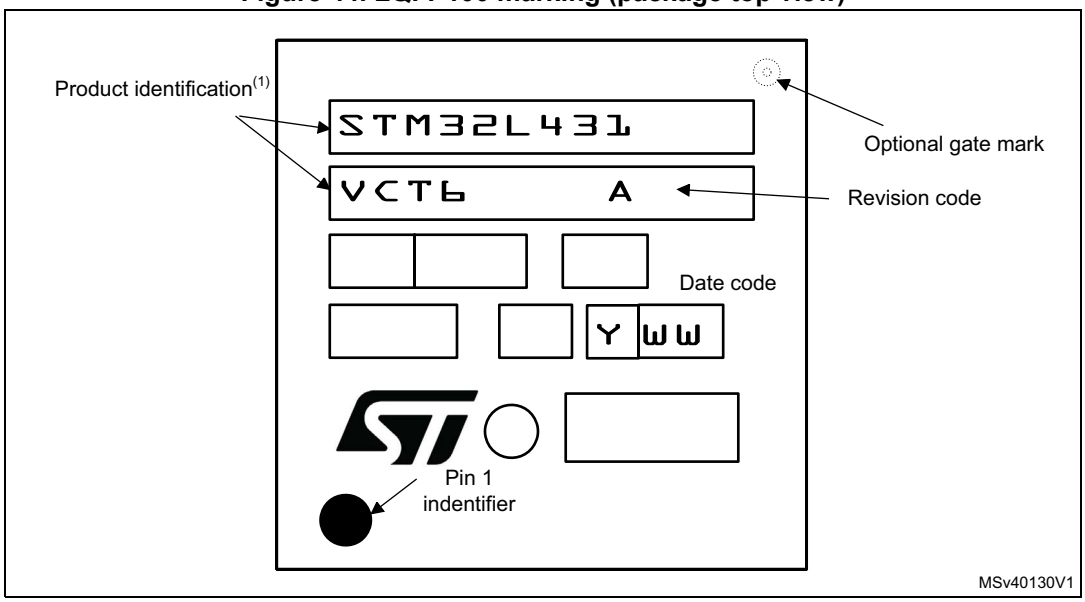
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

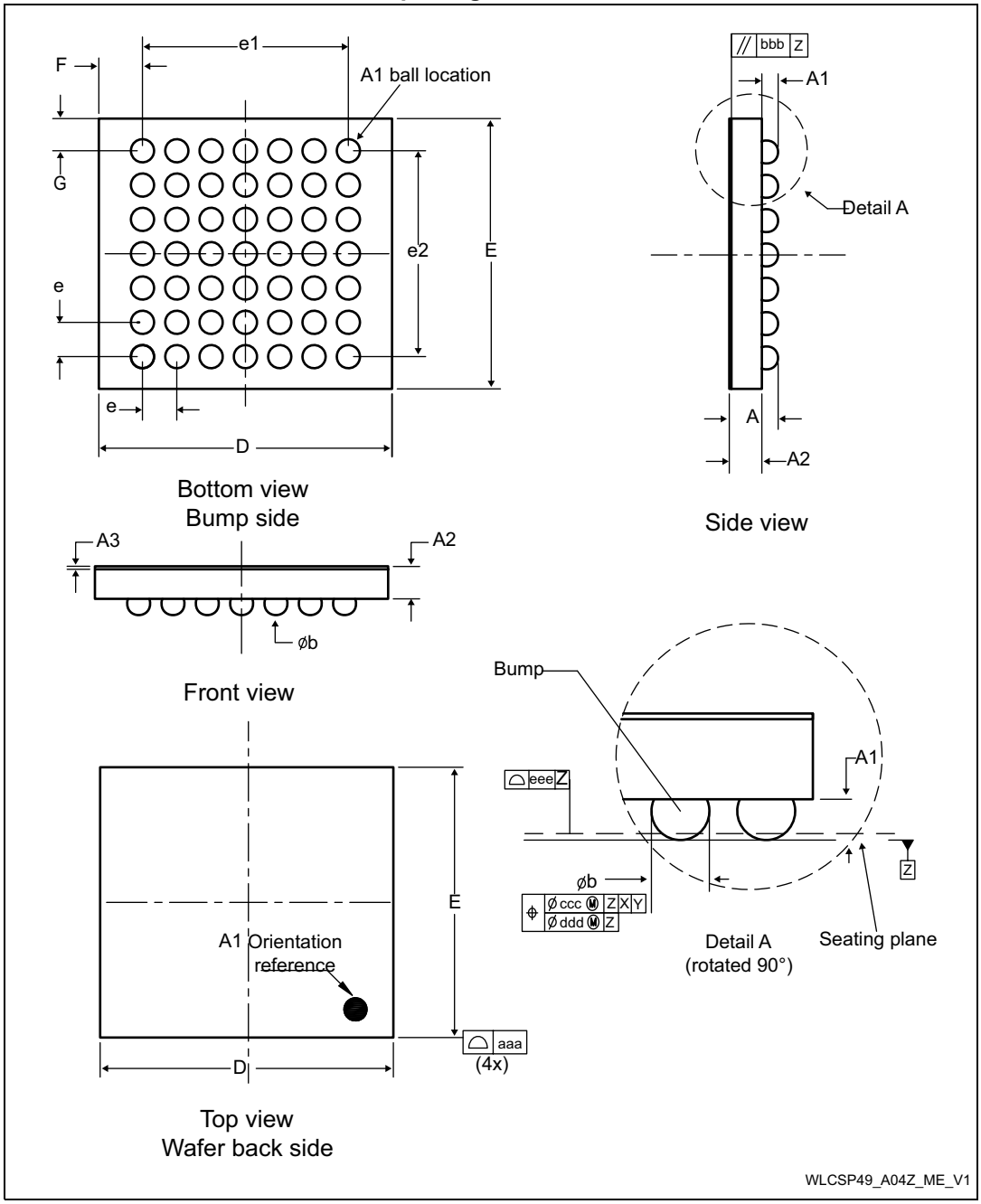
Figure 44. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.6 WLCSP49 package information

Figure 57. WLCSP49 - 49-ball, 3.141 x 3.127 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

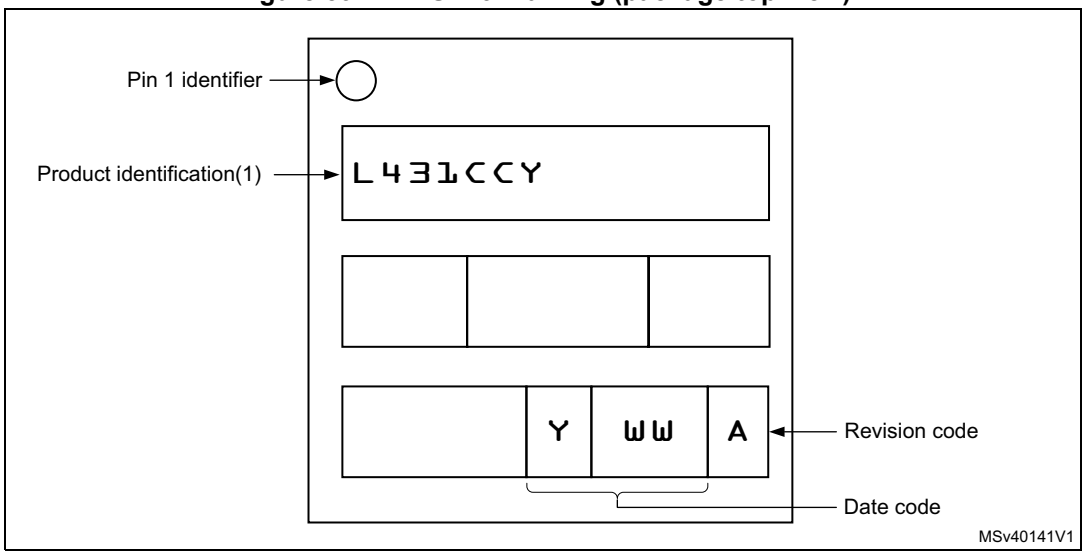
Table 98. WLCSP49 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 59. WLCSP49 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

9 Revision history

Table 104. Document revision history

Date	Revision	Changes
31-May-2016	1	Initial release.