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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p80c51fa-4a-512

80C51 8-bit microcontroller family
8K–64K/256–1K OTP/ROM/ROMless, low voltage (2.7V–5.5V),
low power, high speed (33 MHz)

8XC54/58
8XC51FA/FB/FC/80C51FA
8XC51RA+/RB+/RC+/RD+/80C51RA+

DESCRIPTION

Three different Single-Chip 8-Bit Microcontroller families are presented in this datasheet:

- 8XC54/8XC58
- 80C51FA/8XC51FA/8XC51FB/8XC51FC
- 80C51RA+/8XC51RA+/8XC51RB+/8XC51RC+/8XC51RD+

For applications requiring 4K ROM/EPROM, see the 8XC51/80C31 8-bit CMOS (low voltage, low power, and high speed) microcontroller families datasheet.

All the families are Single-Chip 8-Bit Microcontrollers manufactured in advanced CMOS process and are derivatives of the 80C51 microcontroller family. All the devices have the same instruction set as the 80C51.

These devices provide architectural enhancements that make them applicable in a variety of applications for general control systems.

ROM/EPROM Memory Size (X by 8)	RAM Size (X by 8)	Programmable Timer Counter (PCA)	Hardware Watch Dog Timer
80C31/8XC51			
0K/4K	128	No	No
8XC54/58			
0K/8K/16K/32K	256	No	No
80C51FA/8XC51FA/FB/FC			
0K/8K/16K/32K	256	Yes	No
80C51RA+/8XC51RA+/RB+/RC+			
0K/8K/16K/32K	512	Yes	Yes
8XC51RD+			
64K	1024	Yes	Yes

The ROMless devices, 80C51FA, and 80C51RA+ can address up to 64K of external memory. All the devices have four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra memory capability up to 64k bytes, each can be expanded using standard TTL-compatible memories and logic.

Its added features make it an even more powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multiprocessor communications.

FEATURES

- 80C51 Central Processing Unit
- Speed up to 33 MHz
- Full static operation
- Operating voltage range: 2.7 V to 5.5 V @ 16 MHz
- Security bits:
 - ROM – 2 bits
 - OTP–EPROM – 3 bits
- Encryption array – 64 bytes
- RAM expandable to 64K bytes
- 4 level priority interrupt
- 6 or 7 interrupt sources, depending on device
- Four 8-bit I/O ports
- Full-duplex enhanced UART
 - Framing error detection
 - Automatic address recognition
- Power control modes
 - Clock can be stopped and resumed
 - Idle mode
 - Power down mode
- Programmable clock out
- Second DPTR register
- Asynchronous port reset
- Low EMI (inhibit ALE)

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PIN DESCRIPTIONS (Continued)

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
$\overline{\text{PSEN}}$	29	32	26	O	Program Store Enable: The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/\text{V}_{\text{PP}}$	31	35	29	I	External Access Enable/Programming Supply Voltage: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations starting with 0000H. If $\overline{\text{EA}}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 8k Devices (1FFFFH), 16k Devices (3FFFFH) or 32k Devices (7FFFFH). Since the RD+ has 64k Internal Memory, the RD+ will execute only from internal memory when $\overline{\text{EA}}$ is held high. This pin also receives the 12.75 V programming supply voltage (V_{PP}) during EPROM programming. If security bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier.

NOTE:

To avoid “latch-up” effect at power-on, the voltage on any pin at any time must not be higher than $\text{V}_{\text{CC}} + 0.5 \text{ V}$ or $\text{V}_{\text{SS}} - 0.5 \text{ V}$, respectively.

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8XC51FA/58

8XC51FA/58

8XC51RA+/RB+/RC+/RD+/80C51RA+

87C51RA+/RB+/RC+/RD+ AND 80C51RA+ ORDERING INFORMATION

	MEMORY SIZE 8K × 8	MEMORY SIZE 16K × 8	MEMORY SIZE 32K × 8	MEMORY SIZE 64K × 8	ROMless	TEMPERATURE RANGE °C AND PACKAGE	VOLTAGE RANGE	FREQ. (MHz)	DWG. #
ROM	P83C51RA+4N	P83C51RB+4N	P83C51RC+4N	P83C51RD+4N	P80C51RA+4N	0 to +70, 40-Pin Plastic Dual In-line Pkg.	2.7V to 5.5V	0 to 16	SOT129-1
OTP	P87C51RA+4N	P87C51RB+4N	P87C51RC+4N	P87C51RD+4N					
ROM	P83C51RA+4A	P83C51RB+4A	P83C51RC+4A	P83C51RD+4A	P80C51RA+4A	0 to +70, 44-Pin Plastic Leaded Chip Carrier	2.7V to 5.5V	0 to 16	SOT187-2
OTP	P87C51RA+4A	P87C51RB+4A	P87C51RC+4A	P87C51RD+4A					
ROM	P83C51RA+4B	P83C51RB+4B	P83C51RC+4B	P83C51RD+4B	P80C51RA+4B	0 to +70, 44-Pin Plastic Quad Flat Pack	2.7V to 5.5V	0 to 16	SOT307-2
OTP	P87C51RA+4B	P87C51RB+4B	P87C51RC+4B	P87C51RD+4B					
ROM	P83C51RA+5N	P83C51RB+5N	P83C51RC+5N	P83C51RD+5N	P80C51RA+5N	–40 to +85, 40-Pin Plastic Dual In-line Pkg.	2.7V to 5.5V	0 to 16	SOT129-1
OTP	P87C51RA+5N	P87C51RB+5N	P87C51RC+5N	P87C51RD+5N					
ROM	P83C51RA+5A	P83C51RB+5A	P83C51RC+5A	P83C51RD+5A	P80C51RA+5A	–40 to +85, 44-Pin Plastic Leaded Chip Carrier	2.7V to 5.5V	0 to 16	SOT187-2
OTP	P87C51RA+5A	P87C51RB+5A	P87C51RC+5A	P87C51RD+5A					
ROM	P83C51RA+5B	P83C51RB+5B	P83C51RC+5B	P83C51RD+5B	P80C51RA+5B	–40 to +85, 44-Pin Plastic Quad Flat Pack	2.7V to 5.5V	0 to 16	SOT307-2
OTP	P87C51RA+5B	P87C51RB+5B	P87C51RC+5B	P87C51RD+5B					
ROM	P83C51RA+IN	P83C51RB+IN	P83C51RC+IN	P83C51RD+IN	P80C51RA+IN	0 to +70, 40-Pin Plastic Dual In-line Pkg.	5V	0 to 33	SOT129-1
OTP	P87C51RA+IN	P87C51RB+IN	P87C51RC+IN	P87C51RD+IN					
ROM	P83C51RA+IA	P83C51RB+IA	P83C51RC+IA	P83C51RD+IA	P80C51RA+IA	0 to +70, 44-Pin Plastic Leaded Chip Carrier	5V	0 to 33	SOT187-2
OTP	P87C51RA+IA	P87C51RB+IA	P87C51RC+IA	P87C51RD+IA					
ROM	P83C51RA+IB	P83C51RB+IB	P83C51RC+IB	P83C51RD+IB	P80C51RA+IB	0 to +70, 44-Pin Plastic Quad Flat Pack	5V	0 to 33	SOT307-2
OTP	P87C51RA+IB	P87C51RB+IB	P87C51RC+IB	P87C51RD+IB					
ROM	P83C51RA+JN	P83C51RB+JN	P83C51RC+JN	P83C51RD+JN	P80C51RA+JN	–40 to +85, 40-Pin Plastic Dual In-line Pkg.	5V	0 to 33	SOT129-1
OTP	P87C51RA+JN	P87C51RB+JN	P87C51RC+JN	P87C51RD+JN					
ROM	P83C51RA+JA	P83C51RB+JA	P83C51RC+JA	P83C51RD+JA	P80C51RA+JA	–40 to +85, 44-Pin Plastic Leaded Chip Carrier	5V	0 to 33	SOT187-2
OTP	P87C51RA+JA	P87C51RB+JA	P87C51RC+JA	P87C51RD+JA					
ROM	P83C51RA+JB	P83C51RB+JB	P83C51RC+JB	P83C51RD+JB	P80C51RA+JB	–40 to +85, 44-Pin Plastic Quad Flat Pack	5V	0 to 33	SOT307-2
OTP	P87C51RA+JB	P87C51RB+JB	P87C51RC+JB	P87C51RD+JB					

Note: For Multi Time Programmable devices, See P89C51RX+ Flash datasheet.

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 8XC51RA+/RB+/RC+/RD+/80C51RA+

Table 1. 8XC54/58 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB				LSB				
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	—	—	—	—	—	—	—	AO	xxxxxxx0B
AUXR1#	Auxiliary 1	A2H	—	—	—	LPEP ³	GF3	0	—	DPS	xxx0xxx0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR: DPH DPL	Data Pointer (2 bytes) Data Pointer High Data Pointer Low	83H 82H									00H 00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable	A8H	EA	—	ET2	ES	ET1	EX1	ET0	EX0	0x000000B
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt Priority	B8H	—	—	PT2	PS	PT1	PX1	PT0	PX0	xx000000B
			B7	B6	B5	B4	B3	B2	B1	B0	
IPH#	Interrupt Priority High	B7H	—	—	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	xx000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	—	—	—	—	—	—	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	RD	WR	T1	T0	INT1	INT0	TxD	RxD	FFH
PCON# ¹	Power Control	87H	SMOD1	SMOD0	—	POF ²	GF1	GF0	PD	IDL	00xx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	—	P	000000x0B
RCAP2H#	Timer 2 Capture High	CBH									00H
RCAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00H
T2MOD#	Timer 2 Mode Control	C9H	—	—	—	—	—	—	T2OE	DCEN	xxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH	00H								
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H

* SFRs are bit addressable.

SFRs are modified from or added to the 80C51 SFRs.

– Reserved bits.

1. Reset value depends on reset source.

2. Bit will not be affected by Reset.

3. LPEP – Low Power OTP–EPROM only operation.

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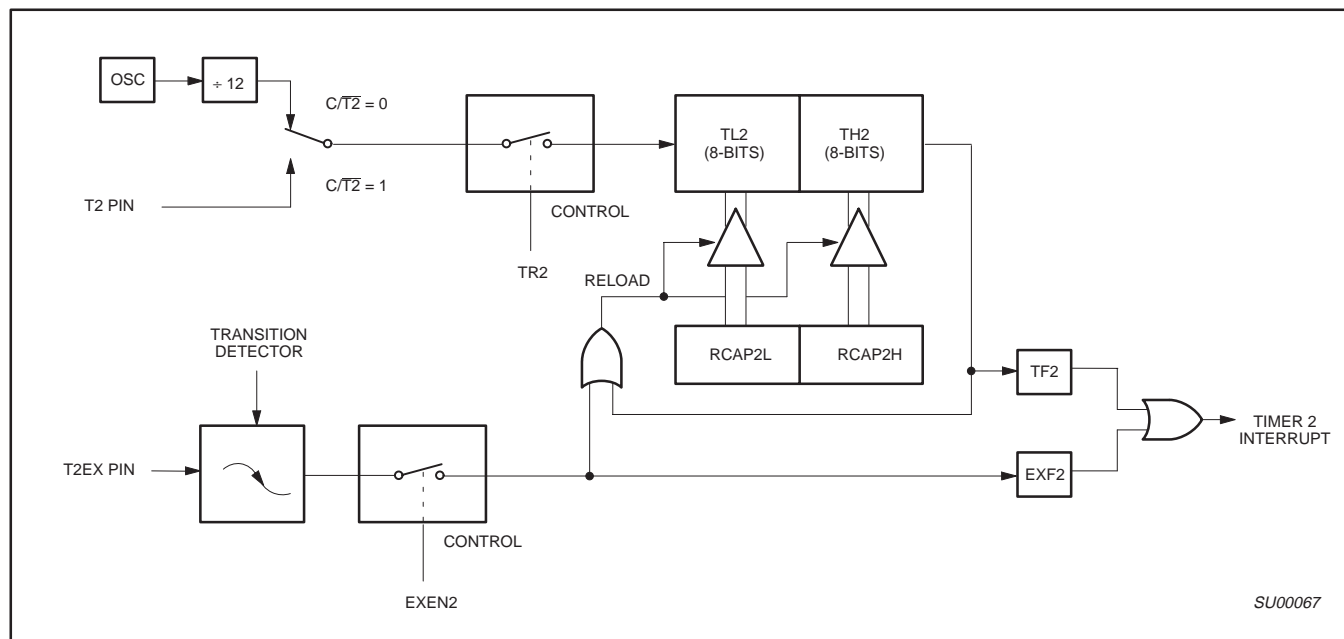


Figure 4. Timer 2 in Auto-Reload Mode (DCEN = 0)

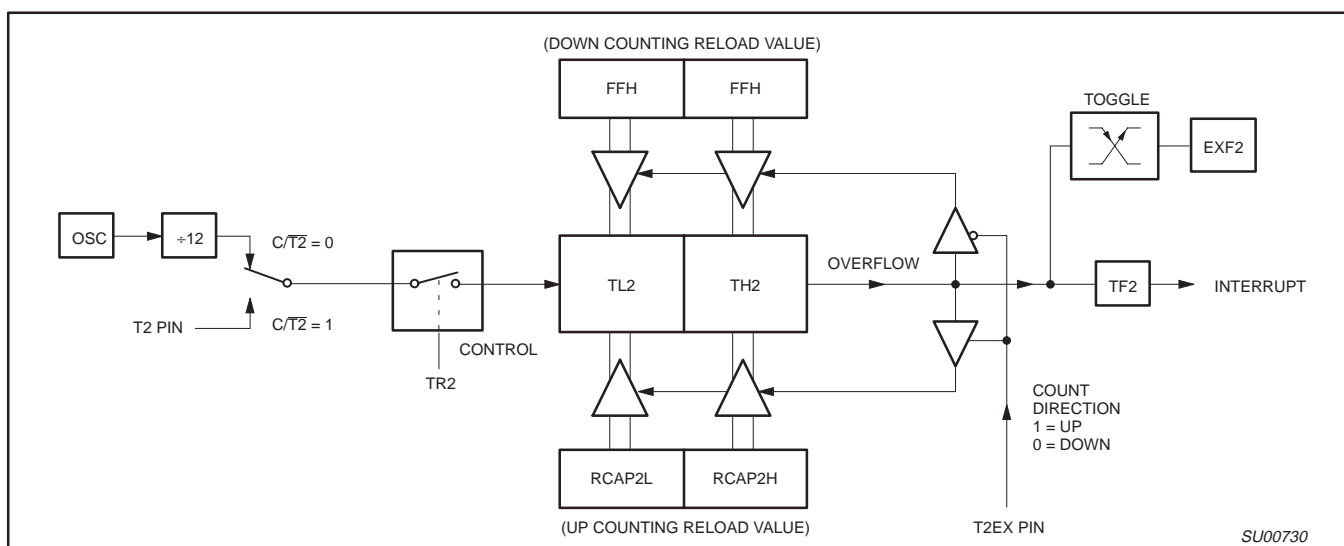


Figure 5. Timer 2 Auto Reload Mode (DCEN = 1)

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Enhanced UART

The UART operates in all of the usual modes that are described in the first section of *Data Handbook IC20, 80C51-Based 8-Bit Microcontrollers*. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 7). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 8.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 9.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR =	1100 0000
	SADEN =	1111 1101
	Given =	1100 00X0

Slave 1	SADDR =	1100 0000
	SADEN =	1111 1110
	Given =	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR =	1100 0000
	SADEN =	1111 1001
	Given =	1100 0XX0
Slave 1	SADDR =	1110 0000
	SADEN =	1111 1010
	Given =	1110 0XX0
Slave 2	SADDR =	1110 0000
	SADEN =	1111 1100
	Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

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		7	6	5	4	3	2	1	0
IP (0B8H)		—	PPC	PT2	PS	PT1	PX1	PT0	PX0
		Priority Bit = 1 assigns high priority Priority Bit = 0 assigns low priority							
BIT	SYMBOL	FUNCTION							
IP.7	—	Not implemented, reserved for future use.							
IP.6	PPC	PCA interrupt priority bit for FX and RX+ only, otherwise it is not implemented.							
IP.5	PT2	Timer 2 interrupt priority bit.							
IP.4	PS	Serial Port interrupt priority bit.							
IP.3	PT1	Timer 1 interrupt priority bit.							
IP.2	PX1	External interrupt 1 priority bit.							
IP.1	PT0	Timer 0 interrupt priority bit.							
IP.0	PX0	External interrupt 0 priority bit.							

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Figure 11. IP Registers

		7	6	5	4	3	2	1	0
IPH (B7H)		—	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Priority Bit = 1 assigns higher priority Priority Bit = 0 assigns lower priority							
BIT	SYMBOL	FUNCTION							
IPH.7	—	Not implemented, reserved for future use.							
IPH.6	PPCH	PCA interrupt priority bit high for FX and RX+ only, otherwise it is not implemented.							
IPH.5	PT2H	Timer 2 interrupt priority bit high.							
IPH.4	PSH	Serial Port interrupt priority bit high.							
IPH.3	PT1H	Timer 1 interrupt priority bit high.							
IPH.2	PX1H	External interrupt 1 priority bit high.							
IPH.1	PT0H	Timer 0 interrupt priority bit high.							
IPH.0	PX0H	External interrupt 0 priority bit high.							

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Figure 12. IPH Registers

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8XC51RA+/RB+/RC+/RD+/80C51RA+

(8XC51FX and 8XC51RX+ ONLY)

Programmable Counter Array (PCA) (8XC51FX and 8XC51RX+ only)

The Programmable Counter Array available on the 8XC51FX and 8XC51RX+ is a special 16-bit Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3(CEX0), module 1 to P1.4(CEX1), etc. The basic PCA configuration is shown in Figure 14.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/12 the oscillator frequency, 1/4 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 17):

CPS1	CPS0	PCA Timer Count Source
0	0	1/12 oscillator frequency
0	1	1/4 oscillator frequency
1	0	Timer 0 overflow
1	1	External Input at ECI pin

In the CMOD SFR are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows. These functions are shown in Figure 15.

The watchdog timer function is implemented in module 4 (see Figure 24).

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (refer to Figure 18). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the

ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software. The PCA interrupt system shown in Figure 16.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 19). The registers contain the bits that control the mode that each module will operate in. The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function. Figure 20 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

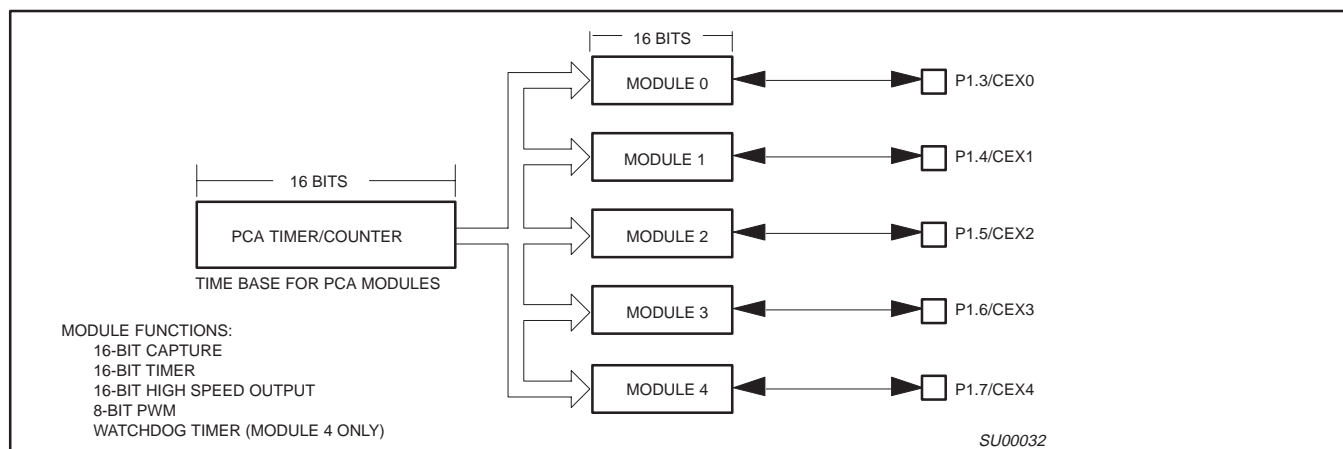


Figure 14. Programmable Counter Array (PCA)

80C51 8-bit microcontroller family
8K–64K/256–1K OTP/ROM/ROMless, low voltage (2.7V–5.5V),
low power, high speed (33MHz)

8XC54/58
8XC51FA/FB/FC/80C51FA
8XC51RA+/RB+/RC+/RD+/80C51RA+

(8XC51FX and 8XC51RX+ ONLY)

CMOD Address = 0D9H

Reset Value = 00XX X000B

	CIDL	WDTE	–	–	–	CPS1	CPS0	ECF
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.
–	Not implemented, reserved for future use.*
CPS1	PCA Count Pulse Select bit 1.
CPS0	PCA Count Pulse Select bit 0.
CPS1	CPS0
0	0
0	1
1	0
1	1
ECF	

Selected PCA Input**

0 Internal clock, $f_{OSC} \div 12$

1 Internal clock, $f_{OSC} \div 4$

2 Timer 0 overflow

3 External clock at ECI/P1.2 pin (max. rate = $f_{OSC} \div 8$)

PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.

NOTE:

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

** f_{OSC} = oscillator frequency

SU00035

SU00035

Figure 17. CMOD: PCA Counter Mode Register

CCON Address = 0D8H

Reset Value = 00X0 0000B

Bit Addressable

	CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
–	Not implemented, reserved for future use*.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

NOTE:

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

SU00036

SU00036

Figure 18. CCON: PCA Counter Control Register

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8XC54/58
8XC51FA/FB/FC/80C51FA
8XC51RA+/RB+/RC+/RD+/80C51RA+

(8XC51FX and 8XC51RX+ ONLY)

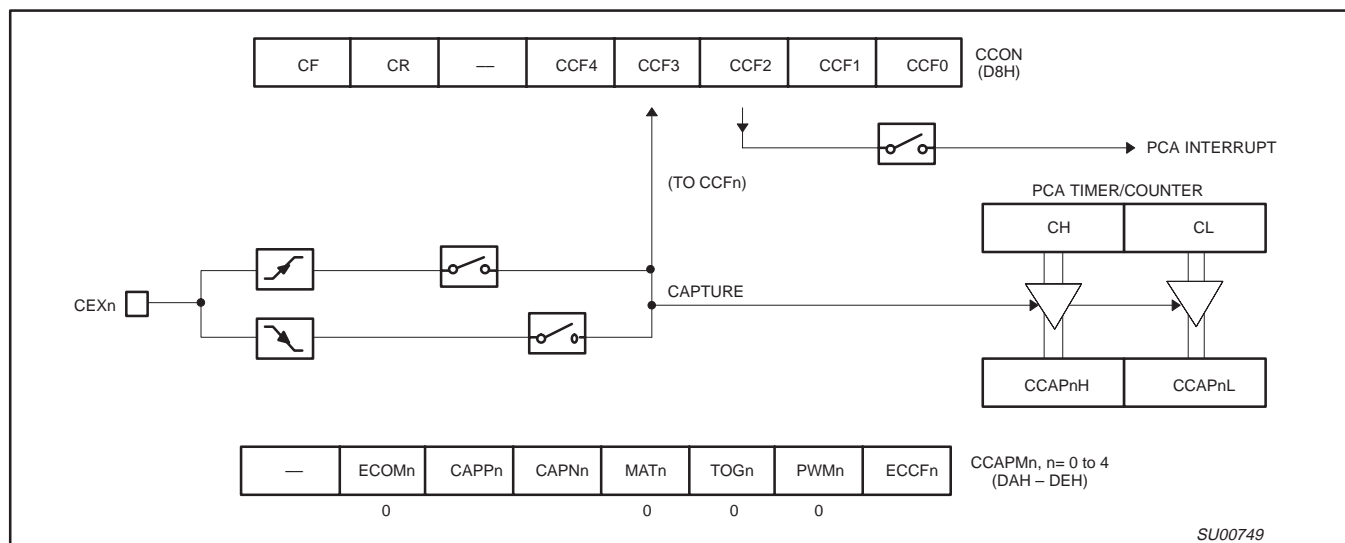


Figure 21. PCA Capture Mode

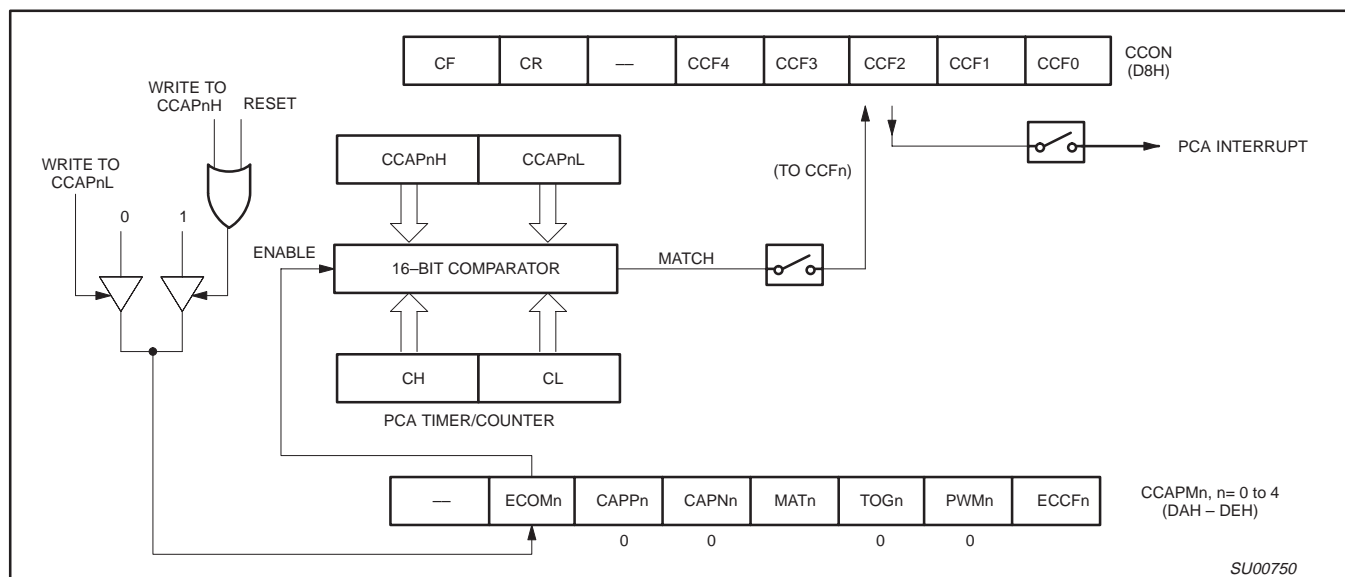


Figure 22. PCA Compare Mode

80C51 8-bit microcontroller family
8K–64K/256–1K OTP/ROM/ROMless, low voltage (2.7V–5.5V),
low power, high speed (33MHz)

8XC54/58
8XC51FA/FB/FC/80C51FA
8XC51RA+/RB+/RC+/RD+/80C51RA+

(8XC51FX and 8XC51RX+ ONLY)

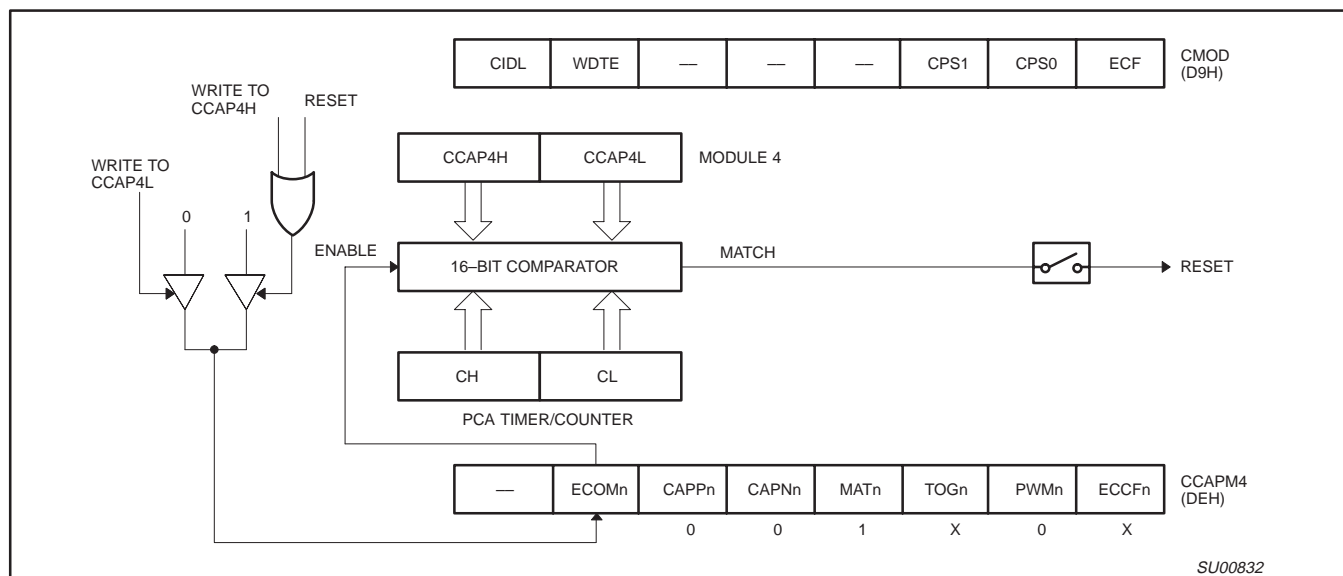


Figure 25. PCA Watchdog Timer m(Module 4 only)

PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed.

Figure 25 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare values, or
3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for **all** modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

Figure 26 shows the code for initializing the watchdog timer. Module 4 can be configured in either compare mode, and the WDTE bit in CMOD must also be set. The user's software then must periodically change (CCAP4H,CCAP4L) to keep a match from occurring with the PCA timer (CH,CL). This code is given in the WATCHDOG routine in Figure 26.

This routine should not be part of an interrupt service routine, because if the program counter goes astray and gets stuck in an infinite loop, interrupts will still be serviced and the watchdog will keep getting reset. Thus, the purpose of the watchdog would be defeated. Instead, call this subroutine from the main program within 2^{16} count of the PCA timer.

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8XC54/58
8XC51FA/FB/FC/80C51FA
8XC51RA+/RB+/RC+/RD+/80C51RA+

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 5.5V , $V_{SS} = 0\text{V}$ (16MHz devices)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage	$4.0\text{V} < V_{CC} < 5.5\text{V}$	-0.5		$0.2V_{CC}-0.1$	V
		$2.7\text{V} < V_{CC} < 4.0\text{V}$	-0.5		0.7	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{\text{EA}}$)		$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$		$V_{CC}+0.5$	V
V_{OL}	Output low voltage, ports 1, 2 ⁸	$V_{CC} = 2.7\text{V}$ $I_{OL} = 1.6\text{mA}^2$			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{\text{PSEN}}$ ^{8, 7}	$V_{CC} = 2.7\text{V}$ $I_{OL} = 3.2\text{mA}^2$			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 2.7\text{V}$ $I_{OH} = -20\mu\text{A}$	$V_{CC} - 0.7$			V
		$V_{CC} = 4.5\text{V}$ $I_{OH} = -30\mu\text{A}$	$V_{CC} - 0.7$			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , $\overline{\text{PSEN}}$ ³	$V_{CC} = 2.7\text{V}$ $I_{OH} = -3.2\text{mA}$	$V_{CC} - 0.7$			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{V}$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0\text{V}$ See note 4			-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$			± 10	μA
I_{CC}	Power supply current (see Figure 36): Active mode @ 16MHz (all except 8XC51RD+) 87C51RD+ Idle mode @ 16MHz Power-down mode or clock stopped (see Figure 40 for conditions)	See note 5 $T_{amb} = 0^{\circ}\text{C}$ to 70°C $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		3	15	mA
					16	mA
					4	mA
					50	μA
					75	μA
R_{RST}	Internal reset pull-down resistor		40		225	$\text{k}\Omega$
C_{IO}	Pin capacitance ¹⁰ (except $\overline{\text{EA}}$)				15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading $> 100\text{pF}$), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{\text{PSEN}}$ to momentarily fall below the $V_{CC}-0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
- See Figures 37 through 40 for I_{CC} test conditions, and Figure 36 for I_{CC} vs Freq.
Active mode: $I_{CC} = (0.9 \times \text{FREQ.} + 1.1)\text{mA}$ for all devices except 8XC51RD+; 8XC51RD+ $I_{CC} = (0.9 \times \text{Freq} + 2.1)\text{mA}$
Idle mode: $I_{CC} = (0.18 \times \text{FREQ.} + 1.01)\text{mA}$
- This value applies to $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$. For $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $I_{TL} = -750\mu\text{A}$.
- Load capacitance for port 0, ALE, and $\overline{\text{PSEN}} = 100\text{pF}$, load capacitance for all other outputs = 80pF .
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15mA (*NOTE: This is 85°C specification.)
Maximum I_{OL} per 8-bit port: 26mA
Maximum total I_{OL} for all outputs: 71mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except $\overline{\text{EA}}$ is 25pF).

80C51 8-bit microcontroller family
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8XC54/58
8XC51FA/FB/FC/80C51FA
8XC51RA+/RB+/RC+/RD+/80C51RA+

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$, 33MHz devices; $5V \pm 10\%$; $V_{SS} = 0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage	$4.5V < V_{CC} < 5.5V$	-0.5		$0.2V_{CC}-0.1$	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, \overline{EA})		$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$		$V_{CC}+0.5$	V
V_{OL}	Output low voltage, ports 1, 2, 3 ⁸	$V_{CC} = 4.5V$ $I_{OL} = 1.6mA^2$			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, \overline{PSEN} ^{7, 8}	$V_{CC} = 4.5V$ $I_{OL} = 3.2mA^2$			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 4.5V$ $I_{OH} = -30\mu A$	$V_{CC} - 0.7$			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , \overline{PSEN} ³	$V_{CC} = 4.5V$ $I_{OH} = -3.2mA$	$V_{CC} - 0.7$			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4V$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0V$ See note 4			-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$			± 10	μA
I_{CC}	Power supply current (see Figure 36): Active mode (see Note 5) Idle mode (see Note 5) Power-down mode or clock stopped (see Figure 40 for conditions)	See note 5 $T_{amb} = 0^{\circ}\text{C}$ to 70°C $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		3	50 75	μA μA
R_{RST}	Internal reset pull-down resistor		40		225	k Ω
C_{IO}	Pin capacitance ¹⁰ (except \overline{EA})				15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading $> 100pF$), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and \overline{PSEN} to momentarily fall below the $V_{CC}-0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
- See Figures 37 through 40 for I_{CC} test conditions and Figure 36 for I_{CC} vs Freq.
Active mode: $I_{CC(MAX)} = (0.9 \times \text{FREQ.} + 1.1)mA$, for all devices except 8XC51RD+; 8XC51RD+ $I_{CC} = (0.9 \times \text{Freq} + 2.1) mA$
Idle mode: $I_{CC(MAX)} = (0.18 \times \text{FREQ.} + 1.0)mA$
- This value applies to $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$. For $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $I_{TL} = -750\mu A$.
- Load capacitance for port 0, ALE, and $\overline{PSEN} = 100pF$, load capacitance for all other outputs = 80pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15mA (*NOTE: This is 85°C specification.)
Maximum I_{OL} per 8-bit port: 26mA
Maximum total I_{OL} for all outputs: 71mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except \overline{EA} is 25pF).

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8XC51FA/FB/FC/80C51FA
8XC51RA+/RB+/RC+/RD+/80C51RA+

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE

P – $\overline{\text{PSEN}}$
Q – Output data
R – $\overline{\text{RD}}$ signal
t – Time
V – Valid
W – $\overline{\text{WR}}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
 t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.

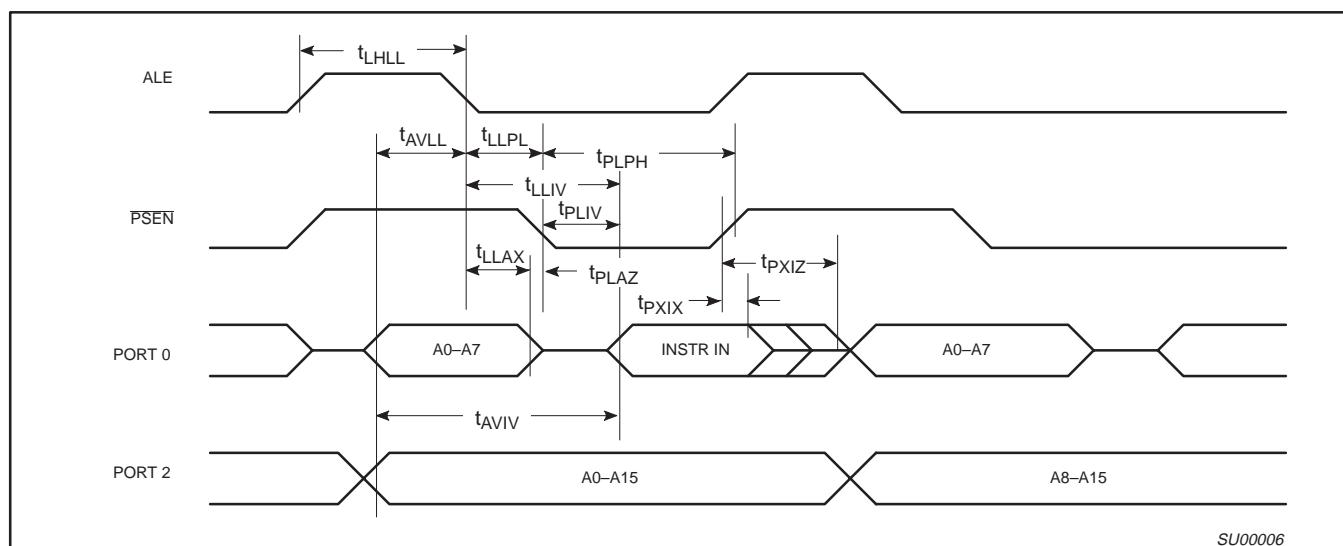


Figure 29. External Program Memory Read Cycle

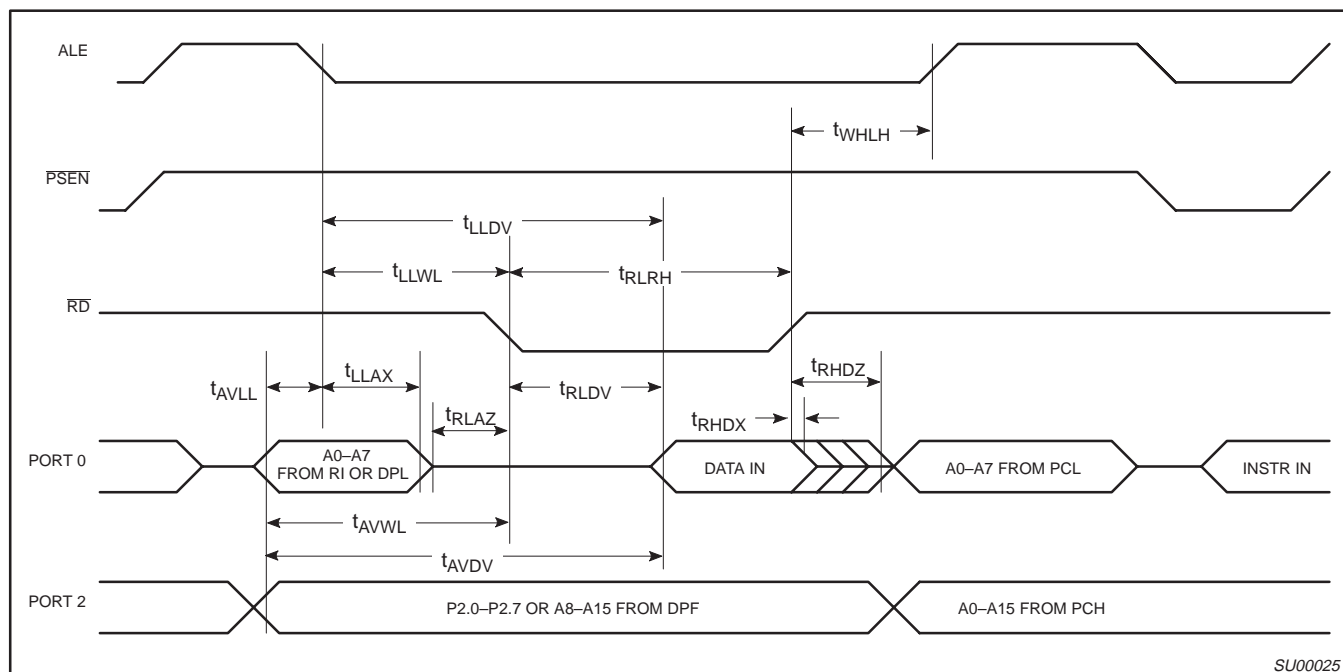


Figure 30. External Data Memory Read Cycle

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8XC51RA+/RB+/RC+/RD+/80C51RA+

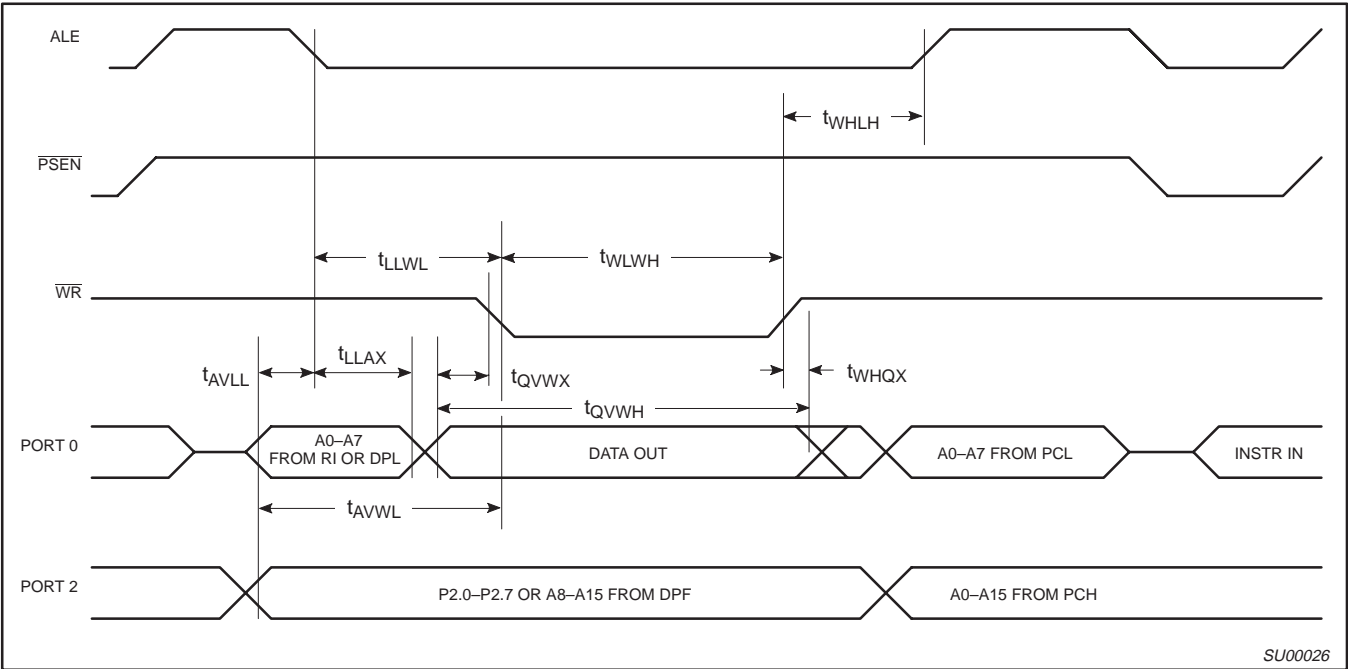


Figure 31. External Data Memory Write Cycle

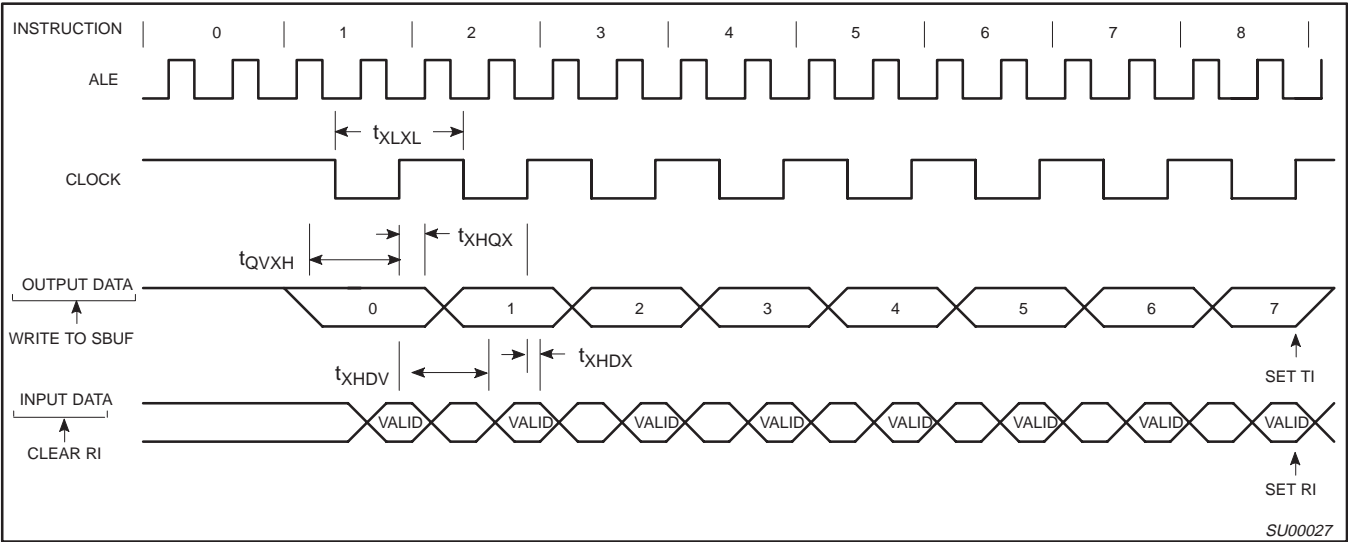


Figure 32. Shift Register Mode Timing

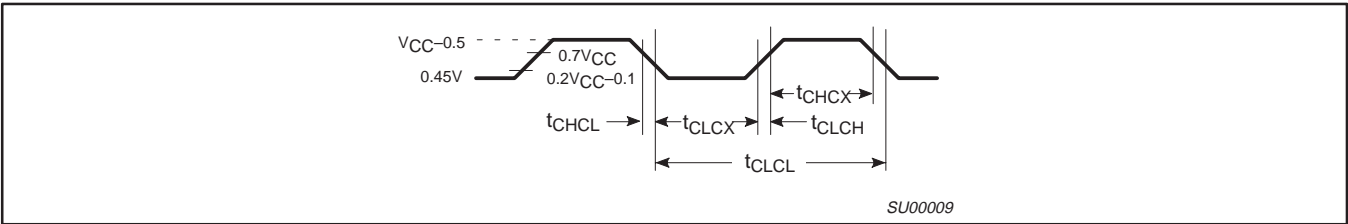


Figure 33. External Clock Drive

80C51 8-bit microcontroller family
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8XC54/58
8XC51FA/FB/FC/80C51FA
8XC51RA+/RB+/RC+/RD+/80C51RA+

EPROM CHARACTERISTICS

All these devices can be programmed by using a modified Improved Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The family contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as being manufactured by Philips.

Table 9 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 41 and 42. Figure 43 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 41. Note that the device is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 41. The code byte to be programmed into that location is applied to port 0. RST, \overline{PSEN} and pins of ports 2 and 3 specified in Table 9 are held at the 'Program Code Data' levels indicated in Table 9. The ALE/PROG is pulsed low 5 times as shown in Figure 42.

To program the encryption table, repeat the 5 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 5 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bits can still be programmed.

Note that the \overline{EA}/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bits 2 and 3 have not been programmed, the on-chip program memory can be read out for program verification. The

address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 43. The other pins are held at the 'Verify Code Data' levels indicated in Table 9. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the 64 byte encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = BBH indicates 87C54

BDH indicates 87C58

B1H indicates 87C51FA

B2H indicates 87C51FB

B3H indicates 87C51FC

CAH indicates 87C51RA+

CBH indicates 87C51RB+

CCH indicates 87C51RC+

CDH indicates 87C51RD+

(060H) = NA

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 9, and which satisfies the timing specifications, is suitable.

Security Bits

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 (see Table 10) is programmed, MOV_C instructions executed from external program memory are disabled from fetching code bytes from the internal memory, EA is latched on Reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

Encryption Array

64 bytes of encryption array are initially unprogrammed (all 1s).

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8XC51RA+/RB+/RC+/RD+/80C51RA+

Table 9. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	EA/V _{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V _{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V _{PP}	1	0	1	0
Pgm security bit 1	1	0	0*	V _{PP}	1	1	1	1
Pgm security bit 2	1	0	0*	V _{PP}	1	1	0	0
Pgm security bit 3	1	0	0*	V _{PP}	0	1	0	1

NOTES:

1. '0' = Valid low for that pin, '1' = valid high for that pin.

2. V_{PP} = 12.75V ±0.25V.

3. V_{CC} = 5V±10% during programming and verification.

* ALE/PROG receives 5 programming pulses for code data (also for user array; 5 pulses for encryption or security bits) while V_{PP} is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

Table 10. Program Security Bits for EPROM Devices

PROGRAM LOCK BITS ^{1, 2}				PROTECTION DESCRIPTION
	SB1	SB2	SB3	
1	U	U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, external execution is disabled.

NOTES:

1. P – programmed. U – unprogrammed.

2. Any other combination of the security bits is not defined.

80C51 8-bit microcontroller family
8K–64K/256–1K OTP/ROM/ROMless, low voltage (2.7V–5.5V),
low power, high speed (33MHz)

8XC54/58
8XC51FA/FB/FC/80C51FA
8XC51RA+/RB+/RC+/RD+/80C51RA+

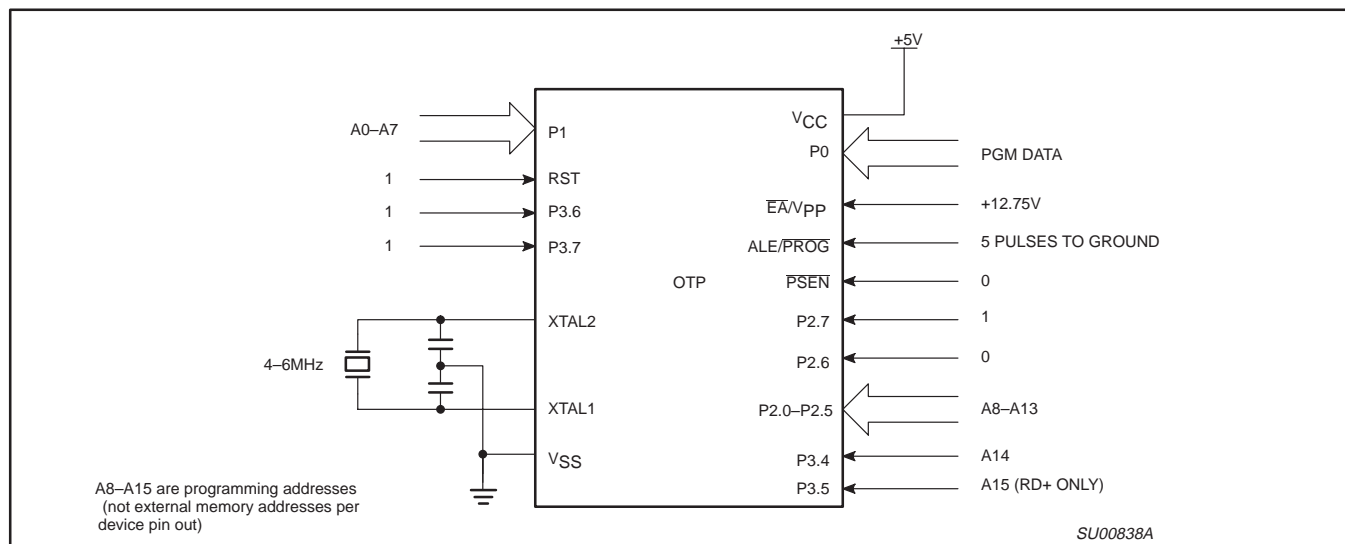


Figure 41. Programming Configuration

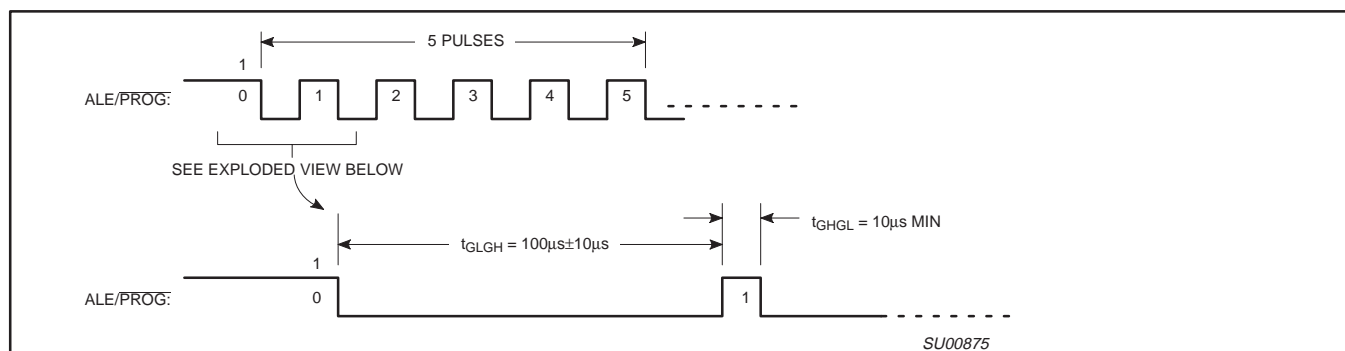


Figure 42. PROG Waveform

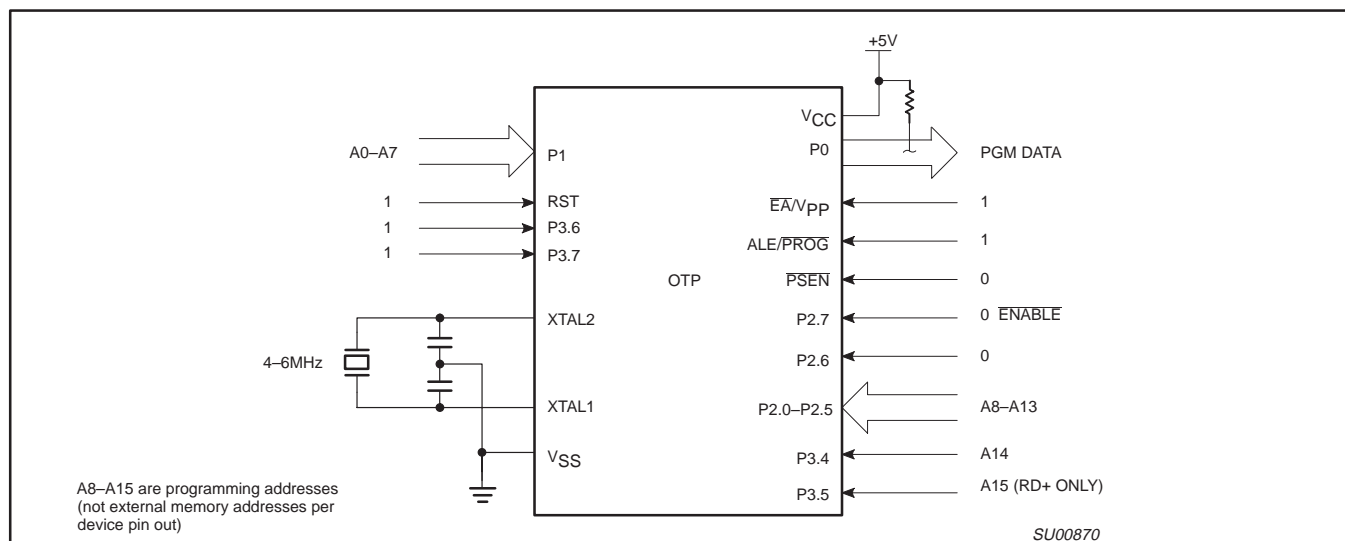


Figure 43. Program Verification

80C51 8-bit microcontroller family
8K–64K/256–1K OTP/ROM/ROMless, low voltage (2.7V–5.5V),
low power, high speed (33MHz)

8XC54/58
8XC51FA/FB/FC/80C51FA
8XC51RA+/RB+/RC+/RD+/80C51RA+

MASK ROM DEVICES

Security Bits

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 (see Table 11) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the

internal memory, \overline{EA} is latched on Reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled.

Encryption Array

64 bytes of encryption array are initially unprogrammed (all 1s).

Table 11. Program Security Bits

PROGRAM LOCK BITS ^{1, 2}			PROTECTION DESCRIPTION
	SB1	SB2	
1	U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on Reset, and further programming of the EPROM is disabled.

NOTES:

1. P – programmed. U – unprogrammed.
2. Any other combination of the security bits is not defined.

ROM CODE SUBMISSION FOR 8K ROM DEVICES (83C51FA, AND 83C51RA+)

When submitting ROM code for the 8k ROM devices, the following must be specified:

1. 8k byte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 1FFFH	DATA	7:0	User ROM Data
2000H to 203FH	KEY	7:0	ROM Encryption Key FFH = no encryption
2040H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
2040H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. \overline{EA} is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

NOTE: Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

- Security Bit #1: ☐ Enabled ☐ Disabled
- Security Bit #2: ☐ Enabled ☐ Disabled
- Encryption: ☐ No ☐ Yes If Yes, must send key file.

80C51 8-bit microcontroller family
 8K–64K/256–1K OTP/ROM/ROMless, low voltage (2.7V–5.5V),
 low power, high speed (33MHz)

8XC54/58
 8XC51FA/FB/FC/80C51FA
 8XC51RA+/RB+/RC+/RD+/80C51RA+

ROM CODE SUBMISSION FOR 16K ROM DEVICES (80C54, 83C51FB AND 83C51RB+)

When submitting ROM code for the 16K ROM devices, the following must be specified:

1. 16k byte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 3FFFH	DATA	7:0	User ROM Data
4000H to 403FH	KEY	7:0	ROM Encryption Key FFH = no encryption
4040H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
4040H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. \overline{EA} is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

NOTE: Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1: ☐ Enabled ☐ Disabled

Security Bit #2: ☐ Enabled ☐ Disabled

Encryption: ☐ No ☐ Yes If Yes, must send key file.