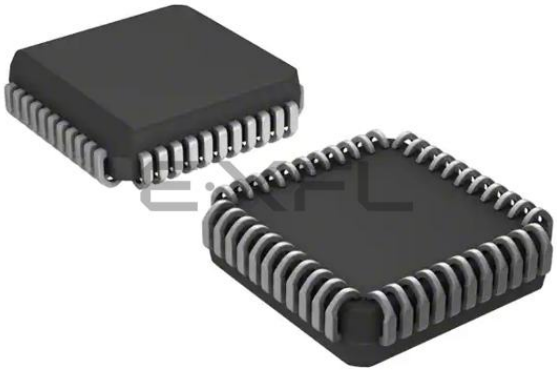

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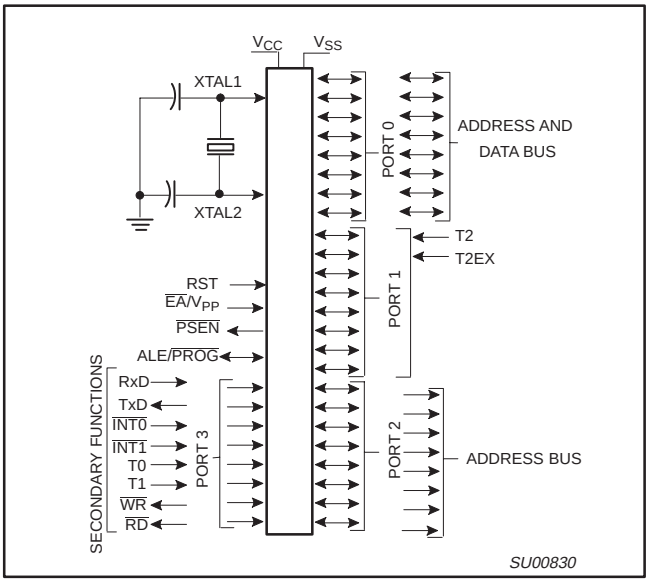
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

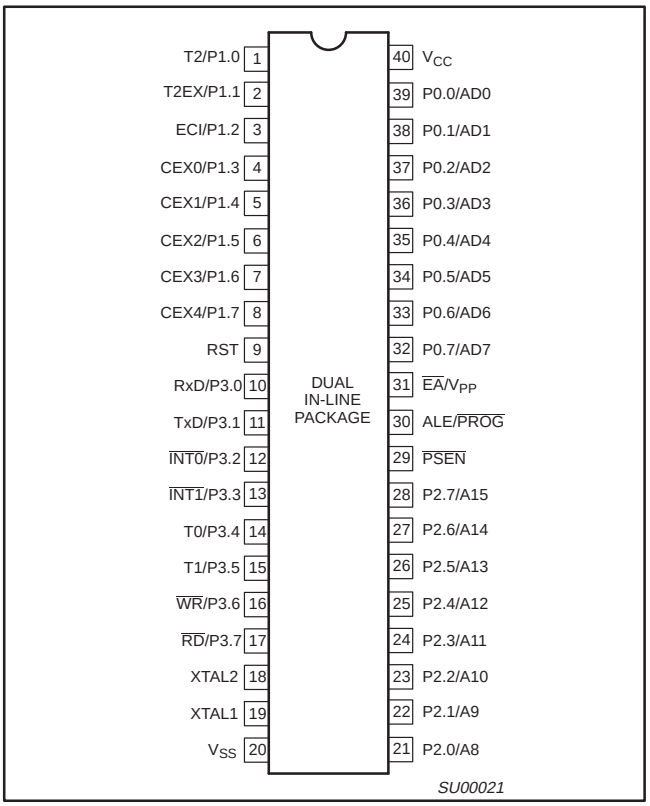
| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | EBI/EMI, UART/USART |
| Peripherals | POR, PWM |
| Number of I/O | 32 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c51fa-5a-512 |

## LOGIC SYMBOL

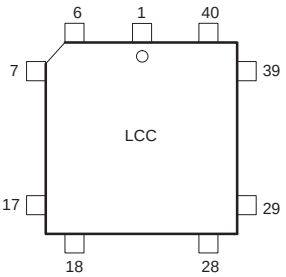



## PIN CONFIGURATIONS

## DUAL IN-LINE PACKAGE PIN FUNCTIONS




## PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

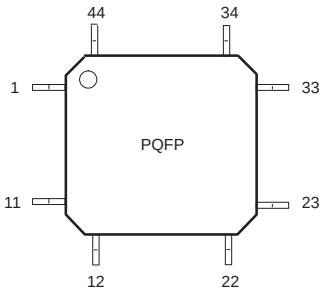



| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | NIC* | 16 | P3.4/T0 | 31 | P2.7/A15 |
| 2 | P1.0/T2 | 17 | P3.5/T1 | 32 | PSEN |
| 3 | P1.1/T2EX | 18 | P3.6/WR | 33 | ALE/PROG |
| 4 | P1.2/ECI | 19 | P3.7/RD | 34 | NIC* |
| 5 | P1.3/CEX0 | 20 | XTAL2 | 35 | EA/VPP |
| 6 | P1.4/CEX1 | 21 | XTAL1 | 36 | P0.7/AD7 |
| 7 | P1.5/CEX2 | 22 | VSS | 37 | P0.6/AD6 |
| 8 | P1.6/CEX3 | 23 | NIC* | 38 | P0.5/AD5 |
| 9 | P1.7/CEX4 | 24 | P2.0/A8 | 39 | P0.4/AD4 |
| 10 | RST | 25 | P2.1/A9 | 40 | P0.3/AD3 |
| 11 | P3.0/RxD | 26 | P2.2/A10 | 41 | P0.2/AD2 |
| 12 | NIC* | 27 | P2.3/A11 | 42 | P0.1/AD1 |
| 13 | P3.1/TxD | 28 | P2.4/A12 | 43 | P0.0/AD0 |
| 14 | P3.2/INT0 | 29 | P2.5/A13 | 44 | VCC |
| 15 | P3.3/INT1 | 30 | P2.6/A14 | | |

* NO INTERNAL CONNECTION

SU00023

## PLASTIC QUAD FLAT PACK PIN FUNCTIONS




| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | P1.5/CEX2 | 16 | VSS | 31 | P0.6/AD6 |
| 2 | P1.6/CEX3 | 17 | NIC* | 32 | P0.5/AD5 |
| 3 | P1.7/CEX4 | 18 | P2.0/A8 | 33 | P0.4/AD4 |
| 4 | RST | 19 | P2.1/A9 | 34 | P0.3/AD3 |
| 5 | P3.0/RxD | 20 | P2.2/A10 | 35 | P0.2/AD2 |
| 6 | NIC* | 21 | P2.3/A11 | 36 | P0.1/AD1 |
| 7 | P3.1/TxD | 22 | P2.4/A12 | 37 | P0.0/AD0 |
| 8 | P3.2/INT0 | 23 | P2.5/A13 | 38 | VCC |
| 9 | P3.3/INT1 | 24 | P2.6/A14 | 39 | NIC* |
| 10 | P3.4/T0 | 25 | P2.7/A15 | 40 | P1.0/T2 |
| 11 | P3.5/T1 | 26 | PSEN | 41 | P1.1/T2EX |
| 12 | P3.6/WR | 27 | ALE/PROG | 42 | P1.2/ECI |
| 13 | P3.7/RD | 28 | NIC* | 43 | P1.3/CEX0 |
| 14 | XTAL2 | 29 | EA/VPP | 44 | P1.4/CEX1 |
| 15 | XTAL1 | 30 | P0.7/AD7 | | |

* NO INTERNAL CONNECTION

SU00024

## PIN DESCRIPTIONS (Continued)

| MNEMONIC | PIN NUMBER DIP | PIN NUMBER LCC | PIN NUMBER QFP | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|---|
| $\overline{PSEN}$ | 29 | 32 | 26 | O | **Program Store Enable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory. |
| $\overline{EA}/V_{PP}$ | 31 | 35 | 29 | I | **External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations starting with 0000H. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 8k Devices (IFFFH), 16k Devices (3FFFH) or 32k Devices (7FFFH). Since the RD+ has 64k Internal Memory, the RD+ will execute only from internal memory when $\overline{EA}$ is held high. This pin also receives the 12.75 V programming supply voltage ($V_{PP}$) during EPROM programming. If security bit 1 is programmed, $\overline{EA}$ will be internally latched on Reset. |
| XTAL1 | 19 | 21 | 15 | I | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| XTAL2 | 18 | 20 | 14 | O | **Crystal 2:** Output from the inverting oscillator amplifier. |

**NOTE:**
To avoid “latch-up” effect at power-on, the voltage on any pin at any time must not be higher than $V_{CC}$ + 0.5 V or $V_{SS}$ – 0.5 V, respectively.

## 8XC54/58 ORDERING INFORMATION

| | MEMORY SIZE 16K × 8 | MEMORY SIZE 32K × 8 | TEMPERATURE RANGE °C AND PACKAGE | VOLTAGE RANGE | FREQ. (MHz) | DWG. # |
|---|---|---|---|---|---|---|
| ROM | P80C54SBPN | P80C58SBPN | 0 to +70, Plastic Dual In-line Package | 2.7 V to 5.5 V | 0 to 16 | SOT129-1 |
| OTP | P87C54SBPN | P87C58SBPN | | | | |
| ROM | P80C54SBAA | P80C58SBAA | 0 to +70, Plastic Leaded Chip Carrier | 2.7 V to 5.5 V | 0 to 16 | SOT187-2 |
| OTP | P87C54SBAA | P87C58SBAA | | | | |
| ROM | P80C54SBBB | P80C58SBBB | 0 to +70, Plastic Quad Flat Pack | 2.7 V to 5.5 V | 0 to 16 | SOT307-2 |
| OTP | P87C54SBBB | P87C58SBBB | | | | |
| ROM | P80C54SFPN | P80C58SFPN | –40 to +85, Plastic Dual In-line Package | 2.7 V to 5.5 V | 0 to 16 | SOT129-1 |
| OTP | P87C54SFPN | P87C58SFPN | | | | |
| ROM | P80C54SFAA | P80C58SFAA | –40 to +85, Plastic Leaded Chip Carrier | 2.7 V to 5.5 V | 0 to 16 | SOT187-2 |
| OTP | P87C54SFAA | P87C58SFAA | | | | |
| ROM | P80C54SFBB | P80C58SFBB | –40 to +85, Plastic Quad Flat Pack | 2.7 V to 5.5 V | 0 to 16 | SOT307-2 |
| OTP | P87C54SFBB | P87C58SFBB | | | | |
| ROM | P80C54UBAA | P80C58UBAA | 0 to +70, Plastic Leaded Chip Carrier | 5 V | 0 to 33 | SOT187-2 |
| OTP | P87C54UBAA | P87C58UBAA | | | | |
| ROM | P80C54UBPN | P80C58UBPN | 0 to +70, Plastic Dual In-line Package | 5 V | 0 to 33 | SOT129-1 |
| OTP | P87C54UBPN | P87C58UBPN | | | | |
| ROM | P80C54UBBB | P80C58UBBB | 0 to +70, Plastic Quad Flat Pack | 5 V | 0 to 33 | SOT307-2 |
| OTP | P87C54UBBB | P87C58UBBB | | | | |
| ROM | P80C54UFAA | P80C58UFAA | –40 to +85, Plastic Leaded Chip Carrier | 5 V | 0 to 33 | SOT187-2 |
| OTP | P87C54UFAA | P87C58UFAA | | | | |
| ROM | P80C54UFPN | P80C58UFPN | –40 to +85, Plastic Dual In-line Package | 5 V | 0 to 33 | SOT129-1 |
| OTP | P87C54UFPN | P87C58UFPN | | | | |
| ROM | P80C54UFBB | P80C58UFBB | –40 to +85, Plastic Quad Flat Pack | 5 V | 0 to 33 | SOT307-2 |
| OTP | P87C54UFBB | P87C58UFBB | | | | |

Note: For Multi Time Programmable devices, See P89C51RX+ Flash datasheet.

**Table 2. 8XC51FA/FB/FC, 8XC51RA+/RB+/RC+/RD+ Special Function Registers** (Continued)

| SYMBOL | DESCRIPTION | DIRECT ADDRESS | BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB | | | | | | | LSB | RESET VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PSW* | Program Status Word | D0H | CY | AC | F0 | RS1 | RS0 | OV | – | P | 000000x0B |
| RACAP2H# | Timer 2 Capture High | CBH | | | | | | | | | 00H |
| RACAP2L# | Timer 2 Capture Low | CAH | | | | | | | | | 00H |
| SADDR# | Slave Address | A9H | | | | | | | | | 00H |
| SADEN# | Slave Address Mask | B9H | | | | | | | | | 00H |
| SBUF | Serial Data Buffer | 99H | | | | | | | | | xxxxxxxxB |
| | | | 9F | 9E | 9D | 9C | 9B | 9A | 99 | 98 | |
| SCON* | Serial Control | 98H | SM0/FE | SM1 | SM2 | REN | TB8 | RB8 | TI | RI | 00H |
| SP | Stack Pointer | 81H | | | | | | | | | 07H |
| | | | 8F | 8E | 8D | 8C | 8B | 8A | 89 | 88 | |
| TCON* | Timer Control | 88H | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00H |
| | | | CF | CE | CD | CC | CB | CA | C9 | C8 | |
| T2CON* | Timer 2 Control | C8H | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/$\overline{T2}$ | CP/$\overline{RL2}$ | 00H |
| T2MOD# | Timer 2 Mode Control | C9H | – | – | – | – | – | – | T2OE | DCEN | xxxxxx00B |
| TH0 | Timer High 0 | 8CH | | | | | | | | | 00H |
| TH1 | Timer High 1 | 8DH | | | | | | | | | 00H |
| TH2# | Timer High 2 | CDH | | | | | | | | | 00H |
| TL0 | Timer Low 0 | 8AH | | | | | | | | | 00H |
| TL1 | Timer Low 1 | 8BH | | | | | | | | | 00H |
| TL2# | Timer Low 2 | CCH | | | | | | | | | 00H |
| TMOD | Timer Mode | 89H | GATE | C/$\overline{T}$ | M1 | M0 | GATE | C/$\overline{T}$ | M1 | M0 | 00H |
| WDTRST | HDW Watchdog Timer Reset (RX+ only) | 0A6H | | | | | | | | | |

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
– Reserved bits.

## OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

## RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on $V_{CC}$ and RST must come up at the same time for a proper start-up. Ports 1, 2, and 3 will asynchronously be driven to their reset condition when a voltage above $V_{IH1}$ (min.) is applied to RESET.

## LOW POWER MODES

### Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

### Idle Mode

In the idle mode (see Table 3), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

### Power-Down Mode

To save even more power, a Power Down mode (see Table 3) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2.0V and care must be taken to return $V_{CC}$ to the minimum specified operating voltages before the Power Down Mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before $V_{CC}$ is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

### LPEP

The LPEP bit (AUXR.4), only needs to be set for applications operating at $V_{CC}$ less than 4V.

## POWER OFF FLAG

The Power Off Flag (POF) is set by on-chip circuitry when the $V_{CC}$ level on the 8XC51FX/8XC51RX+ rises from 0 to 5V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The $V_{CC}$ level must remain above 3V for the POF to remain unaffected by the $V_{CC}$ level.

### Design Consideration

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

### ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

### Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 61Hz to 4MHz at a 16MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

**Table 3. External Pin Status During Idle and Power-Down Mode**

| MODE | PROGRAM MEMORY | ALE | $\overline{PSEN}$ | PORT 0 | PORT 1 | PORT 2 | PORT 3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power-down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power-down | External | 0 | 0 | Float | Data | Data | Data |

## TIMER 2 OPERATION

### Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/$\overline{T}$2* in the special function register T2CON (see Figure 1). Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 4.

### Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by C/$\overline{T}$2* in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2= 1, Timer 2 operates as described above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt. The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). The capture mode is illustrated in Figure 2. (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/12 pulses.)

### Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured (as either a timer or counter [C/$\overline{T}$2* in T2CON]) then programmed to count up or down. The counting direction is determined by bit DCEN (Down Counter Enable) which is located in the T2MOD register (see Figure 3). When reset is applied the DCEN=0 which means Timer 2 will default to counting up. If DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 4 shows Timer 2 which will count up automatically since DCEN=0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 5 DCEN=1, which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16–bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

(MSB) (LSB)

| TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/$\overline{T2}$ | CP/$\overline{RL2}$ |
|---|---|---|---|---|---|---|---|

| Symbol | Position | Name and Significance |
|---|---|---|
| TF2 | T2CON.7 | Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1. |
| EXF2 | T2CON.6 | Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1). |
| RCLK | T2CON.5 | Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock. |
| TCLK | T2CON.4 | Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock. |
| EXEN2 | T2CON.3 | Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX. |
| TR2 | T2CON.2 | Start/stop control for Timer 2. A logic 1 starts the timer. |
| C/$\overline{T2}$ | T2CON.1 | Timer or counter select. (Timer 2)<br>0 = Internal timer (OSC/12)<br>1 = External event counter (falling edge triggered). |
| CP/$\overline{RL2}$ | T2CON.0 | Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow. |

*SU00728*

**Figure 1. Timer/Counter 2 (T2CON) Control Register**

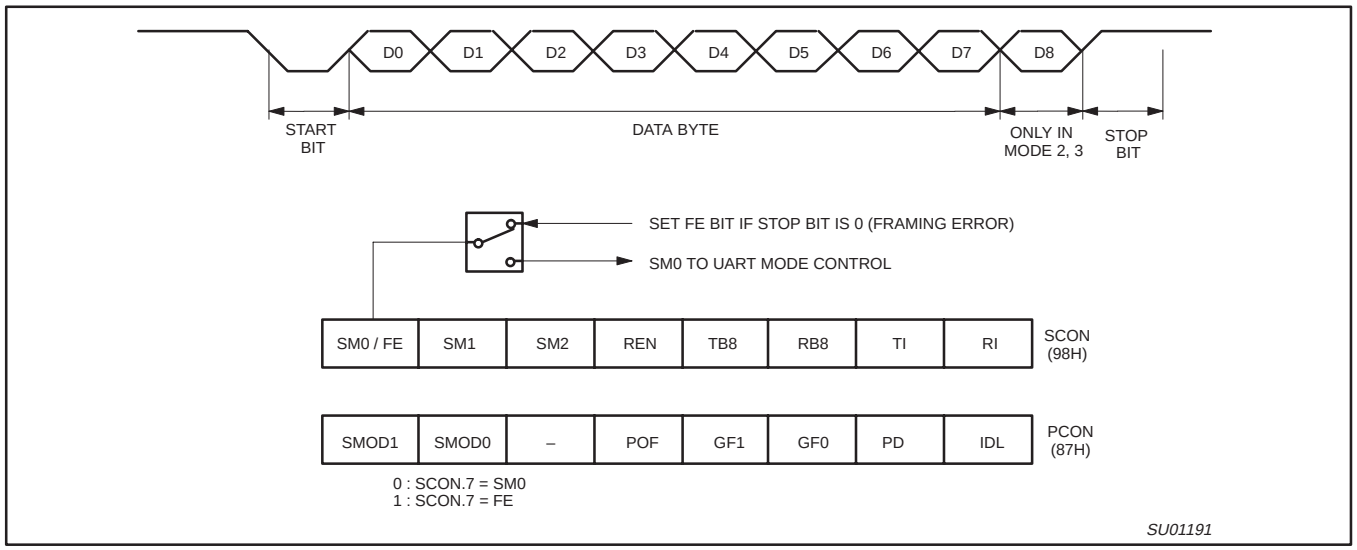



**Figure 8. UART Framing Error Detection**

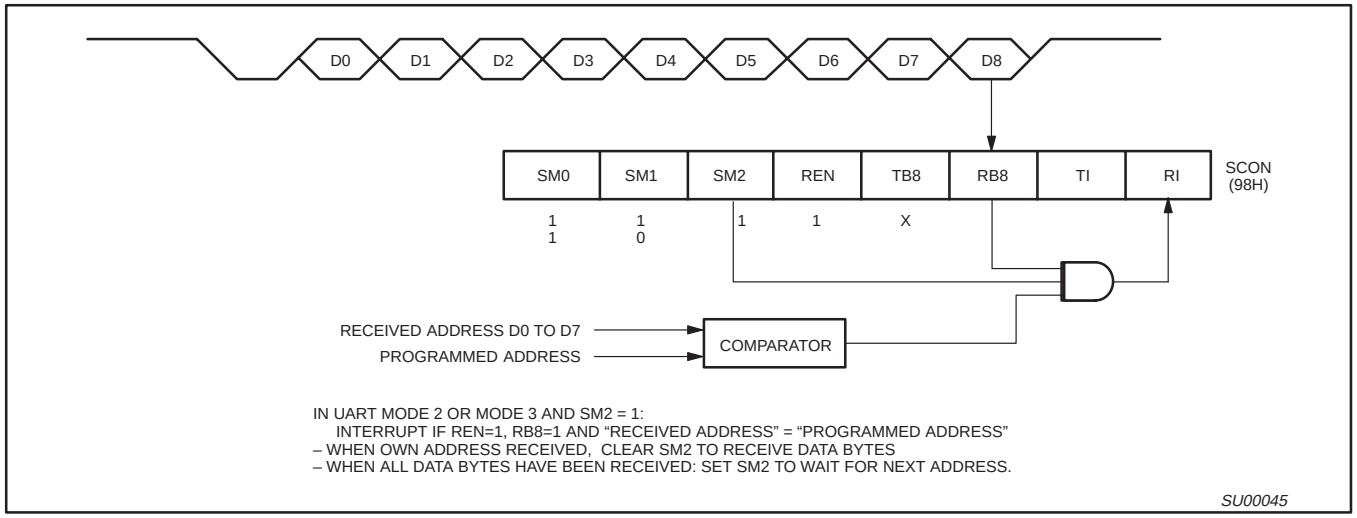



**Figure 9. UART Multiprocessor Communication, Automatic Address Recognition**

## Interrupt Priority Structure

The 8XC51FA/FB/FC and 8XC51RA+/RB+/RC+/RD+ have a 7-source four-level interrupt structure (see Table 8). The 80C54/58 have a 6-source four-level interrupt structure because these devices do not have a PCA.

There are 3 SFRs associated with the four-level interrupt. They are the IE, IP, and IPH. (See Figures 10, 11, and 12.) The IPH (Interrupt Priority High) register makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown in Figure 12.

The function of the IPH SFR is simple and when combined with the IP SFR determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

| PRIORITY BITS | | INTERRUPT PRIORITY LEVEL |
|---|---|---|
| IPH.x | IP.x | |
| 0 | 0 | Level 0 (lowest priority) |
| 0 | 1 | Level 1 |
| 1 | 0 | Level 2 |
| 1 | 1 | Level 3 (highest priority) |

The priority scheme for servicing the interrupts is the same as that for the 80C51, except there are four interrupt levels rather than two as on the 80C51. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

### Table 8. Interrupt Table

| SOURCE | POLLING PRIORITY | REQUEST BITS | HARDWARE CLEAR? | VECTOR ADDRESS |
|---|---|---|---|---|
| X0 | 1 | IE0 | N (L)[1] Y (T)[2] | 03H |
| T0 | 2 | TF0 | Y | 0B |
| X1 | 3 | IE1 | N (L) Y (T) | 13 |
| T1 | 4 | TF1 | Y | 1B |
| PCA | 5 | CF, CCFn n = 0–4 | N | 33 |
| SP | 6 | RI, TI | N | 23 |
| T2 | 7 | TF2, EXF2 | N | 2B |

**NOTES:**
1. L = Level activated
2. T = Transition activated

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **IE (0A8H)** | EA | EC | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

| BIT | SYMBOL | FUNCTION |
|---|---|---|
| IE.7 | EA | Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit. |
| IE.6 | EC | PCA interrupt enable bit for FX and RX+ only – otherwise it is not implemented. |
| IE.5 | ET2 | Timer 2 interrupt enable bit. |
| IE.4 | ES | Serial Port interrupt enable bit. |
| IE.3 | ET1 | Timer 1 interrupt enable bit. |
| IE.2 | EX1 | External interrupt 1 enable bit. |
| IE.1 | ET0 | Timer 0 interrupt enable bit. |
| IE.0 | EX0 | External interrupt 0 enable bit. |

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**Figure 10. IE Registers**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **IP (0B8H)** | — | PPC | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

Priority Bit = 1 assigns high priority
Priority Bit = 0 assigns low priority

| BIT | SYMBOL | FUNCTION |
|---|---|---|
| IP.7 | — | Not implemented, reserved for future use. |
| IP.6 | PPC | PCA interrupt priority bit for FX and RX+ only, otherwise it is not implemented. |
| IP.5 | PT2 | Timer 2 interrupt priority bit. |
| IP.4 | PS | Serial Port interrupt priority bit. |
| IP.3 | PT1 | Timer 1 interrupt priority bit. |
| IP.2 | PX1 | External interrupt 1 priority bit. |
| IP.1 | PT0 | Timer 0 interrupt priority bit. |
| IP.0 | PX0 | External interrupt 0 priority bit. |

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**Figure 11. IP Registers**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **IPH (B7H)** | — | PPCH | PT2H | PSH | PT1H | PX1H | PT0H | PX0H |

Priority Bit = 1 assigns higher priority
Priority Bit = 0 assigns lower priority

| BIT | SYMBOL | FUNCTION |
|---|---|---|
| IPH.7 | — | Not implemented, reserved for future use. |
| IPH.6 | PPCH | PCA interrupt priority bit high for FX and RX+ only, otherwise it is not implemented. |
| IPH.5 | PT2H | Timer 2 interrupt priority bit high. |
| IPH.4 | PSH | Serial Port interrupt priority bit high. |
| IPH.3 | PT1H | Timer 1 interrupt priority bit high. |
| IPH.2 | PX1H | External interrupt 1 priority bit high. |
| IPH.1 | PT0H | Timer 0 interrupt priority bit high. |
| IPH.0 | PX0H | External interrupt 0 priority bit high. |

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**Figure 12. IPH Registers**

## Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

## Reduced EMI Mode

**AUXR (8EH)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | EXTRAM | AO |

| | | |
|---|---|---|
| AUXR.1 | EXTRAM | (RX+ only) |
| AUXR.0 | AO | Turns off ALE output. |

## Dual DPTR

The dual DPTR structure (see Figure 13) is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

- New Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxxx00x0B

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | – | – | LPEP | GF3 | 0 | – | DPS |

Where:

DPS = AUXR1/bit0 = Switches between DPTR0 and DPTR1.

| Select Reg | DPS |
|---|---|
| DPTR0 | 0 |
| DPTR1 | 1 |

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

The GF3 bit is a general purpose user–defined flag. Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC DPTR instruction without affecting the GF3 or LPEP bits.

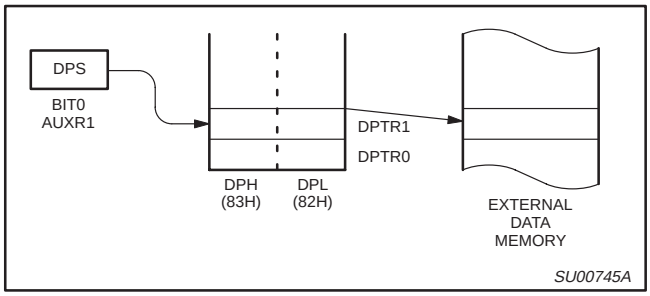



**Figure 13.**

**DPTR Instructions**

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

| | |
|---|---|
| INC DPTR | Increments the data pointer by 1 |
| MOV DPTR, #data16 | Loads the DPTR with a 16-bit constant |
| MOV A, @ A+DPTR | Move code byte relative to DPTR to ACC |
| MOVX A, @ DPTR | Move external RAM (16-bit address) to ACC |
| MOVX @ DPTR , A | Move ACC to external RAM (16-bit address) |
| JMP @ A + DPTR | Jump indirect relative to DPTR |

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs. See application note AN458 for more details.

**(8XC51FX and 8XC51RX+ ONLY)**

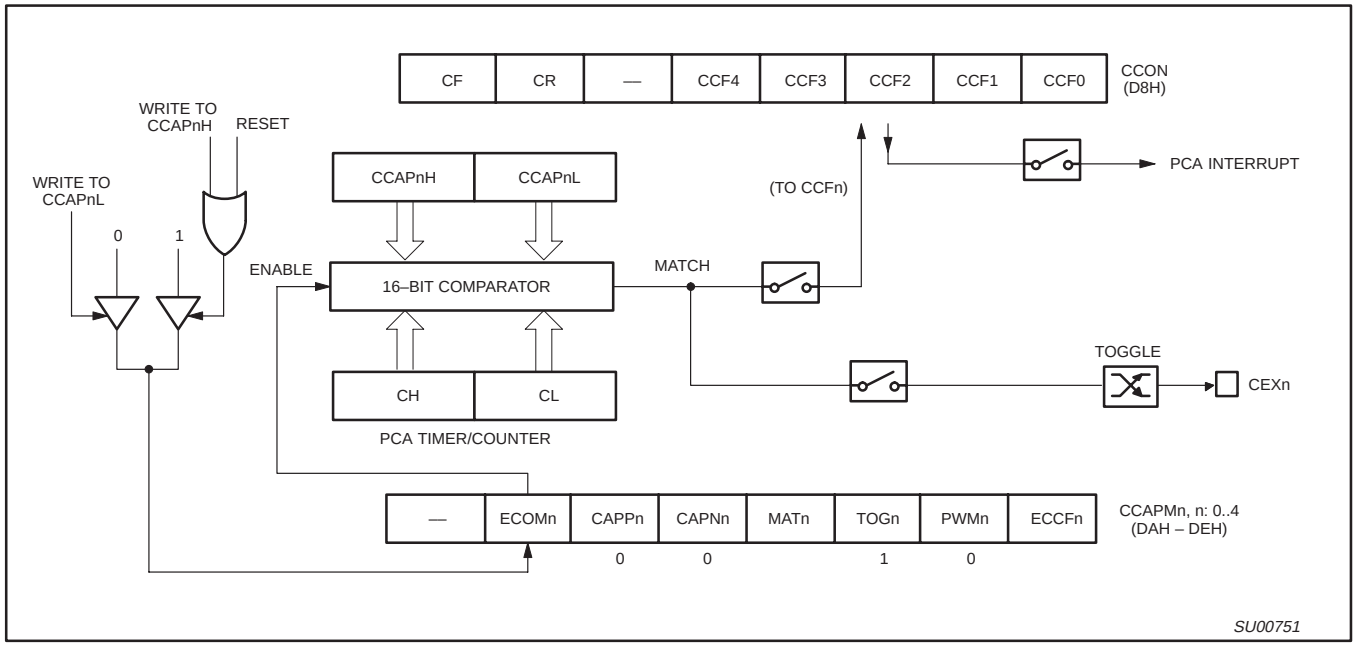



**Figure 23. PCA High Speed Output Mode**

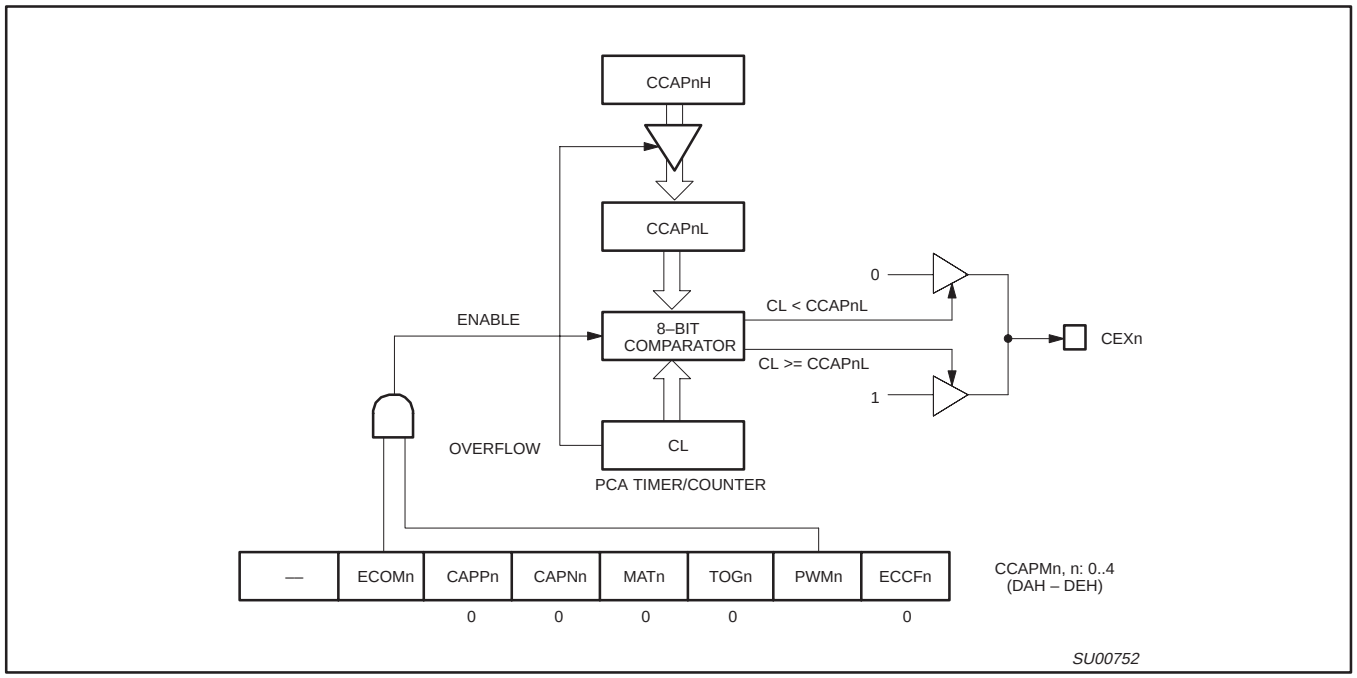



**Figure 24. PCA PWM Mode**

**(8XC51FX and 8XC51RX+ ONLY)**

```
INIT_WATCHDOG:
   MOV CCAPM4, #4CH         ; Module 4 in compare mode
   MOV CCAP4L, #0FFH        ; Write to low byte first
   MOV CCAP4H, #0FFH        ; Before PCA timer counts up to
                            ; FFFF Hex, these compare values
                            ; must be changed
   ORL CMOD, #40H           ; Set the WDTE bit to enable the
                            ; watchdog timer without changing
                            ; the other bits in CMOD
;
;*******************************************************************
;
; Main program goes here, but CALL WATCHDOG periodically.
;
;*******************************************************************
;
WATCHDOG:
   CLR EA                   ; Hold off interrupts
   MOV CCAP4L, #00          ; Next compare value is within
   MOV CCAP4H, CH           ; 255 counts of the current PCA
   SETB EA                  ; timer value
   RET
```

**Figure 26. PCA Watchdog Timer Initialization Code**

**(8XC51RX+ ONLY)**

## Expanded Data RAM Addressing (8XC51RX+ ONLY)

The 8XC51RX+ have internal data memory that is mapped into four separate segments: the lower 128 bytes of RAM, upper 128 bytes of RAM, 128 bytes Special Function Register (SFR), and 256 bytes (768 for RD+) expanded RAM (EXTRAM).

The four segments are:

1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
4. The 256-bytes (768 for RD+) expanded RAM ((EXTRAM (256-bytes) 00H–FFH)) and ((EXTRAM (768-bytes for RD+) 00H – 2FFH)) are indirectly accessed by move external instruction, MOVX, and with the EXTRAM bit cleared, see Figure 27.

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction. Instructions that use direct addressing access SFR space. For example:

MOV 0A0H,#data

accesses the SFR at location 0A0H (which is P2). Instructions that use indirect addressing access the Upper 128 bytes of data RAM. For example:

MOV @R0,#data

where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).
The EXTRAM can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory is physically located on-chip, logically occupies the first 256-bytes (768 for RD+) of external data memory.

With EXTRAM = 0, the EXTRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to EXTRAM will not affect ports P0, P3.6 (WR#) and P3.7 (RD#). P2 SFR is output during external addressing. For example, with EXTRAM = 0,

MOVX @R0,#data

where R0 contains 0A0H, access the EXTRAM at address 0A0H rather than external memory. An access to external data memory locations higher than FFH (2FF for RD+) (i.e., 0100H to FFFFH) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals. Refer to Figure 28.

With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an 8-bit address multiplexed with data on Port 0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a 16-bit address. Port 2 outputs the high-order eight address bits (the contents of DPH) while Port 0 multiplexes the low-order eight address bits (DPL) with data. MOVX @Ri and MOVX @DPTR will generate either read or write signals on P3.6 (#WR) and P3.7 (#RD).

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the EXTRAM.

**AUXR** Address = 8EH — Reset Value = xxxx xx00B

Not Bit Addressable

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | **EXTRAM** | **AO** |
| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| **AO** | Disable/Enable ALE |
| | **AO** **Operating Mode**<br>0 ALE is emitted at a constant rate of 1/6 the oscillator frequency.<br>1 ALE is active only during a MOVX or MOVC instruction. |
| **EXTRAM** | Internal/External RAM access using MOVX @Ri/@DPTR |
| | **EXTRAM** **Operating Mode**<br>0 Internal ERAM (00H–FFH) (00H–2FFH for RD+) access using MOVX @Ri/@DPTR<br>1 External data memory access. |
| — | Not implemented, reserved for future use*. |

**NOTE:**
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

*SU01003*

**Figure 27. AUXR: Auxiliary Register (RX+ only)**

## DC ELECTRICAL CHARACTERISTICS

$T_{amb}$ = 0°C to +70°C or –40°C to +85°C, $V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V (16MHz devices)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP[1] | MAX | |
| $V_{IL}$ | Input low voltage | 4.0V < $V_{CC}$ < 5.5V | –0.5 | | $0.2V_{CC}$–0.1 | V |
| | | 2.7V<$V_{CC}$< 4.0V | –0.5 | | 0.7 | V |
| $V_{IH}$ | Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$) | | $0.2V_{CC}$+0.9 | | $V_{CC}$+0.5 | V |
| $V_{IH1}$ | Input high voltage, XTAL1, RST | | $0.7V_{CC}$ | | $V_{CC}$+0.5 | V |
| $V_{OL}$ | Output low voltage, ports 1, 2 [8] | $V_{CC}$ = 2.7V<br>$I_{OL}$ = 1.6mA[2] | | | 0.4 | V |
| $V_{OL1}$ | Output low voltage, port 0, ALE, $\overline{PSEN}$[8, 7] | $V_{CC}$ = 2.7V<br>$I_{OL}$ = 3.2mA[2] | | | 0.4 | V |
| $V_{OH}$ | Output high voltage, ports 1, 2, 3 [3] | $V_{CC}$ = 2.7V<br>$I_{OH}$ = –20µA | $V_{CC}$ – 0.7 | | | V |
| | | $V_{CC}$ = 4.5V<br>$I_{OH}$ = –30µA | $V_{CC}$ – 0.7 | | | V |
| $V_{OH1}$ | Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3] | $V_{CC}$ = 2.7V<br>$I_{OH}$ = –3.2mA | $V_{CC}$ – 0.7 | | | V |
| $I_{IL}$ | Logical 0 input current, ports 1, 2, 3 | $V_{IN}$ = 0.4V | –1 | | –50 | µA |
| $I_{TL}$ | Logical 1-to-0 transition current, ports 1, 2, 3[6] | $V_{IN}$ = 2.0V<br>See note 4 | | | –650 | µA |
| $I_{LI}$ | Input leakage current, port 0 | 0.45 < $V_{IN}$ < $V_{CC}$ – 0.3 | | | ±10 | µA |
| $I_{CC}$ | Power supply current (see Figure 36): | See note 5 | | | | |
| | Active mode @ 16MHz (all except 8XC51RD+) | | | | 15 | mA |
| | 87C51RD+ | | | | 16 | mA |
| | Idle mode @ 16MHz | | | | 4 | mA |
| | Power-down mode or clock stopped (see Figure 40 for conditions) | $T_{amb}$ = 0°C to 70°C | | 3 | 50 | µA |
| | | $T_{amb}$ = –40°C to +85°C | | | 75 | µA |
| $R_{RST}$ | Internal reset pull-down resistor | | 40 | | 225 | kΩ |
| $C_{IO}$ | Pin capacitance[10] (except $\overline{EA}$) | | | | 15 | pF |

**NOTES:**

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the $V_{OL}$s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. $I_{OL}$ can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall below the $V_{CC}$–0.7 specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when $V_{IN}$ is approximately 2V.
5. See Figures 37 through 40 for $I_{CC}$ test conditions, and Figure 36 for $I_{CC}$ vs Freq.
   Active mode: $I_{CC}$ = (0.9 × FREQ. + 1.1)mA for all devices except 8XC51RD+; 8XC51RD+ $I_{CC}$ = (0.9 x Freq +2.1) mA
   Idle mode: $I_{CC}$ = (0.18 × FREQ. +1.01)mA
6. This value applies to $T_{amb}$ = 0°C to +70°C. For $T_{amb}$ = –40°C to +85°C, $I_{TL}$ = –750µA.
7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
8. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 15mA (*NOTE: This is 85°C specification.)
   Maximum $I_{OL}$ per 8-bit port: 26mA
   Maximum total $I_{OL}$ for all outputs: 71mA
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. ALE is tested to $V_{OH1}$, except when ALE is off then $V_{OH}$ is the voltage specification.
10. Pin capacitance is characterized but not tested. Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except $\overline{EA}$ is 25pF).

## AC ELECTRICAL CHARACTERISTICS

$T_{amb}$ = 0°C to +70°C or –40°C to +85°C, $V_{CC}$ = 5V ±10%, $V_{SS}$ = 0V[1, 2, 3]

| SYMBOL | FIGURE | PARAMETER | VARIABLE CLOCK[4] | | 33MHz CLOCK | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{LHLL}$ | 29 | ALE pulse width | $2t_{CLCL}$–40 | | 21 | | ns |
| $t_{AVLL}$ | 29 | Address valid to ALE low | $t_{CLCL}$–25 | | 5 | | ns |
| $t_{LLAX}$ | 29 | Address hold after ALE low | $t_{CLCL}$–25 | | | | ns |
| $t_{LLIV}$ | 29 | ALE low to valid instruction in | | $4t_{CLCL}$–65 | | 55 | ns |
| $t_{LLPL}$ | 29 | ALE low to $\overline{PSEN}$ low | $t_{CLCL}$–25 | | 5 | | ns |
| $t_{PLPH}$ | 29 | $\overline{PSEN}$ pulse width | $3t_{CLCL}$–45 | | 45 | | ns |
| $t_{PLIV}$ | 29 | $\overline{PSEN}$ low to valid instruction in | | $3t_{CLCL}$–60 | | 30 | ns |
| $t_{PXIX}$ | 29 | Input instruction hold after $\overline{PSEN}$ | 0 | | 0 | | ns |
| $t_{PXIZ}$ | 29 | Input instruction float after $\overline{PSEN}$ | | $t_{CLCL}$–25 | | 5 | ns |
| $t_{AVIV}$ | 29 | Address to valid instruction in | | $5t_{CLCL}$–80 | | 70 | ns |
| $t_{PLAZ}$ | 29 | $\overline{PSEN}$ low to address float | | 10 | | 10 | ns |
| **Data Memory** | | | | | | | |
| $t_{RLRH}$ | 30, 31 | $\overline{RD}$ pulse width | $6t_{CLCL}$–100 | | 82 | | ns |
| $t_{WLWH}$ | 30, 31 | $\overline{WR}$ pulse width | $6t_{CLCL}$–100 | | 82 | | ns |
| $t_{RLDV}$ | 30, 31 | $\overline{RD}$ low to valid data in | | $5t_{CLCL}$–90 | | 60 | ns |
| $t_{RHDX}$ | 30, 31 | Data hold after $\overline{RD}$ | 0 | | 0 | | ns |
| $t_{RHDZ}$ | 30, 31 | Data float after $\overline{RD}$ | | $2t_{CLCL}$–28 | | 32 | ns |
| $t_{LLDV}$ | 30, 31 | ALE low to valid data in | | $8t_{CLCL}$–150 | | 90 | ns |
| $t_{AVDV}$ | 30, 31 | Address to valid data in | | $9t_{CLCL}$–165 | | 105 | ns |
| $t_{LLWL}$ | 30, 31 | ALE low to $\overline{RD}$ or $\overline{WR}$ low | $3t_{CLCL}$–50 | $3t_{CLCL}$+50 | 40 | 140 | ns |
| $t_{AVWL}$ | 30, 31 | Address valid to $\overline{WR}$ low or $\overline{RD}$ low | $4t_{CLCL}$–75 | | 45 | | ns |
| $t_{QVWX}$ | 30, 31 | Data valid to $\overline{WR}$ transition | $t_{CLCL}$–30 | | 0 | | ns |
| $t_{WHQX}$ | 30, 31 | Data hold after $\overline{WR}$ | $t_{CLCL}$–25 | | 5 | | ns |
| $t_{QVWH}$ | 31 | Data valid to $\overline{WR}$ high | $7t_{CLCL}$–130 | | 80 | | ns |
| $t_{RLAZ}$ | 30, 31 | $\overline{RD}$ low to address float | | 0 | | 0 | ns |
| $t_{WHLH}$ | 30, 31 | $\overline{RD}$ or $\overline{WR}$ high to ALE high | $t_{CLCL}$–25 | $t_{CLCL}$+25 | 5 | 55 | ns |
| **External Clock** | | | | | | | |
| $t_{CHCX}$ | 33 | High time | $0.38t_{CLCL}$ | $t_{CLCL}$–$t_{CLCX}$ | | | ns |
| $t_{CLCX}$ | 33 | Low time | $0.38t_{CLCL}$ | $t_{CLCL}$–$t_{CHCX}$ | | | ns |
| $t_{CLCH}$ | 33 | Rise time | | 5 | | | ns |
| $t_{CHCL}$ | 33 | Fall time | | 5 | | | ns |
| **Shift Register** | | | | | | | |
| $t_{XLXL}$ | 32 | Serial port clock cycle time | $12t_{CLCL}$ | | 360 | | ns |
| $t_{QVXH}$ | 32 | Output data setup to clock rising edge | $10t_{CLCL}$–133 | | 167 | | ns |
| $t_{XHQX}$ | 32 | Output data hold after clock rising edge | $2t_{CLCL}$–80 | | | | ns |
| $t_{XHDX}$ | 32 | Input data hold after clock rising edge | 0 | | 0 | | ns |
| $t_{XHDV}$ | 32 | Clock rising edge to input data valid | | $10t_{CLCL}$–133 | | 167 | ns |

**NOTES:**
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. Interfacing the microcontroller to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. For frequencies equal or less than 16MHz, see 16MHz “AC Electrical Characteristics”, page 38.
5. Parts are guaranteed to operate down to 0Hz.

## Table 9. EPROM Programming Modes

| MODE | RST | $\overline{PSEN}$ | ALE/$\overline{PROG}$ | $\overline{EA}$/$V_{PP}$ | P2.7 | P2.6 | P3.7 | P3.6 |
|---|---|---|---|---|---|---|---|---|
| Read signature | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| Program code data | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 1 | 1 |
| Verify code data | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| Pgm encryption table | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 1 | 0 |
| Pgm security bit 1 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 1 | 1 |
| Pgm security bit 2 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 0 | 0 |
| Pgm security bit 3 | 1 | 0 | 0* | $V_{PP}$ | 0 | 1 | 0 | 1 |

**NOTES:**
1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. $V_{PP}$ = 12.75V ±0.25V.
3. $V_{CC}$ = 5V±10% during programming and verification.

* ALE/$\overline{PROG}$ receives 5 programming pulses for code data (also for user array; 5 pulses for encryption or security bits) while $V_{PP}$ is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

## Table 10. Program Security Bits for EPROM Devices

| PROGRAM LOCK BITS[1, 2] | | | | |
|---|---|---|---|---|
| | SB1 | SB2 | SB3 | PROTECTION DESCRIPTION |
| 1 | U | U | U | No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.) |
| 2 | P | U | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on Reset, and further programming of the EPROM is disabled. |
| 3 | P | P | U | Same as 2, also verify is disabled. |
| 4 | P | P | P | Same as 3, external execution is disabled. |

**NOTES:**
1. P – programmed. U – unprogrammed.
2. Any other combination of the security bits is not defined.

## ROM CODE SUBMISSION FOR 16K ROM DEVICES (80C54, 83C51FB AND 83C51RB+)

When submitting ROM code for the 16K ROM devices, the following must be specified:

1. 16k byte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

| ADDRESS | CONTENT | BIT(S) | COMMENT |
|---|---|---|---|
| 0000H to 3FFFH | DATA | 7:0 | User ROM Data |
| 4000H to 403FH | KEY | 7:0 | ROM Encryption Key<br>FFH = no encryption |
| 4040H | SEC | 0 | ROM Security Bit 1<br>0 = enable security<br>1 = disable security |
| 4040H | SEC | 1 | ROM Security Bit 2<br>0 = enable security<br>1 = disable security |

**Security Bit 1:** When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. $\overline{EA}$ is latched on Reset.

**Security Bit 2:** When programmed, this bit inhibits Verify User ROM.

**NOTE:** Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1: ☐ Enabled ☐ Disabled

Security Bit #2: ☐ Enabled ☐ Disabled

Encryption: ☐ No ☐ Yes If Yes, must send key file.

## ROM CODE SUBMISSION FOR 32K ROM DEVICES (80C58, 83C51FC, AND 83C51RC+)

When submitting ROM code for the 32K ROM devices, the following must be specified:

1. 32k byte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

| ADDRESS | CONTENT | BIT(S) | COMMENT |
|---|---|---|---|
| 0000H to 7FFFH | DATA | 7:0 | User ROM Data |
| 8000H to 803FH | KEY | 7:0 | ROM Encryption Key<br>FFH = no encryption |
| 8040H | SEC | 0 | ROM Security Bit 1<br>0 = enable security<br>1 = disable security |
| 8040H | SEC | 1 | ROM Security Bit 2<br>0 = enable security<br>1 = disable security |

**Security Bit 1:** When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. $\overline{EA}$ is latched on Reset.

**Security Bit 2:** When programmed, this bit inhibits Verify User ROM.

**NOTE:** Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1: ☐ Enabled ☐ Disabled

Security Bit #2: ☐ Enabled ☐ Disabled

Encryption: ☐ No ☐ Yes If Yes, must send key file.

## ROM CODE SUBMISSION FOR 64K ROM DEVICE (83C51RD+)

When submitting ROM code for the 64K ROM devices, the following must be specified:

1. 64k byte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

| ADDRESS | CONTENT | BIT(S) | COMMENT |
|---|---|---|---|
| 0000H to FFFFH | DATA | 7:0 | User ROM Data |
| 10000H to 1003FH | KEY | 7:0 | ROM Encryption Key<br>FFH = no encryption |
| 10040H | SEC | 0 | ROM Security Bit 1<br>0 = enable security<br>1 = disable security |
| 10040H | SEC | 1 | ROM Security Bit 2<br>0 = enable security<br>1 = disable security |

**Security Bit 1:** When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. $\overline{EA}$ is latched on Reset.

**Security Bit 2:** When programmed, this bit inhibits Verify User ROM.

**NOTE:** Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

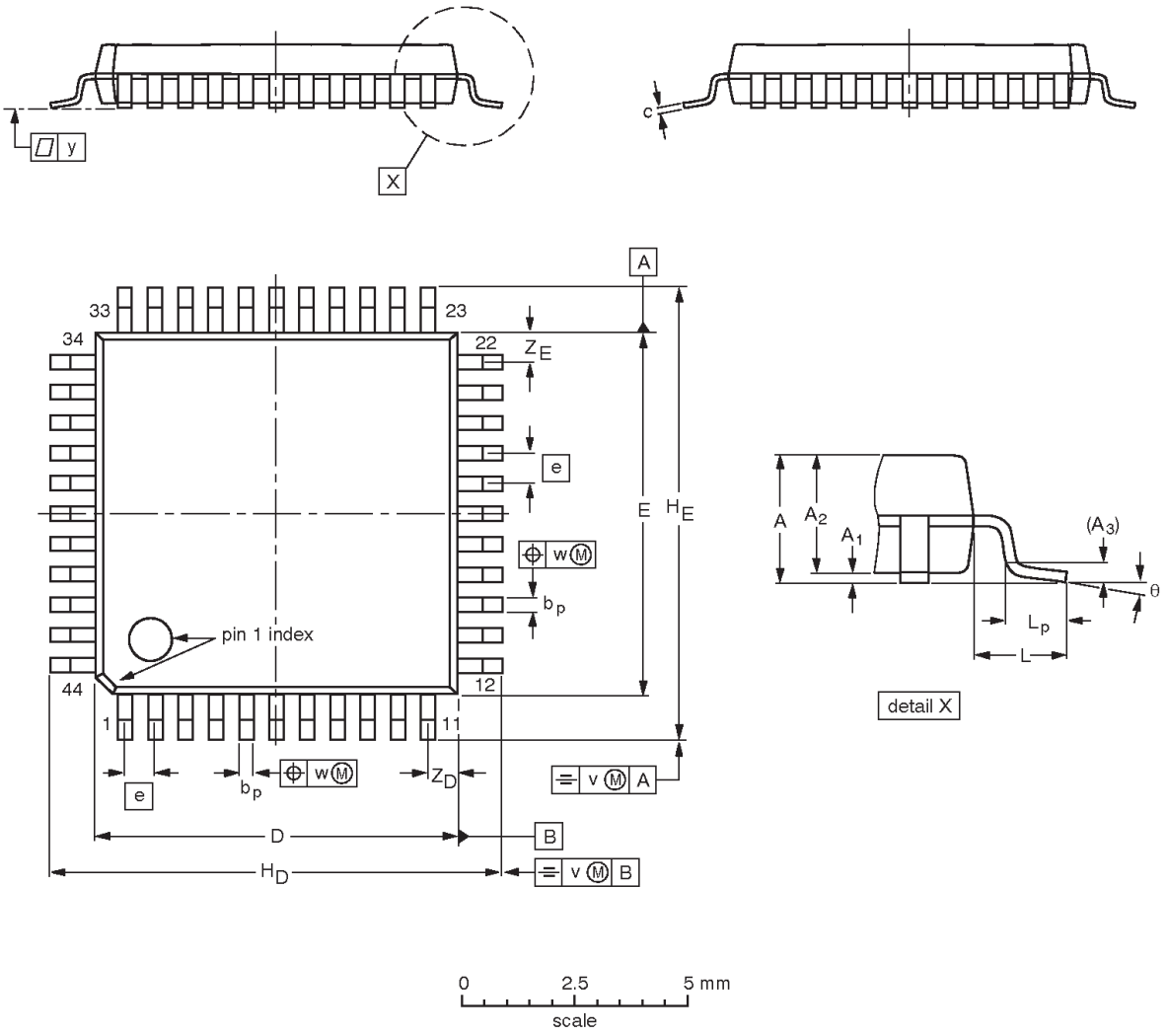
For each of the following, check the appropriate box, and send to Philips along with the code:

Security Bit #1: ☐ Enabled ☐ Disabled

Security Bit #2: ☐ Enabled ☐ Disabled

Encryption: ☐ No ☐ Yes If Yes, must send

## QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.10 | 0.25<br>0.05 | 1.85<br>1.65 | 0.25 | 0.40<br>0.20 | 0.25<br>0.14 | 10.1<br>9.9 | 10.1<br>9.9 | 0.8 | 12.9<br>12.3 | 12.9<br>12.3 | 1.3 | 0.95<br>0.55 | 0.15 | 0.15 | 0.1 | 1.2<br>0.8 | 1.2<br>0.8 | $10^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT307-2 | | | | | | ~~95-02-04~~<br>97-08-01 |