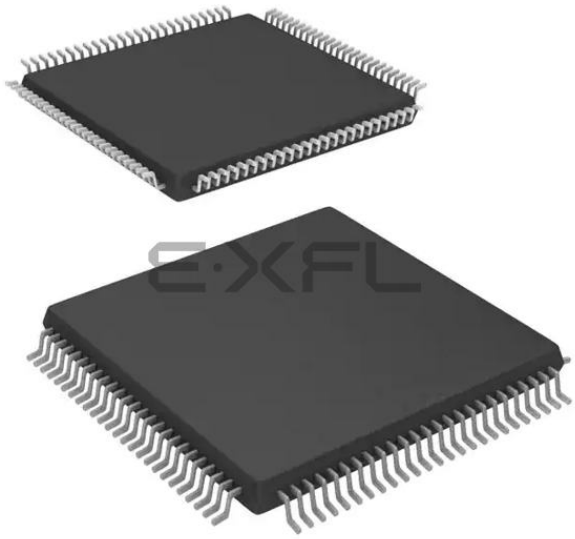


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-1
Core Size	32-Bit Single-Core
Speed	12.5MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417020svx12iv

Table 1 Manual Organization (cont)

Category	Section Title	Abbreviation	Contents
Pins	14. Pin Function Controller	PFC	Pin function selection
	15. Parallel I/O Ports	I/O	I/O port
Memory	16. ROM	ROM	On-chip ROM
	17. RAM	RAM	On-chip RAM
Power-Down States	18. Power-Down States	—	Sleep mode, standby mode
Electrical Characteristics	19. Electrical Characteristics	—	Absolute maximum ratings, AC characteristics, DC characteristics, operation timing

6.5.3 Instruction Fetch Break

If a break is attempted at the task A return destination instruction fetch, task B is activated before the UBC interrupt by interrupt B generated during task A processing, and the UBC interrupt is handled after the interrupt B exception handling.

(1) Cause

The SH7032/SH7034 chip operates as follows.

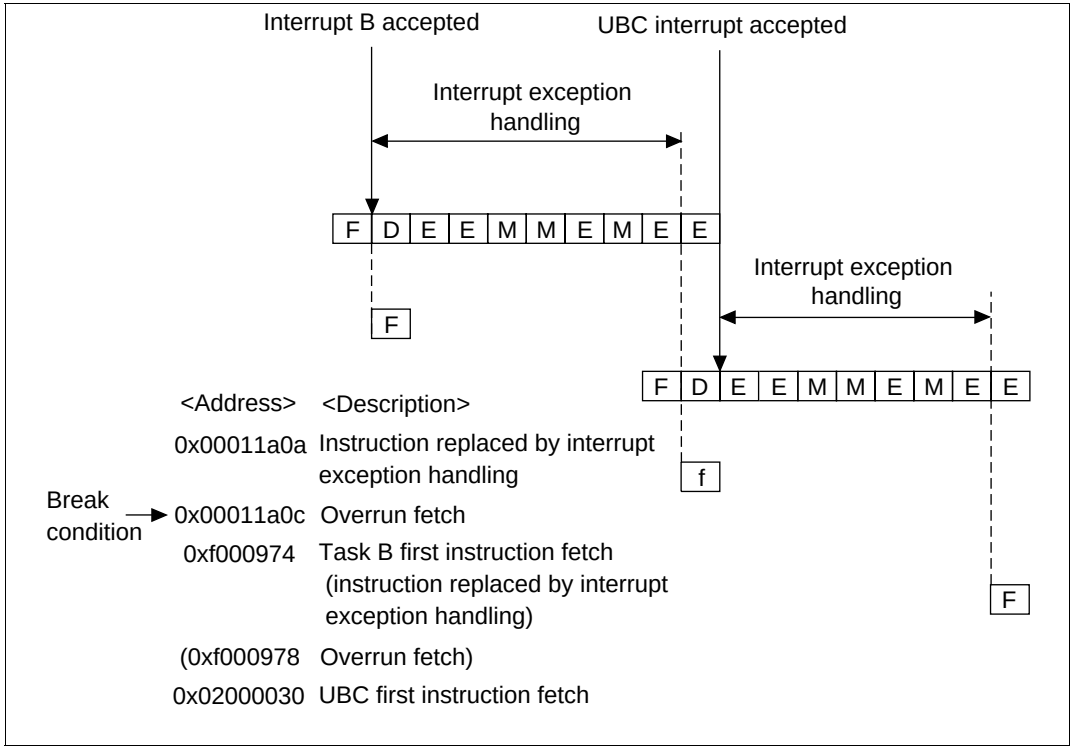


Figure 6.3 UBC Operation

It actually takes at least two cycles for the UBC interrupt generated by the address 0x00011a0c instruction fetch cycle to be sent to the interrupt controller and interrupt exception handling to begin. However, as shown in figure 6.3, when the UBC interrupt is generated, previously generated interrupt B initiated by task B is accepted first, and the UBC interrupt is accepted after completion of the interrupt B exception handling.

(2) Remedy

There is no way of preventing this operation by hardware. A software solution, such as the use of a flag, must be employed.

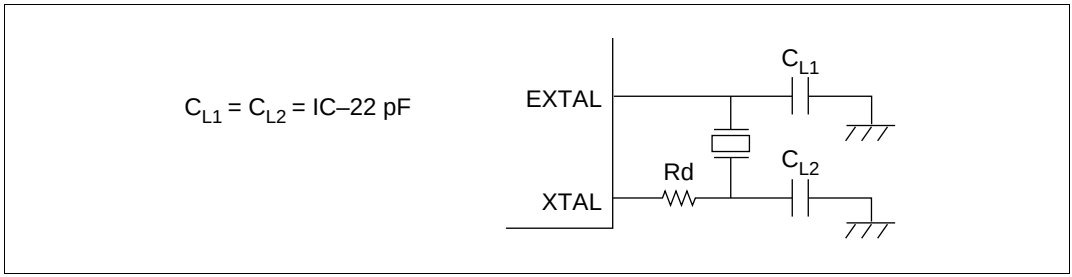


Figure 7.2 Connection of the Crystal Resonator (Example)

Table 7.1 Damping Resistance

Frequency [MHz]	2	4	8	12	16	20
Rd [Ω]	1k	500	200	0	0	0

Crystal Resonator: Figure 7.3 shows an equivalent circuit of the crystal resonator. Use a crystal resonator with the characteristics listed in table 7.2.

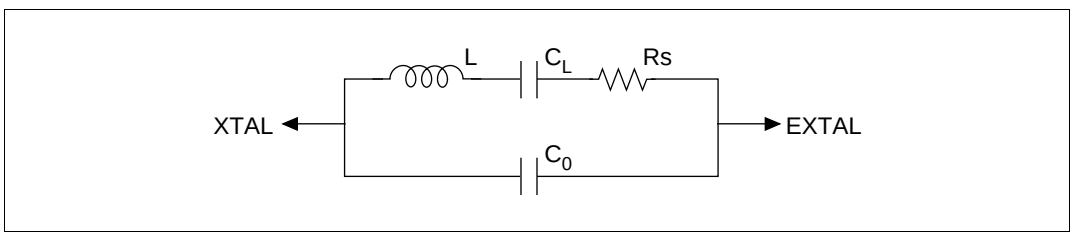


Figure 7.3 Crystal Resonator Equivalent Circuit

Table 7.2 Crystal Resonator Parameters

	Frequency (MHz)					
Parameter	**2**	**4**	**8**	**12**	**16**	**20**
Rs max [Ω]	500	120	80	60	50	40
Co max [pF]	7	7	7	7	7	7

Value to be determined (TBD)

7.2.2 External Clock Input

An external clock signal can be input at the EXTAL pin as shown in figure 7.6. The XTAL pin should be left open. The frequency must be equal to the system clock (CK) frequency. The specifications for the waveform of the external clock input are given below. Make the external clock frequency the same as the system clock (CK).

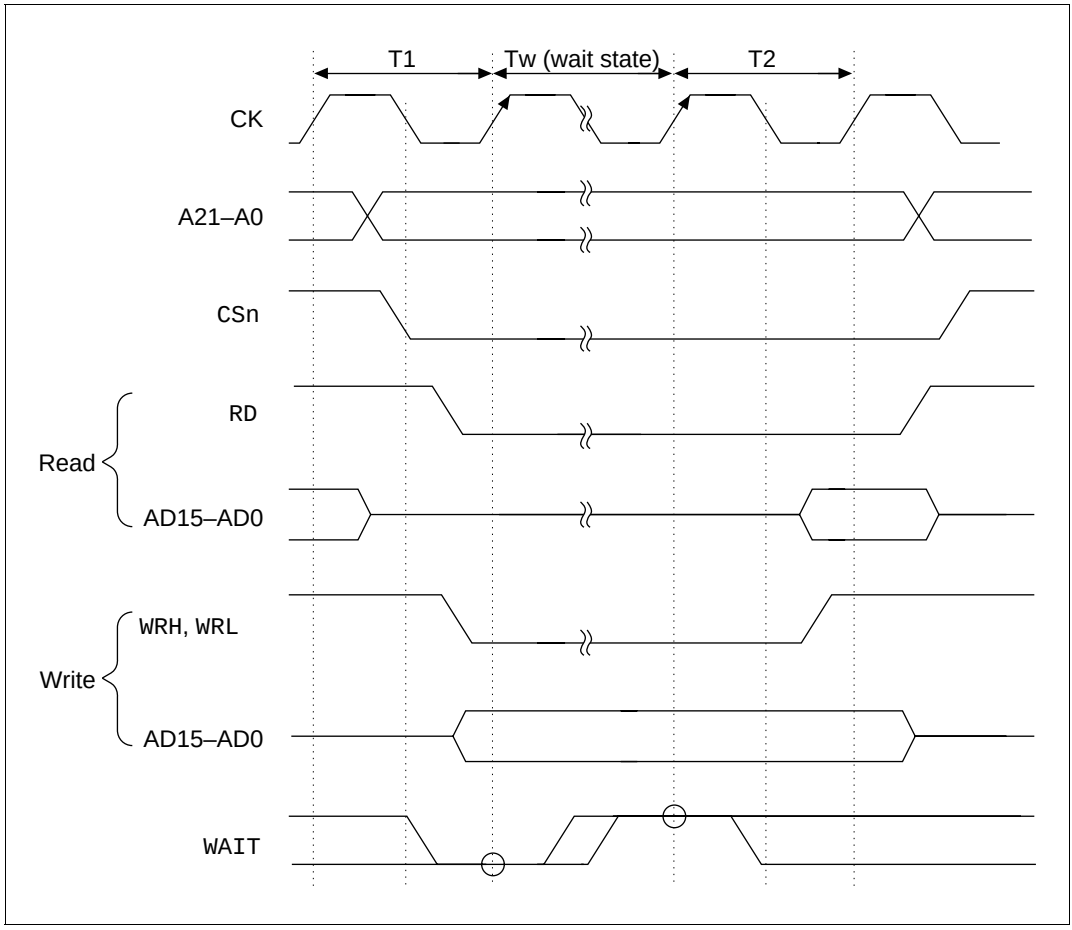
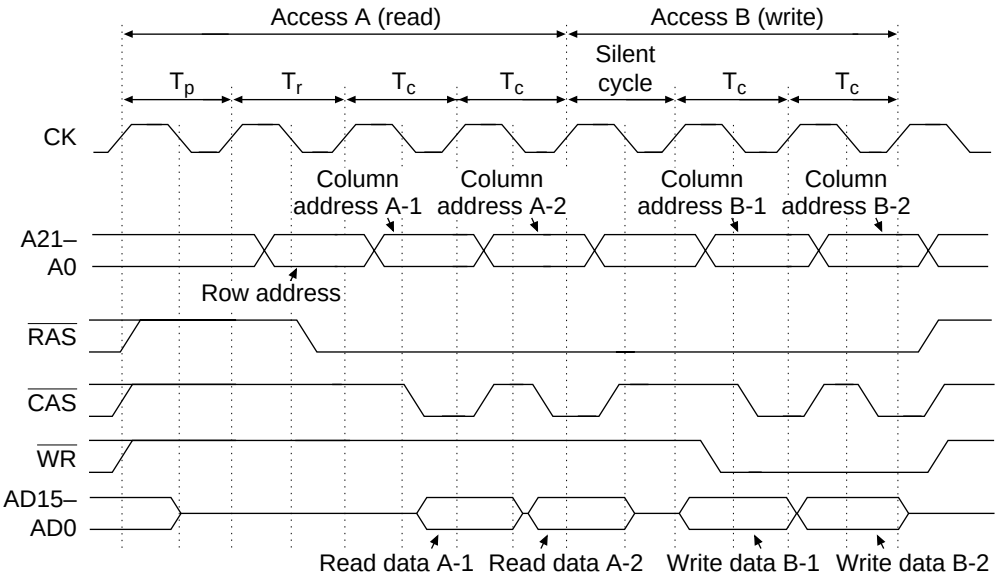


Figure 8.13 Wait State Timing for External Memory Space Access (2 states plus wait states from $\overline{\text{WAIT}}$ signal)

Areas 0, 2 and 6 have long wait functions. When the corresponding bits in WCR1 and WCR2 are cleared to 0, the access cycle is 1 state plus the number of long wait states (set in WCR3, selectable between 1 and 4) and the $\overline{\text{WAIT}}$ pin input signal is not sampled. When the bits are set to 1, the $\overline{\text{WAIT}}$ signal is sampled and the number of states is 1 plus the number of long wait states plus the number of wait states in the $\overline{\text{WAIT}}$ signal. The $\overline{\text{WAIT}}$ signal is sampled at the rise of the system clock (CK) directly preceding the last long wait state and the wait states are inserted as long as the level is low. When a high level is detected, it shifts to the final long wait state. Figure 8.14 shows the wait state timing when accessing the external memory spaces of areas 0, 2, and 6.



Note: Access A and B are examples of 32-bit data accesses in their respective 16-bit bus width spaces.

Figure 8.25 Short Pitch High-Speed Page Mode (When read and write cycle continues with the same row address)

The high-level duty of the $\overline{CAS}$ signal can be selected in the short pitch high-speed page mode using the CAS duty bit (CDTY) in the DCR. When the CDTY bit is cleared to 0, high-level duty is 50% of the TC state; when CDTY is set to 1, it is 35% of the T_C state.

- Long-pitch, high-speed page mode: When the RW1, WW1, DRW1, and DWW1 bits in WCR1 and WCR2 are set to 1, and the corresponding DRAM access cycle is continuing, the $\overline{CAS}$ signal and column address output cycles (2 states) continue as long as the row addresses continue to match. When the $\overline{WAIT}$ signal is detected at the low level, the second cycle of the column address output cycle is repeated as the wait state. Figure 8.26 shows the timing for the long pitch high-speed page mode. See section 20.3.3, Bus Timing, for more information about the timing.

8.7 Parity Check and Generation

The BSC can check and generate parity for data input and output to or from in the DRAM space of area 1 and the external memory space of area 2.

To check and generate parity, select the space (DRAM space only, or DRAM space and area 2) for which parity is to be checked and generated using the parity check enable bits (PCHK1 and PCHK0) of the parity control register and select odd or even parity in the parity polarity bit (PEO).

When data is input from the space selected in the PCHK1 and PCHK0 bits, the BSC checks the PEO bit to see if the polarity of the DPH pin input (upper byte parity data) is accurate for the AD15–AD8 pin input (upper byte data) or if the DPL pin input (lower byte parity data) is accurate for the AD7–AD0 pin input (lower byte data). If the check indicates that either the upper or lower byte parity is incorrect, a parity error interrupt is produced (PEI).

When outputting data to the space selected in the PCHK1 and PCHK0 bits, the BSC outputs parity data output of the polarity set in the PEO bit from the DPH pin for the AD15–AD8 pin output (upper byte data) or from the DPL pin for the AD7–AD0 pin input (lower byte data) using the same timing as the data output.

The BSC is also able to force a parity output for use in testing the system's parity error check function. When the parity force output bit (PFRC) of the PCR is set to 1, a high level is forcibly output from the DPH and DPL pins when data is output to the space selected in the PCHK1 and PCHK0 bits.

8.8 Warp Mode

In warp mode, an external write cycle or DMA single address mode transfer cycle and an internal access cycle (read/write to on-chip memory or on-chip peripheral modules) operate independently in parallel. The warp mode is entered by setting the warp mode bit (WARP) in the BCR to 1. This allows the LSI to be operated at high speed.

When in the warp mode an external write cycle or DMA single address mode transfer cycle continues for at least 2 states and their is an internal access, only the external write cycle will be performed in the initial state. The external write cycle and internal access cycle will be performed in parallel from the next state on, without waiting for the end of the external write cycle. Figure 8.34 shows the timing when an access to an on-chip peripheral module and an external write cycle are performed in parallel.

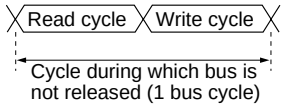


Figure 8.45 TAS Instruction Read Cycle and Write Cycle

(c) Refresh cycle + bus cycle

The bus is never released during a refresh cycle and the following bus cycle ((a) or (b) above)) (figure 8.46).

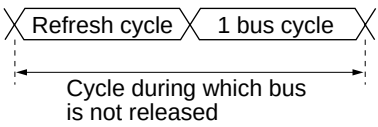


Figure 8.46 Refresh Cycle and Following Bus Cycle

9.2 Register Descriptions

9.2.1 DMA Source Address Registers 0–3 (SAR0–SAR3)

DMA source address registers 0–3 (SAR0–SAR3) are 32-bit read/write registers that specify the source address of a DMA transfer. During a DMA transfer, these registers indicate the next source address (in single-address mode, SAR is ignored in transfers from external devices with DACK to memory-mapped external devices or external memory).

The initial value after resets or in standby mode is undefined.

Bit:	31	30	29	28	27	26	25	24
Bit name:								
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	23	22	21	20	…	0
Bit name:					…	
Initial value:	—	—	—	—	…	—
R/W:	R/W	R/W	R/W	R/W	…	R/W

9.2.2 DMA Destination Address Registers 0–3 (DAR0–DAR3)

DMA destination address registers 0–3 (DAR0–DAR3) are 32-bit read/write registers that specify the destination address of a DMA transfer. During a DMA transfer, these registers indicate the next destination address (in single-address mode, DAR is ignored in transfers from memory-mapped external devices or external memory to external devices with DACK). The initial value after resets or in standby mode is undefined.

Bit:	31	30	29	28	27	26	25	24
Bit name:								
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	23	22	21	20	…	0
Bit name:					…	
Initial value:	—	—	—	—	…	—
R/W:	R/W	R/W	R/W	R/W	…	R/W

9.4.2 Example of DMA Transfer between On-Chip SCI and External Memory

In this example, receive data of on-chip serial communications interface (SCI) channel 0 is transferred to external memory using DMAC channel 3. Table 9.8 shows the transfer conditions and register settings.

Table 9.8 Transfer Conditions and Register Settings for Transfer between On-Chip SCI and External Memory

Transfer Conditions	Register	Setting
Transfer source: RDR0 of on-chip SCI0	SAR3	H'FFFFEC5
Transfer destination: external memory	DAR3	Destination address
Number of transfers: 64	TCR3	H'0040
Transfer destination address: incremented	CHCR3	H'4405
Transfer source address: fixed		
Transfer request source (transfer request signal): SCI0 (RXI0)		
Bus mode: cycle steal		
Transfer unit: byte		
DEI interrupt request generated at end of transfer (channel 3 enabled for transfer		
Channel priority order: fixed (0 > 3 > 2 > 1) (all channels transfer enabled)	DMAOR	H'0001

- Bit 3 (PWM Mode 3 (PWM3)): PWM3 selects the PWM mode for channel 3. When the PWM3 bit is set to 1 and the PWM mode entered, the TIOCA3 pin becomes a PWM output pin. 1 is output on a compare match of general register A3 (GRA3); 0 is output on a compare match of general register B3 (GRB3). When the complementary PWM mode or reset-synchronized PWM mode are set by the CMD1 and CMD0 bits of the timer function control register (TFCR), the setting of this bit is ignored in favor of the settings of CMD1 and CMD0.

Bit 3: PWM3	Description
0	Channel 3 operates normally (initial value)
1	Channel 3 operates in PWM mode

- Bit 2 (PWM Mode 2 (PWM2)): PWM2 selects the PWM mode for channel 2. When the PWM2 bit is set to 1 and the PWM mode entered, the TIOCA2 pin becomes a PWM output pin. 1 is output on a compare match of general register A2 (GRA2); 0 is output on a compare match of general register B2 (GRB2).

Bit 2: PWM2	Description
0	Channel 2 operates normally (initial value)
1	Channel 2 operates in PWM mode

- Bit 1 (PWM Mode 1 (PWM1)): PWM1 selects the PWM mode for channel 1. When the PWM1 bit is set to 1 and the PWM mode entered, the TIOCA1 pin becomes a PWM output pin. 1 is output on a compare match of general register A1 (GRA1); 0 is output on a compare match of general register B1 (GRB1).

Bit 1: PWM1	Description
0	Channel 1 operates normally (initial value)
1	Channel 1 operates in PWM mode

- Bit 0 (PWM Mode 0 (PWM0)): PWM0 selects the PWM mode for channel 0. When the PWM0 bit is set to 1 and the PWM mode entered, the TIOCA0 pin becomes a PWM output pin. 1 is output on a compare match of general register A0 (GRA0); 0 is output on a compare match of general register B0 (GRB0).

Bit 0: PWM0	Description
0	Channel 0 operates normally (initial value)
1	Channel 0 operates in PWM mode

Bit 2: TPSC2	Bit 1: TPSC1	Bit 0: TPSC0	Counter Clock (and cycle when ϕ = 10 MHz)
0	0	0	Internal clock ϕ (initial value)
		1	Internal clock ϕ/2
	1	0	Internal clock ϕ/4
		1	Internal clock ϕ/8
1	0	0	External clock A (TCLKA)
		1	External clock B (TCLKB)
	1	0	External clock C (TCLKC)
		1	External clock D (TCLKD)

10.2.10 Timer I/O Control Register (TIOR)

The timer I/O control register (TIOR) is an eight-bit read/write register that selects the output compare or input capture function for the general registers GRA and GRB. It also selects the function of the TIOCA and TIOCB pins. If output compare is selected, the TIOR also selects the output settings. If input capture is selected, the TIOR also select the input capture edges. TIOR is initialized to H'88 or H'08 on a reset or standby mode. Each ITU channel has one TIOR (table 10.8).

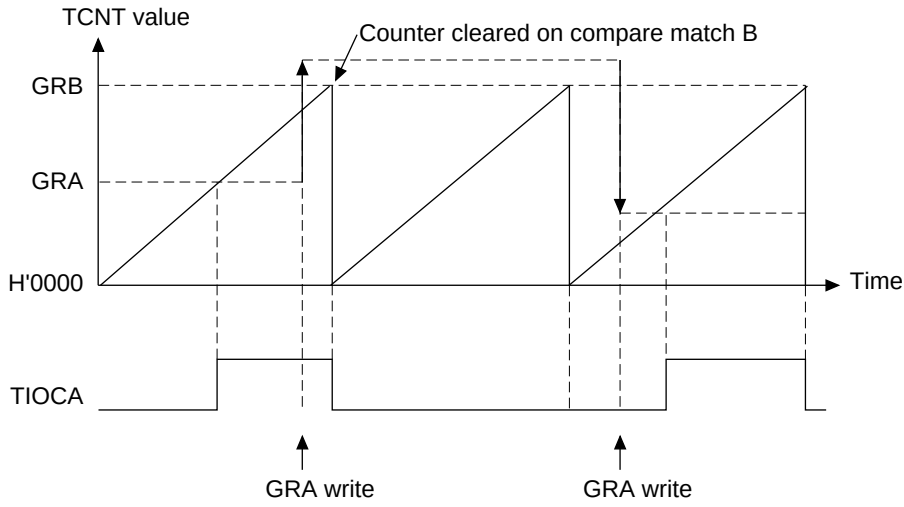
Table 10.8 Timer I/O Control Register (TIOR)

Channel	Abbre-viation	Function
0	TIOR0	The TIOR controls the GRs. Some functions vary during PWM. When channels 3 and 4 are set for complementary PWM mode/reset-synchronized PWM mode, TIOR3 and TIOR4 settings are not valid.
1	TIOR1	
2	TIOR2	
3	TIOR3	
4	TIOR4	

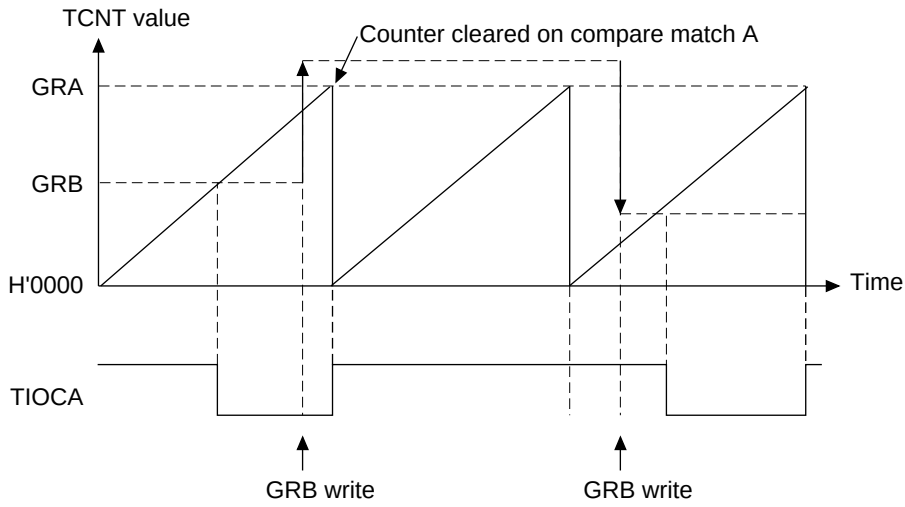
Bit:	7	6	5	4	3	2	1	0
Bit name:	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
Initial value:	*	0	0	0	1	0	0	0
R/W:	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Note: Undefined

- Bit 7 (reserved): Bit 7 is read as undefined. The write value should be 0 or 1.



a. 0% duty



b. 100% duty

Figure 10.30 PWM Mode Operation Example 2

10.6.2 Contention between TCNT Word Write and Increment

If an increment pulse occurs in the T3 state of a TCNT word write cycle, writing takes priority and the TCNT is not incremented. The timing is shown in figure 10.59.

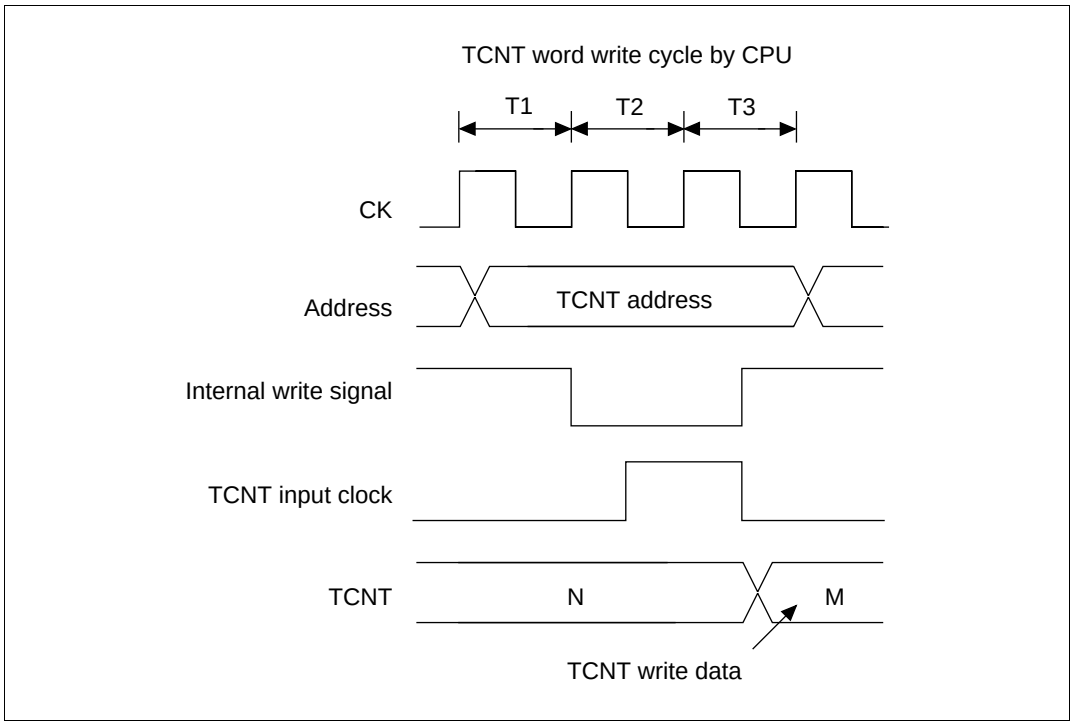


Figure 10.59 Contention between TCNT Word Write and Increment

Section 11 Programmable Timing Pattern Controller (TPC)

11.1 Overview

The SuperH microcomputer has a built-in programmable timing pattern controller (TPC). The TPC can provide pulse outputs by using the 16-bit integrated-timer pulse unit (ITU) as a time base. The TPC pulse outputs are divided into 4-bit groups 3–0. These can operate simultaneously, or independently.

11.1.1 Features

Features of the programmable timing pattern controller are listed below.

- 16-bit output data: Maximum 16-bit data can be output. TPC output can be enabled on a bit-by-bit basis.
- Four output groups: Output trigger signals can be selected in 4-bit groups to provide up to four different 4-bit outputs.
- Selectable output trigger signals: Output trigger signals can be selected by group from the
- 4-channel compare-match signals of the 16-bit integrated-timer pulse unit (ITU).
- Non-overlap mode: A non-overlap interval can be set to come between multiple pulse outputs.
- Can connect to DMA controller: The compare-match signals selected as output trigger signals can activate the DMA controller for sequential output of data without CPU intervention.

Bit:	7	6	5	4	3	2	1	0
Bit name:	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 7–0 (next data enable 7–0 (NDER7–NDER0)): NDER7–NDER0 select enable/disable for TPC output groups 1 and 0 (TP7–TP0) in bit units.

Bit 7–0: NDER7–NDER0	Description
0	Disables TPC outputs TP7–TP0 (transfer from NDR7–NDR0 to PB7–PB0 is disabled) (initial value)
1	Enables TPC outputs TP7–TP0 (transfer from NDR7–NDR0 to PB7–PB0 is enabled)

11.2.6 Next Data Enable Register B (NDERB)

NDERB is an eight-bit read/write register that enables TPC output groups 3 and 2 (TP15–TP8) on a bit-by-bit basis.

When the bits enabled for TPC output by NDERB generate the ITU compare match selected in the TPC output control register, the value of the next data register B (NDRB) is automatically transferred to the corresponding PBDR bits and the output value is updated. For disabled bits, there is no transfer and the output value does not change. When reset, NDERB is initialized to H'00. It is not initialized by standby mode.

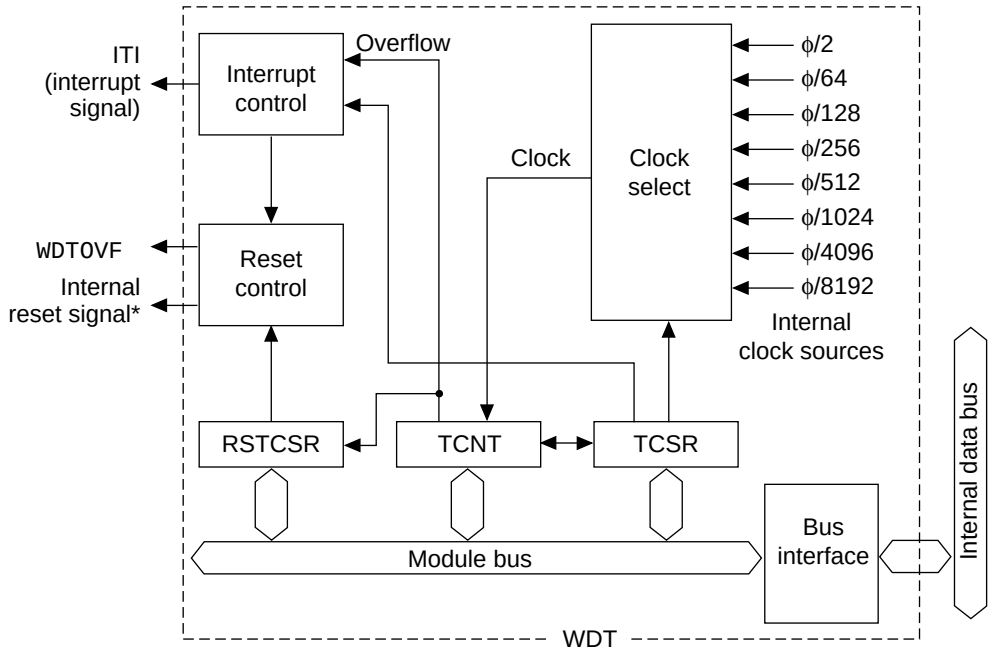
Bit:	7	6	5	4	3	2	1	0
Bit name:	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 7–0 (next data enable 15–8 (NDER15–NDER8)): NDER15–NDER8 select enable/disable for TPC output groups 3 and 2 (TP15–TP8) in bit units.

Bit 7–0: NDER15–NDER8	Description
0	Disables TPC outputs TP15–TP8 (transfer from NDR15–NDR8 to PB15–PB8 is disabled) (initial value)
1	Enables TPC outputs TP15–TP8 (transfer from NDR15–NDR8 to PB15–PB8 is enabled)

12.1.2 Block Diagram

Figure 12.1 is the block diagram of the WDT.



TCSR: Timer control/status register

TCNT: Timer counter

RSTCSR: Reset control/status register

Note: The internal reset signal can be generated by setting the register. The type of reset can be selected (power-on or manual resets).

Figure 12.1 WDT Block Diagram

12.1.3 Pin Configuration

Table 12.1 shows the pin configuration.

12.3.4 Timing of Setting the Overflow Flag (OVF)

In the interval timer mode, when the TCNT overflows the OVF flag is set to 1 and an interval timer interrupt is requested (figure 12.6).

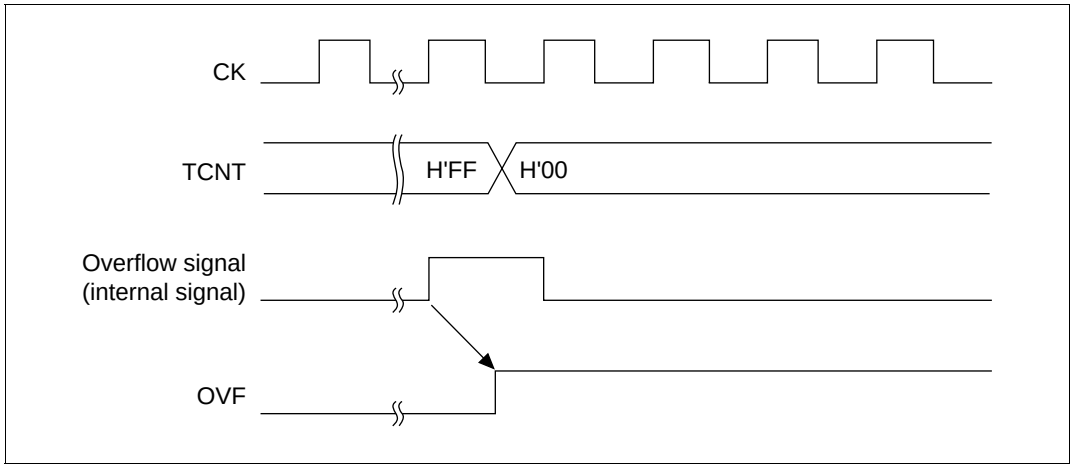


Figure 12.6 Timing of Setting the OVF

12.3.5 Timing of Setting the Watchdog Timer Overflow Flag (WOVF)

When the TCNT overflows the WOVF bit of the RSTCSR is set to 1 and a $\overline{\text{WDTOVF}}$ signal is output. When the RSTE bit is set to 1, TCNT overflow enables an internal reset signal to be generated for the entire chip (figure 12.7).

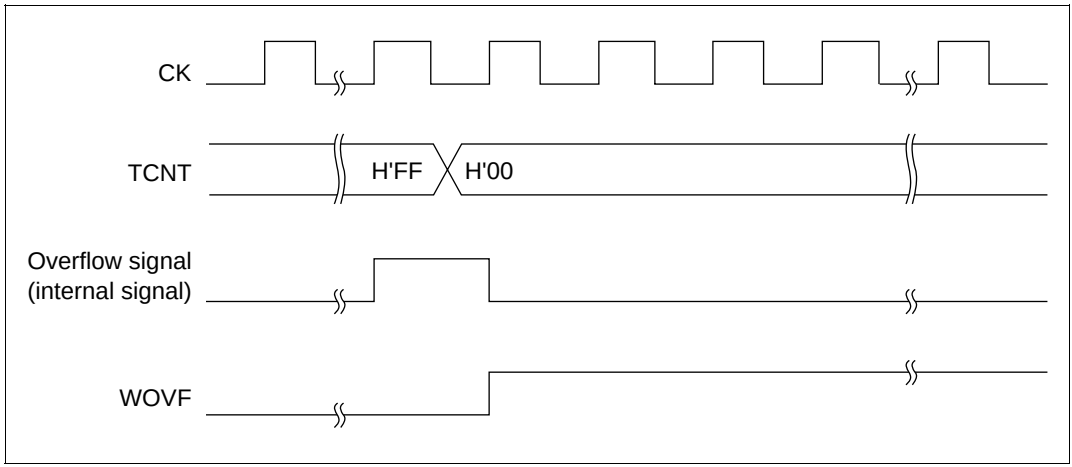


Figure 12.7 Timing of Setting the WOVF Bit and Internal Reset

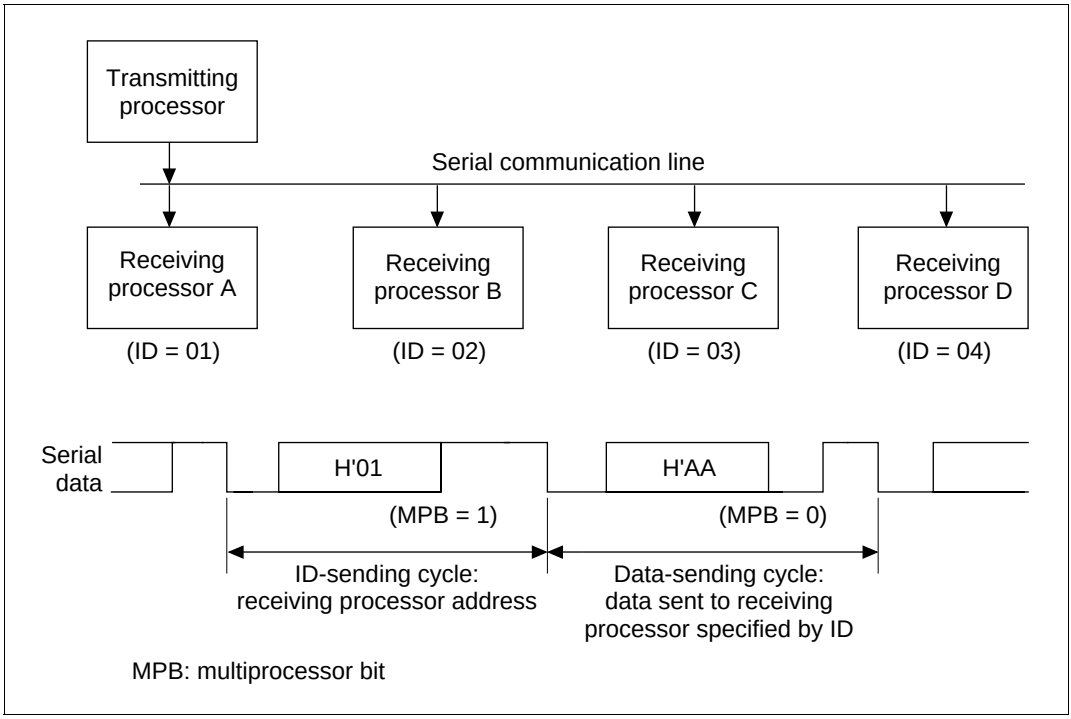


Figure 13.9 Example of Communication among Processors Using Multiprocessor Format (sending data H'AA to receiving processor A)

Communication Formats: Four formats are available. Parity-bit settings are ignored when the multiprocessor format is selected. For details see table 13.8.

Clock: See the description in the asynchronous mode section.

Transmitting Multiprocessor Serial Data: Figure 13.10 shows a sample flowchart for transmitting multiprocessor serial data. The procedure for transmitting multiprocessor serial data is listed below.

1. SCI initialization: select the TxD pin function with the PFC.
2. SCI status check and transmit data write: read the serial status register (SSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (TDR). Also set MPBT (multiprocessor bit transfer) to 0 or 1 in SSR. Finally, clear TDRE to 0.
3. To continue transmitting serial data: read the TDRE bit to check whether it is safe to write (1); if so, write data in TDR, then clear TDRE to 0. When the DMAC is started by a transmit-data-empty interrupt request (TXI) to write data in TDR, the TDRE bit is checked and cleared automatically.
4. To output a break signal at the end of serial transmission: set the DR bit to 0 (I/O data port register), then clear TE to 0 in SCR and set the TxD pin function as output port with the PFC.

18.1.2 Register

Table 18.2 summarizes the register related to the power-down state.

Table 18.2 Standby Control Register (SBYCR)

Name	Abbreviation	R/W	Initial Value	Address	Access size
Standby control register	SBYCR	R/W	H'1F	H'5FFFFBC	8, 16, 32

18.2 Standby Control Register (SBYCR)

The standby control register (SBYCR) is an 8-bit register that can be read or written to. It is set in order to enter the standby mode and also sets the port states in standby mode. The SBYCR is initialized to H'1F when reset.

Bit:	7	6	5	4	3	2	1	0
Bit name:	SBY	HIZ	—	—	—	—	—	—
Initial value:	0	0	0	1	1	1	1	1
R/W:	R/W	R/W	—	—	—	—	—	—

- Bit 7 (standby (SBY)): SBY enables transition to the standby mode. The SBY bit cannot be set to 1 while the timer enable bit (bit TME) in timer control/status register TCSR of watchdog timer WDT is set to 1. To enter the standby mode, clear the TME bit to 0 to halt the WDT and set the SBY bit.

SBY	Description
0	Executing SLEEP instruction puts the LSI into sleep mode (initial value)
1	Executing SLEEP instruction puts the LSI into standby mode

- Bit 6 (port high-impedance (HIZ)): HIZ selects whether I/O ports remain in their previous states during standby, or are placed in the high-impedance state when the standby mode is entered. The HIZ bit cannot be set to 1 while the TME bit is set to 1. To place the pins of the I/O ports in high impedance, clear the TME bit to 0 before setting the HIZ bit.

HIZ	Description
0	Port states are maintained during standby (initial value)
1	Ports are placed in the high-impedance state in standby

19.3 AC Characteristics

The following AC timing chart represents the AC characteristics, not signal functions. For signal functions, see the explanation in the text.

19.3.1 Clock Timing

Table 19.4 Clock Timing

Case A: V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +75°C*
Case B: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, Ta = –20 to +75°C*

*: Normal products. Ta = –40 to +85°C for wide-temperature range products.

		Case A		Case B					
		12.5 MHz		16.6 MHz		20 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Figures
EXTAL input high level pulse width	t_{EXH}	20	—	10	—	10	—	ns	19.1
EXTAL input low level pulse width	t_{EXL}	20	—	10	—	10	—	ns	
EXTAL input rise time	t_{EXr}	—	10	—	5	—	5	ns	
EXTAL input fall time	t_{EXf}	—	10	—	5	—	5	ns	
Clock cycle time	t_{cyc}	80	—	60	500	50	500	ns	19.1, 19.2
Clock high pulse width	t_{CH}	30	—	20	—	20	—	ns	19.2
Clock low pulse width	t_{CL}	30	—	20	—	20	—	ns	
Clock rise time	t_{Cr}	—	10	—	5	—	5	ns	
Clock fall time	t_{Cf}	—	10	—	5	—	5	ns	
Reset oscillation settling time	t_{OSC1}	10	—	10	—	10	—	ms	19.3
Software standby oscillation settling time	t_{OSC2}	10	—	10	—	10	—	ms	