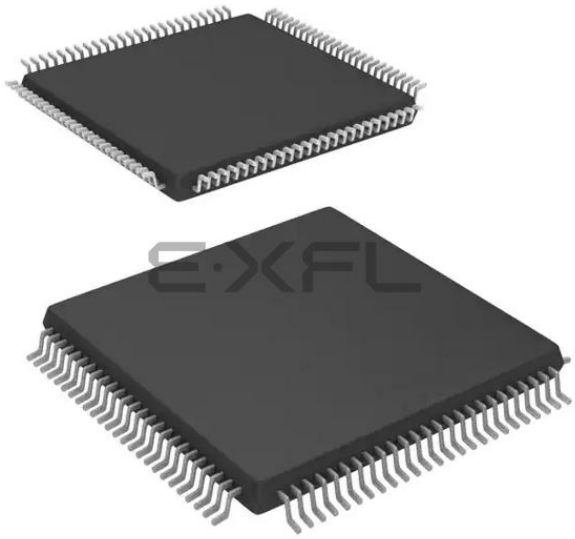


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-1
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417020sx20iv

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

Table 1.3 Pin Functions (cont)

Type	Symbol	Pin No.	I/O	Name and Function
Bus control (cont)	RAS	52	O	Row address strobe: DRAM row-address strobe-timing signal.
	CASH	47	O	Column address strobe high: DRAM column-address strobe-timing signal outputs low level to access the upper eight data bits.
	CASL	49	O	Column address strobe low: DRAM column-address strobe-timing signal outputs low level to access the lower eight data bits.
	RD	57	O	Read: Indicates reading of data from an external device.
	WRH	56	O	Upper write: Indicates write access to the upper eight bits of an external device.
	WRL	55	O	Lower write: Indicates write access to the lower eight bits of an external device.
	CS0–CS7	46–49, 51–54	O	Chip select 0–7: Chip select signals for accessing external memory and devices.
	AH	61	O	Address hold: Address hold timing signal for a device using a multiplexed address/data bus.
	HBS, LBS	20, 56	O	Upper/lower byte strobe: Upper and lower byte strobe signals. (Also used as WRH and A0.)
	WR	55	O	Write: Brought low during write access. (Also used as WRL.)
DMAC	DREQ0, DREQ1	66, 68	I	DMA transfer request (channels 0 and 1): Input pins for external DMA transfer requests.
	DACK0, DACK1	65, 67	O	DMA transfer acknowledge (channels 0 and 1): Indicates that DMA transfer is acknowledged.
16-bit integrated-timer pulse unit (ITU)	TIOCA0, TIOCB0	51, 53	I/O	ITU input capture/output compare (channel 0): Input capture or output compare pins.
	TIOCA1, TIOCB1	62, 64	I/O	ITU input capture/output compare (channel 1): Input capture or output compare pins.
	TIOCA2, TIOCB2	83, 84	I/O	ITU input capture/output compare (channel 2): Input capture or output compare pins.
	TIOCA3, TIOCB3	85, 86	I/O	ITU input capture/output compare (channel 3): Input capture or output compare pins.
	TIOCA4, TIOCB4	87, 89	I/O	ITU input capture/output compare (channel 4): Input capture or output compare pins.

Table 4.5 Address Error Sources

Bus Cycle			
Type	**Bus Master**	**Operation**	**Address Error**
Instruction fetch	CPU	Instruction fetch from even address	None (normal)
		Instruction fetch from odd address	Address error
		Instruction fetch from outside on-chip peripheral module space	None (normal)
		Instruction fetch from on-chip peripheral module space	Address error
Data read/write	CPU or DMAC	Access to word data from even address	None (normal)
		Access to word data from odd address	Address error
		Access to long word data aligned on long word boundary	None (normal)
		Access to long word data not aligned on long word boundary	Address error
		Access to word or byte data in on-chip peripheral module space*	None (normal)
		Access to long word data in 16-bit on-chip peripheral module space*	None (normal)
		Access to long word data in 8-bit on-chip peripheral module space*	Address error

Note: See section 8, Bus State Controller, for details on the on-chip peripheral module space.

4.3.2 Address Error Exception Processing

When an address error occurs, address error exception processing starts after both the bus cycle that caused the address error and the instructions that were being executed at that time have been completed. The CPU then:

1. Pushes the SR onto the stack.
2. Pushes the program counter onto the stack. The PC value saved is the top address of the instruction following the last instruction to be executed.
3. Fetches the exception service routine start address from the exception vector table for the address error that occurred and starts program execution from that address. The branch that occurs here is not a delayed branch.

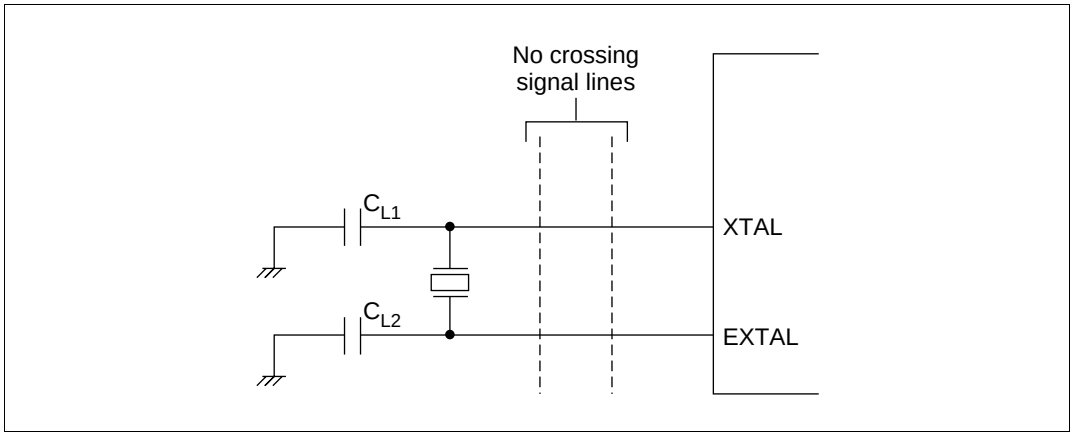


Figure 7.6 Precaution on Oscillator Circuit Board Design

Duty cycle correction circuit: Duty cycle corrections are conducted for an input clock over 5 MHz. Duty cycles may not be corrected if under 5 MHz, but AC characteristics for the high-level pulse width (t_{CH}) and low-level pulse width (t_{CL}) of the clock are satisfied, and the LSI will operate normally. Figure 7.7 shows the standard characteristics of a duty cycle correction.

This duty cycle correction circuit is not for correcting the input clock's transient fluctuations and jutters.

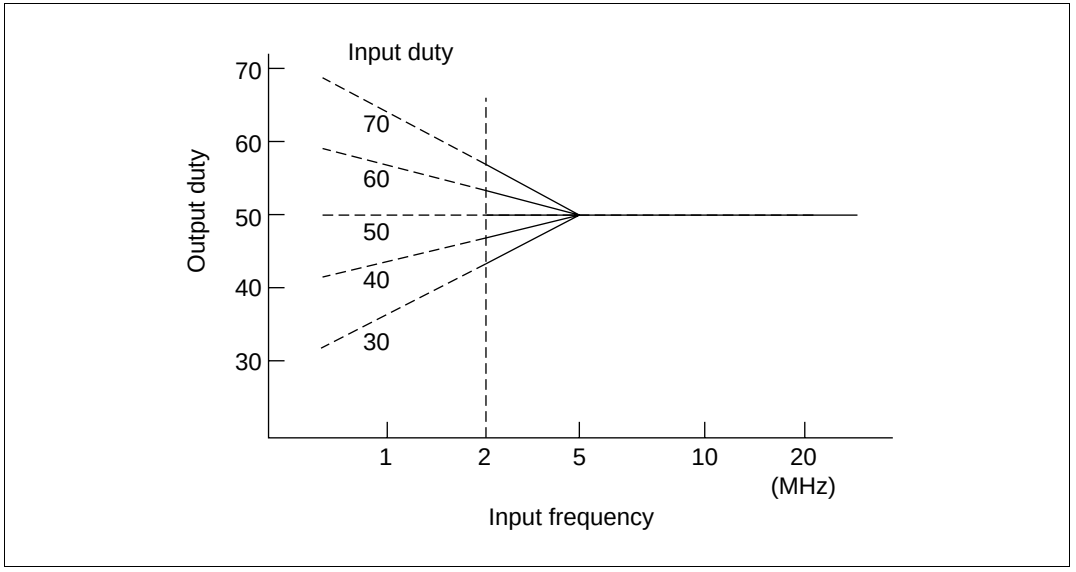


Figure 7.7 Duty Cycle Correction Circuit Standard Characteristics

8.4.3 Byte Access Control

The upper byte and lower byte control signals when 16-bit bus width space is being accessed can be selected from ($\overline{WRH}$, $\overline{WRL}$, A0) or ($\overline{WR}$, $\overline{HBS}$, $\overline{LBS}$). When the byte access select bit (BAS) of the BCR is set to 1, the $\overline{WRH}$, $\overline{WRL}$, and A0 pins output $\overline{WR}$, $\overline{LBS}$ and $\overline{HBS}$ signals. Figure 8.15 illustrates the control signal output timing in the byte write cycle.

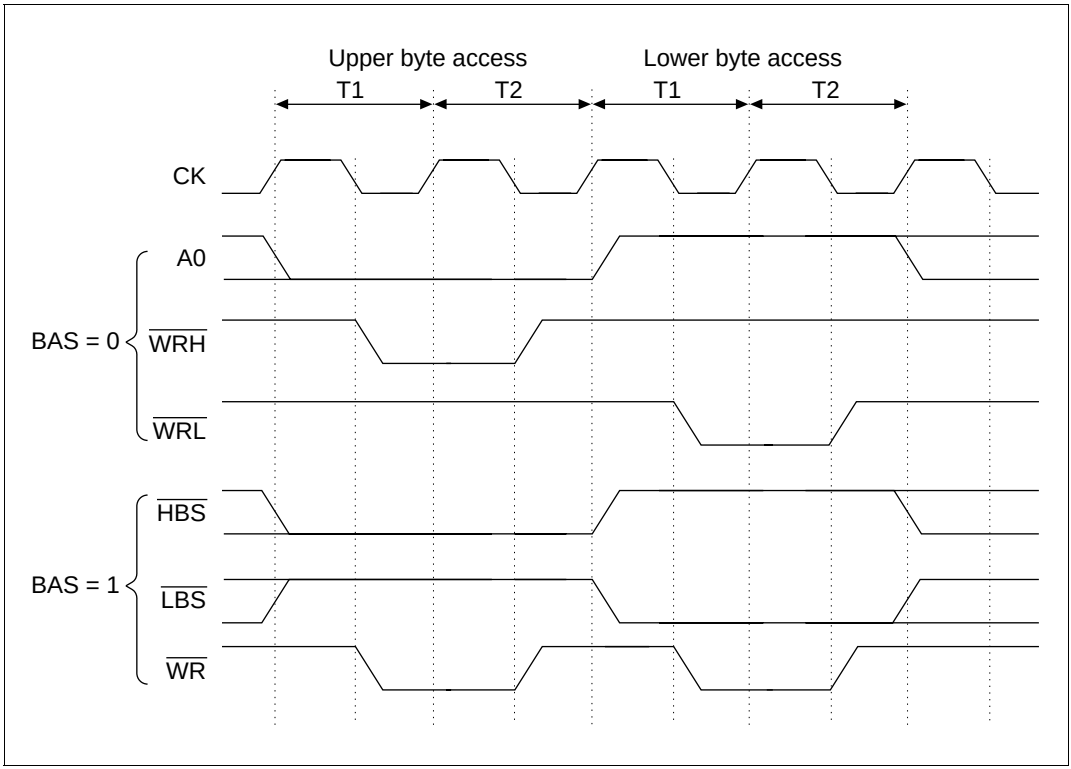


Figure 8.15 Byte Access Control Timing For External Memory Space Access (Write Cycle)

The $\overline{WRH}$, $\overline{WRL}$ system and the $\overline{HBS}$, $\overline{LBS}$ system are available as byte access signals for the 16-bit space in the address/data multiplexing space and the external memory space.

These strobe signals are assigned to pins in the manner: A0/$\overline{HBS}$, $\overline{WRH}$/$\overline{LBS}$, $\overline{WRL}$/$\overline{WR}$, and the BAS bit of the bus control register (BCR) is used to switch specify signal sending.

Note that the byte access signals are strobe signals dedicated to byte access to a 16-bit space and not to be used for byte access to an 8-bit space. When making an access to an 8-bit space, use the A0/$\overline{HBS}$ pin as A0 irrespective of the BAS bit value (0 or 1) to use the $\overline{WRL}$/$\overline{WR}$ pin as the $\overline{WR}$ pin, and avoid using the $\overline{WRH}$/$\overline{LBS}$ pin.

8.5.5 DRAM Burst Mode

In addition to the normal mode of DRAM access, in which row addresses are output at every access and data then accessed (full access), the DRAM also has a high-speed page mode for use when continuously accessing the same row. The high speed page mode enables fast access of data simply by changing the column address after the row address is output (burst mode). Select between full access and burst operation by setting the burst enable bit (BE)) in the DCR. When the BE bit is set to 1, burst operation is performed when the row address matches the previous DRAM access row address. Figure 8.22 shows the comparison of full access and burst operation.

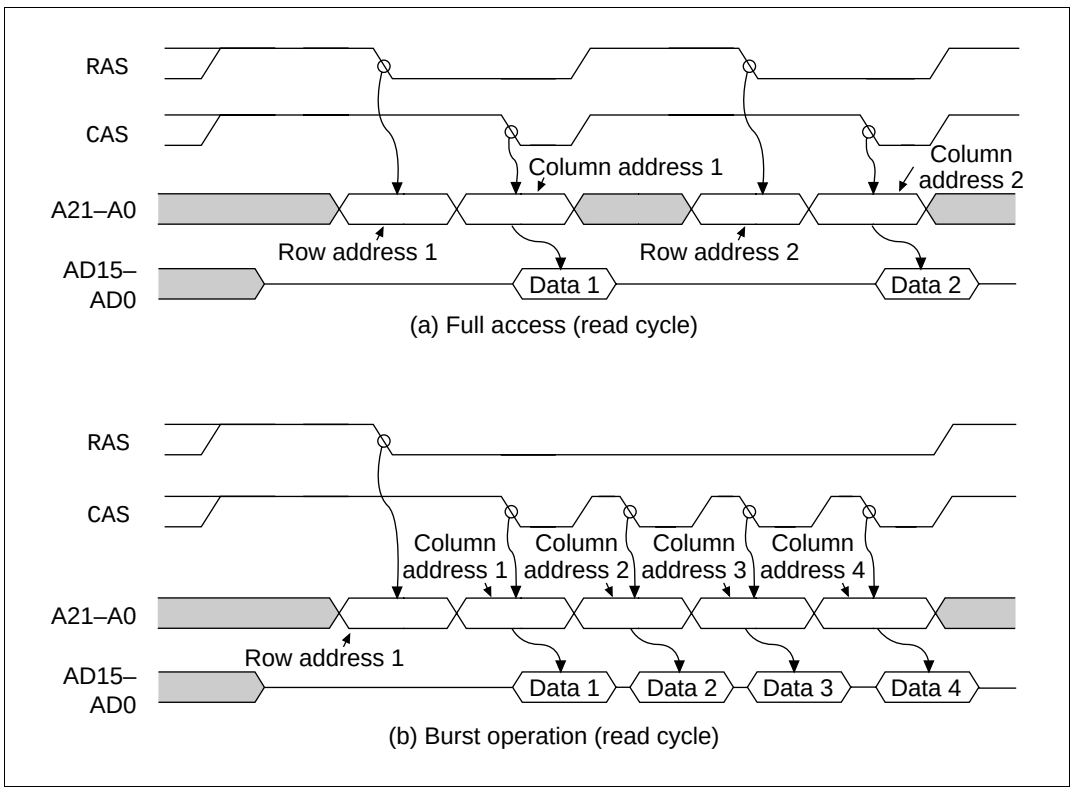


Figure 8.22 Full Access and Burst Operation

Short pitch high-speed page mode or long pitch high-speed page mode burst transfers can be selected independently for DRAM read/write cycles even when the burst operation is selected by using the bits corresponding to area 1 in WCR1 and WCR2 (RW1, WW1, DRW1, DWW1). The RAS down mode or RAS up mode can be selected by setting the RAS down bit (RASD) of the DCR when there is an access outside the DRAM space during burst operation.

Short Pitch High-Speed Page Mode and Long Pitch High-Speed Page Mode: When burst operation is selected by setting the DCR's BE bit to 1, the short pitch high-speed page mode or long pitch high-speed page mode can be selected by setting the RW1, WW1, DRW1, and DWW1 bits of the WCR1 and WCR2.

- Short-pitch, high-speed page mode: When the RW1, WW1, DRW1 and DWW1 bits in the WCR1 and WCR2 are cleared to 0, and the corresponding DRAM access cycle is continuing, the $\overline{CAS}$ signal and column address output cycles continue as long as the row addresses continue to match. The column address output cycle is performed in 1 state and the $\overline{WAIT}$ signal is not sampled. Figure 8.23 shows the read cycle timing for the short pitch high-speed page mode.

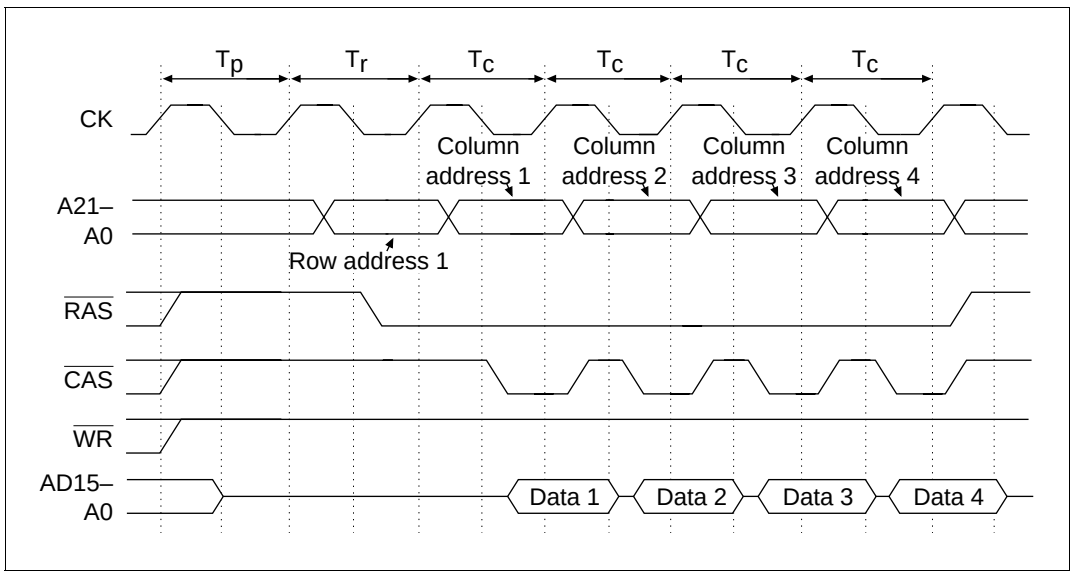


Figure 8.23 Short Pitch High-Speed Page Mode (Read Cycle)

When the write cycle continues for the same row address in the short pitch high-speed page mode, an open cycle (silent cycle) is produced for 1 cycle only. This timing is shown in figure 8.24. Likewise, when a write cycle continues after the read cycle for the same row address, a silent cycle is produced for 1 cycle. This timing is shown in figure 8.25. Note also that when DRAM is written to in short-pitch, high-speed page mode when using DMAC single address mode, a silent cycle is inserted in each transfer. The details of timing are discussed in section 20.3.3, Bus Timing.

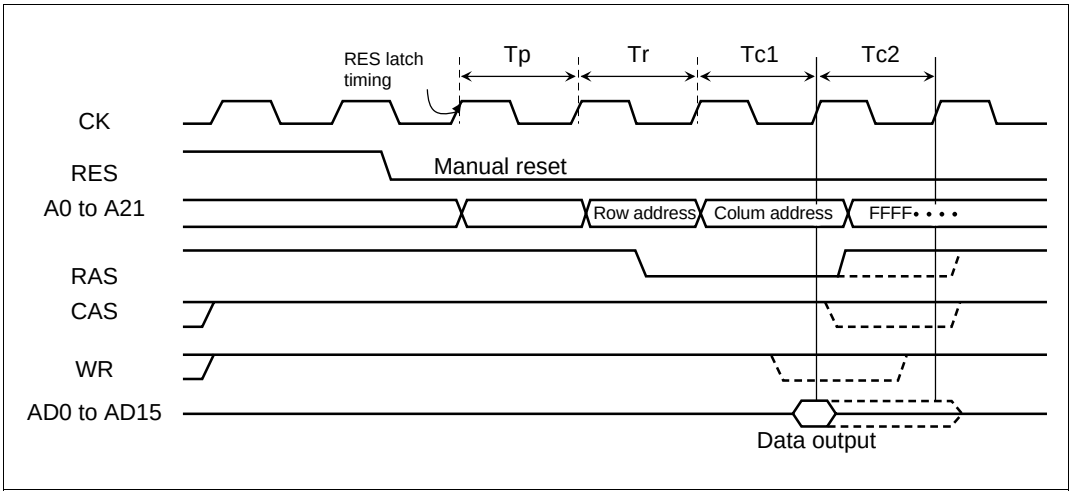


Figure 8.38 Long - pitch Mode Write (1)

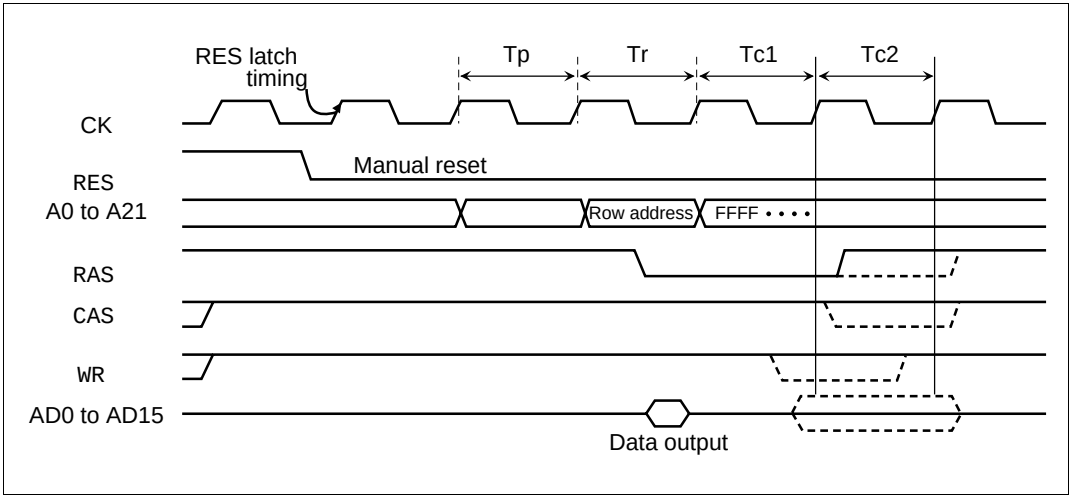


Figure 8.39 Long - pitch Mode Write (2)

The DACK output when a transfer occurs from an external device with DACK to a memory-mapped external device is the write waveform. The DACK output when a transfer occurs from a memory-mapped external device to an external device with DACK is the read waveform. The setting of the acknowledge mode (AM) bits in the channel control registers (CHCR0, CHCR1) have no effect.

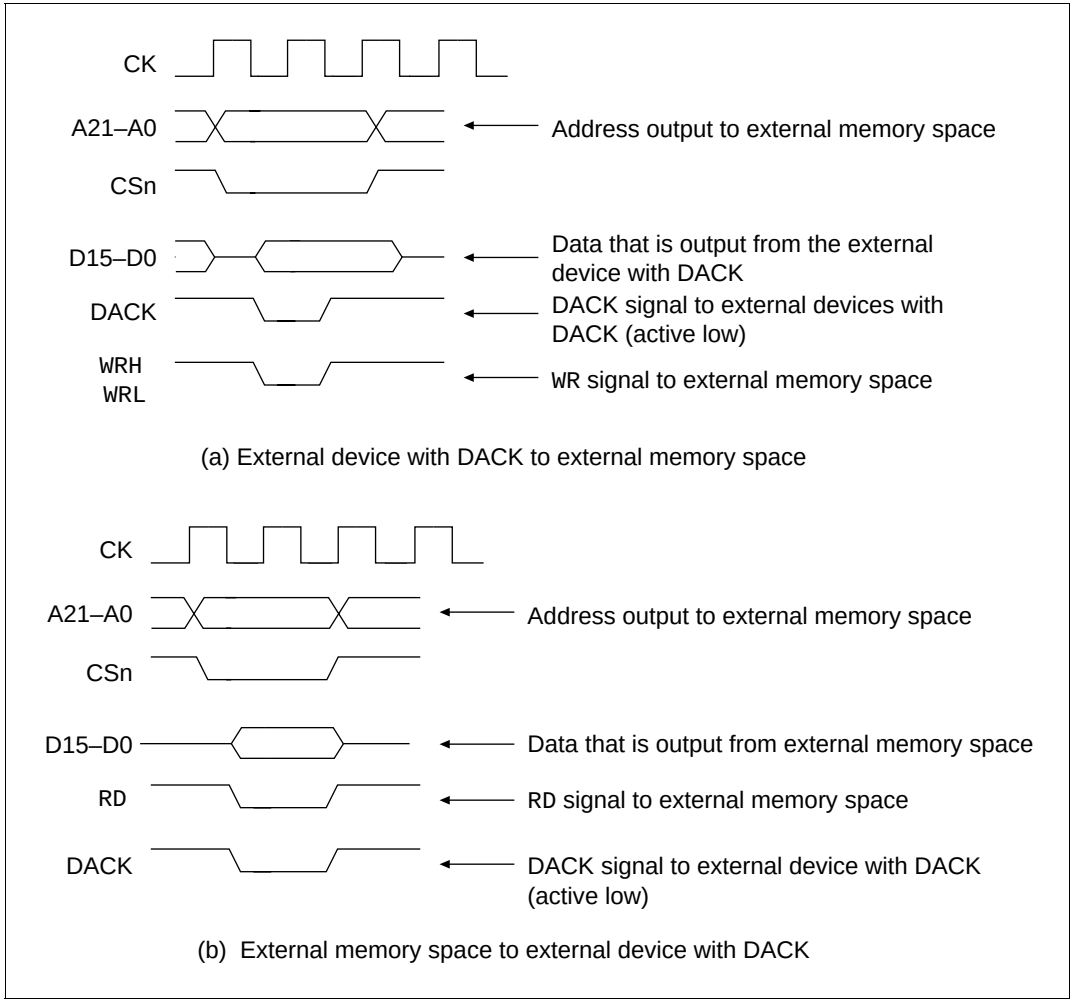


Figure 9.7 Example of DMA Transfer Timing in the Single Address Mode

Address H'5FFFFF7:

- Bits 7–0 (reserved): These bits always read as 1. The write value should always be 1.

Bit:	7	6	5	4	3	2	1	0
Bit name:	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1
R/W:	—	—	—	—	—	—	—	—

Different Triggers for TPC Output Groups 1 and 0: If TPC output groups 1 and 0 are triggered by different compare matches, the address of the upper 4 bits of NDRA (group 1) is H'5FFFFF5 and the address of the lower 4 bits of NDRA (group 0) is H'5FFFFF7. Bits 3–0 of address H'5FFFFF5 and bits 7–4 of address H'5FFFFF7 are reserved bits. The write value should always be 1. These bits always read as 1.

Address H'5FFFFF5:

- Bits 7–4 (next data 7–4 (NDR7–NDR4)): NDR7–NDR4 store the next output data for TPC output group 1.
- Bits 3–0 (reserved): These bits always read as 1. The write value should always be 1.

Bit:	7	6	5	4	3	2	1	0
Bit name:	NDR7	NDR6	NDR5	NDR4	—	—	—	—
Initial value:	0	0	0	0	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	—	—	—	—

Address H'5FFFFF7:

- Bits 7–4 (reserved): These bits always read as 1. The write value should always be 1.
- Bits 3–0 (next data 3–0 (NDR3–NDR0)): NDR3-NDR0 store the next output data for TPC output group 0.

Bit:	7	6	5	4	3	2	1	0
Bit name:	—	—	—	—	NDR3	NDR2	NDR1	NDR0
Initial value:	1	1	1	1	0	0	0	0
R/W:	—	—	—	—	R/W	R/W	R/W	R/W

11.3.2 Output Timing

If TPC output is enabled, next data register (NDRA/NDRB) contents are transferred to the data register (PBDR) and output when the selected compare-match occurs. Figure 11.3 shows the timing of these operations. The example is of ordinary output upon compare match A with groups 2 and 3.

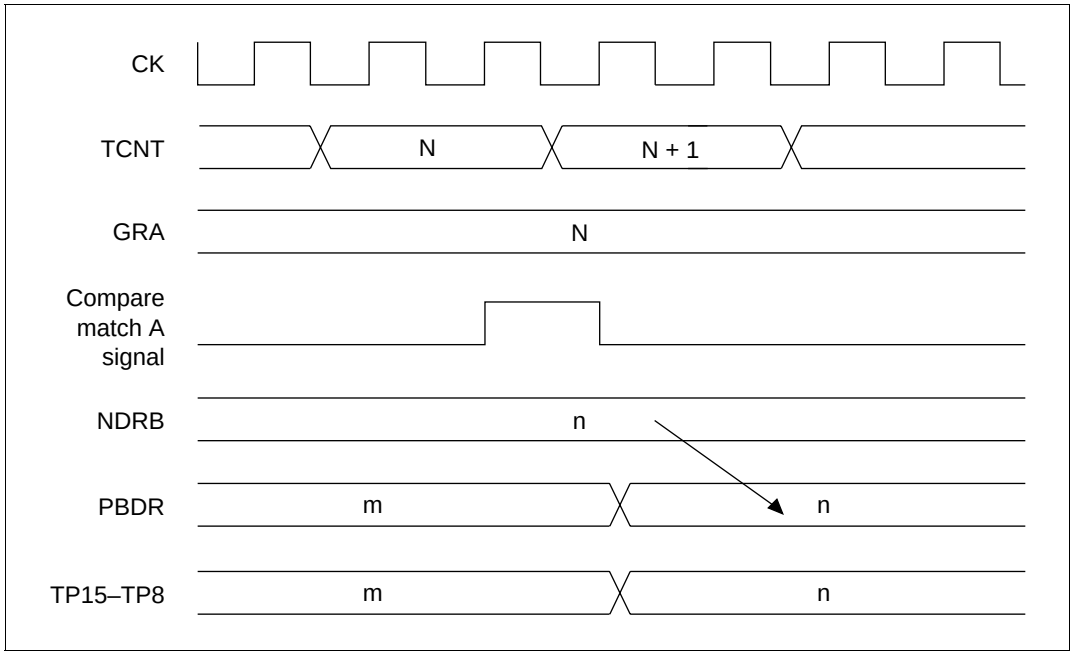
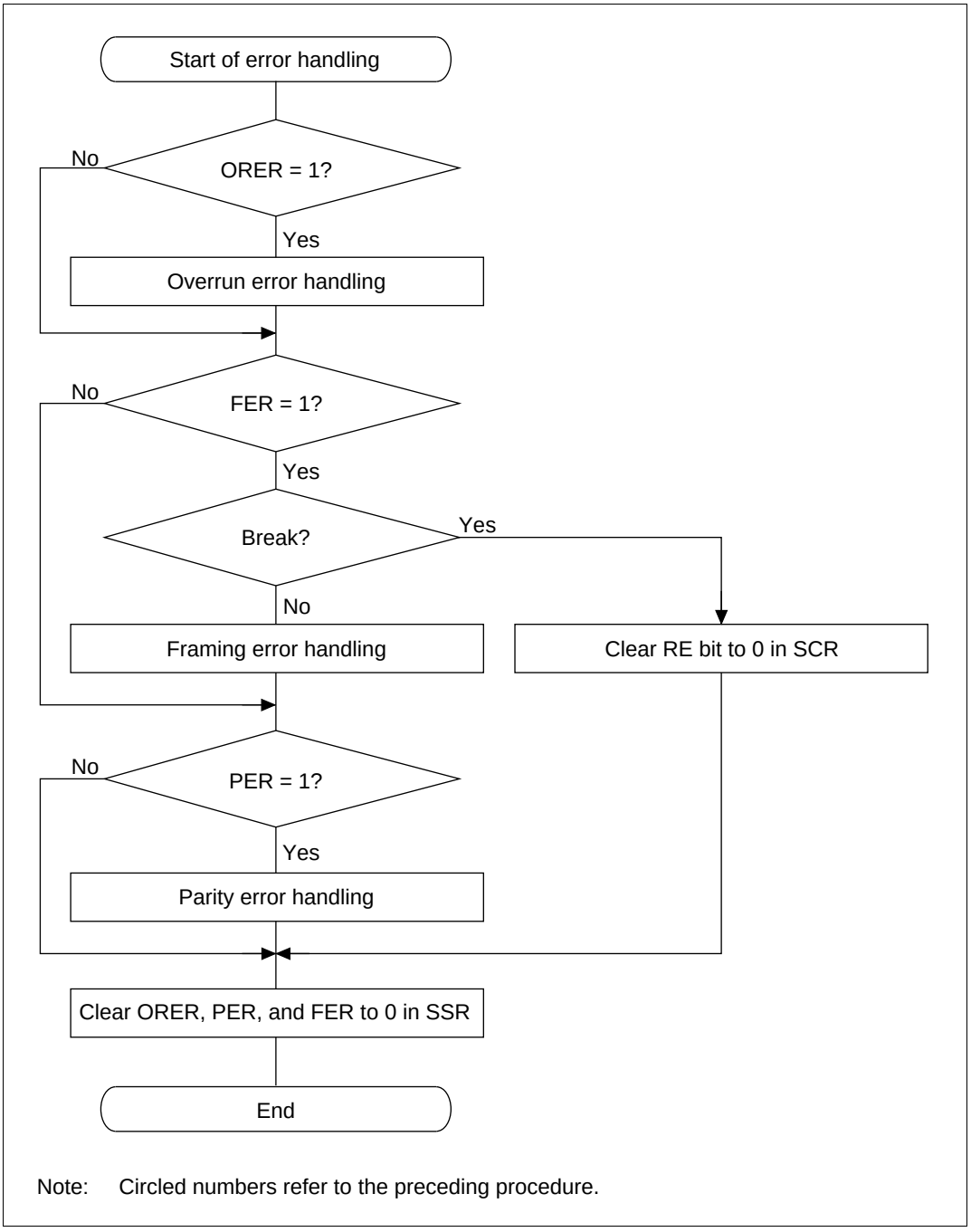


Figure 11.3 Transfer and Output Timing for NDR Data

11.3.3 Examples of Use of Ordinary TPC Output

Settings for Ordinary TPC Output (figure 11.4):

1. Select GRA as the output compare register (output disable) with the timer I/O control register (TIOR).
2. Set the TPC output trigger cycle.
3. Select the counter clock with the TPSC2–TPSC0 bits of the timer control register (TCR). Select the counter clear sources with the CCLR1 and CCLR0 bits.
4. Set the timer interrupt enable register (TIER) to enable IMIA interrupts. Transfers to the NDR can also be set using the DMAC.
5. Set the initial output value in the I/O port data register to be used by TPC.
6. Set the I/O port control register to be used by TPC as the TP pin function (11).



Note: Circled numbers refer to the preceding procedure.

Figure 13.7 Sample Flowchart for Receiving Serial Data (cont)

1. The SCI monitors the TDRE bit in the SSR. When TDRE is cleared to 0 the SCI recognizes that the transmit data register (TDR) contains new data, and loads this data from the TDR into the transmit shift register (TSR).
2. After loading the data from the TDR into the TSR, the SCI sets the TDRE bit to 1 and starts transmitting. If the transmit-data-empty interrupt enable bit (TIE) in the SCR is set to 1, the SCI requests a transmit-data-empty interrupt (TXI) at this time.

Serial transmit data is transmitted in the following order from the TxD pin (figure 13.11):

1. Start bit: one 0 bit is output.
2. Transmit data: seven or eight bits are output, LSB first.
3. Multiprocessor bit: one multiprocessor bit (MPBT value) is output.
4. Stop bit: one or two 1 bits (stop bits) are output.
5. Mark state: output of 1 bits continues until the start bit of the next transmit data.
6. The SCI checks the TDRE bit when it outputs the stop bit. If TDRE is 0, the SCI loads data from the TDR into the TSR, outputs the stop bit, then begins serial transmission of the next frame. If TDRE is 1, the SCI sets the TEND bit in the SSR to 1, outputs the stop bit, then continues output of 1 bits in the mark state. If the transmit-end interrupt enable bit (TEIE) in the SCR is set to 1, a transmit-end interrupt (TEI) is requested at this time.

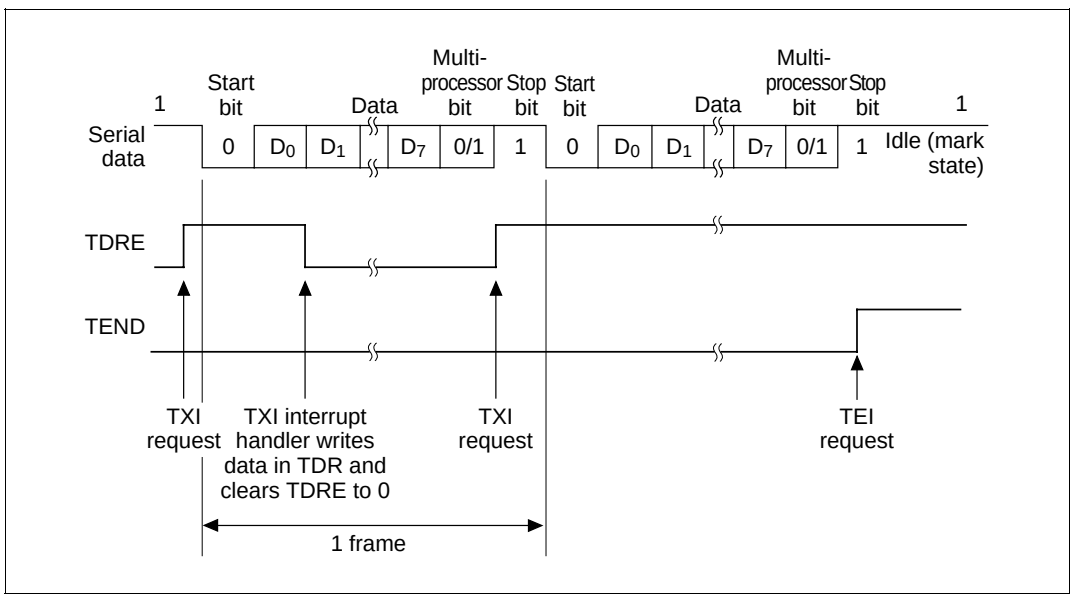


Figure 13.11 Example of SCI Multiprocessor Transmit Operation (8-bit data with multiprocessor bit and one stop bit)

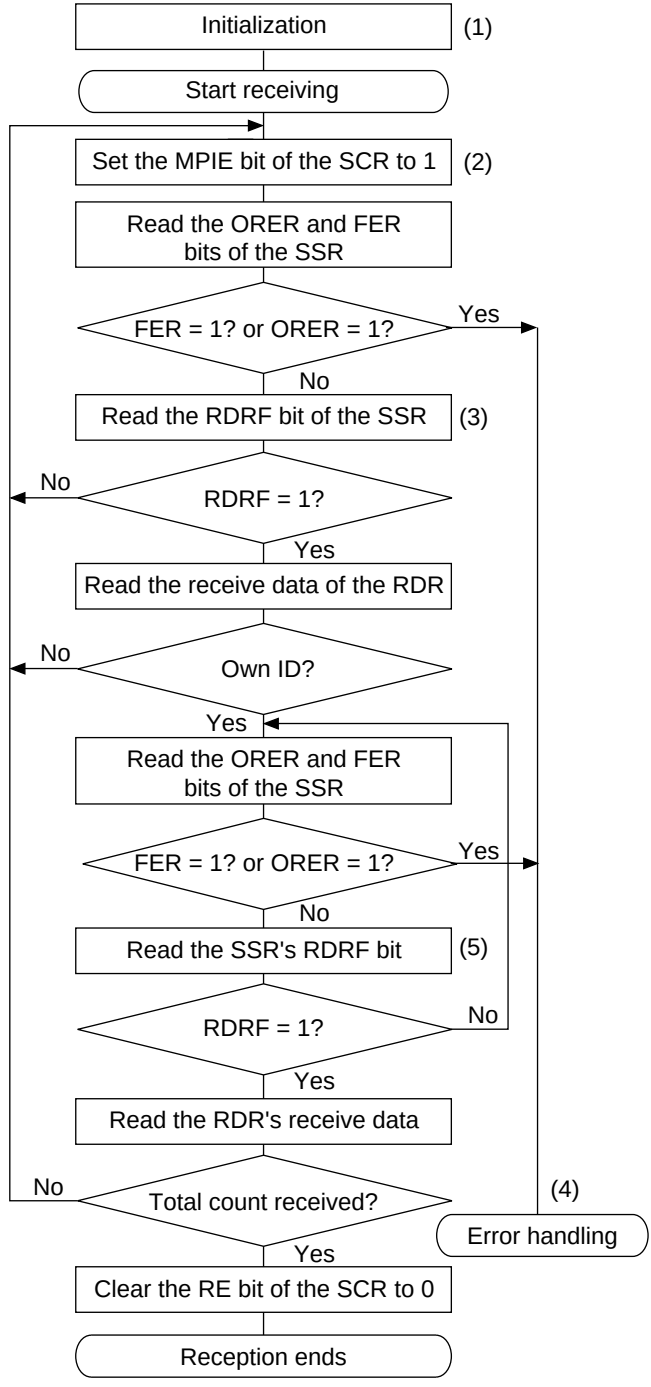
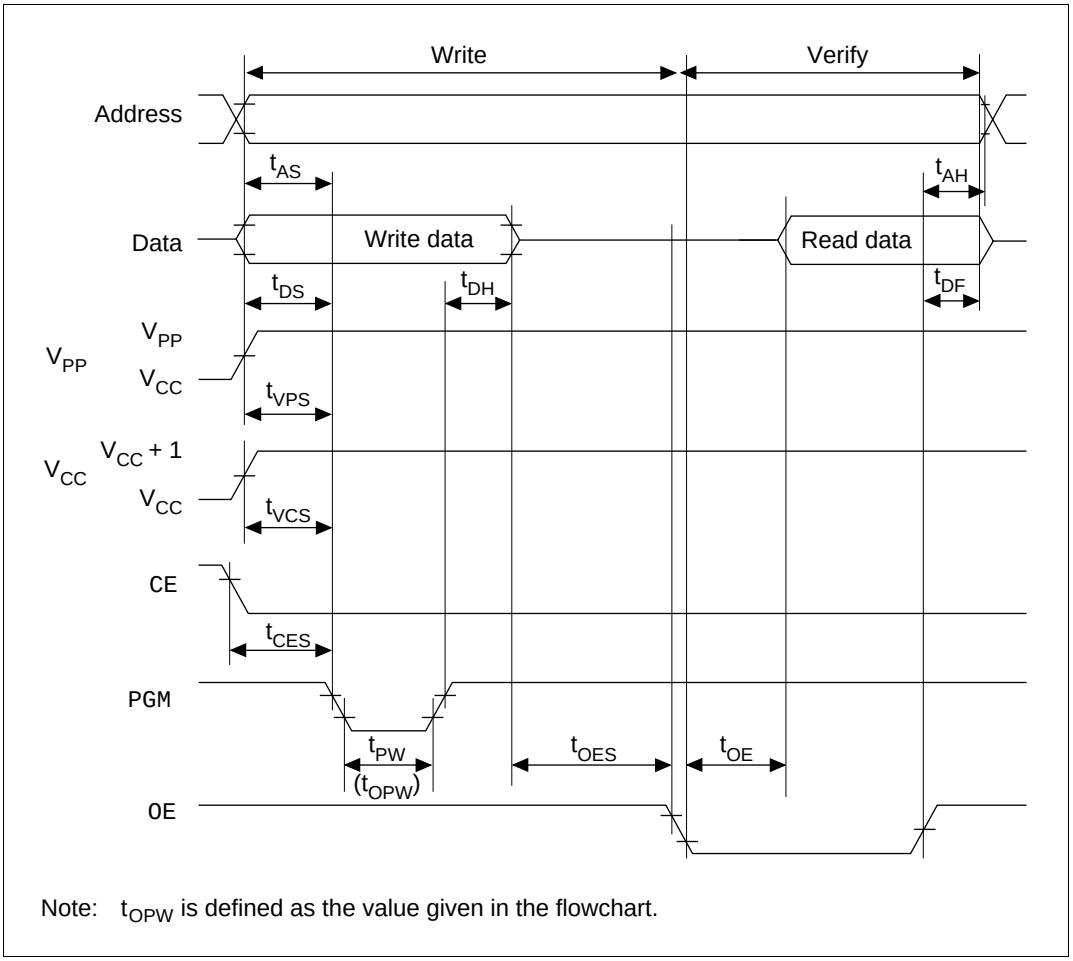


Figure 13.12 Sample Flowchart for Receiving Multiprocessor Serial Data

Section 16 ROM

16.1 Overview

The SH7020 microcomputer has 16 kbytes of on-chip ROM (mask ROM). The SH7021 microcomputer has 32 kbytes of on-chip ROM (mask ROM or PROM). The on-chip ROM is connected to the CPU and the direct memory access controller (DMAC) through a 32-bit data bus (figure 16.1). The CPU can access the on-chip ROM in 8-, 16- and 32-bit widths and the DMAC can access the ROM in 8- and 16-bit widths. Data in the on-chip ROM can always be accessed in one cycle.



Note: t_{OPW} is defined as the value given in the flowchart.

Figure 16.5 Write/Verify Timing

16.3.3 Points to Note About Writing

1. Always write using the prescribed voltage and timing. The write voltage (programming voltage) V_{PP} is 12.5 V (when the EPROM writer is set to the Hitachi specifications for HN27C101, V_{PP} becomes 12.5 V.) Applying a voltage in excess of the rated voltage may damage the device. Pay particular attention to overshooting in the EPROM writer.

2. Before programming, always check that the indexes of the EPROM writer socket, socket adapter, and devices are consistent with each other. If they are not mounted in the proper location, an overcurrent may be generated, damaging the device.

3. Do not touch the socket adapter or device during writing. Contact can cause malfunctions that prevent data from being written accurately.

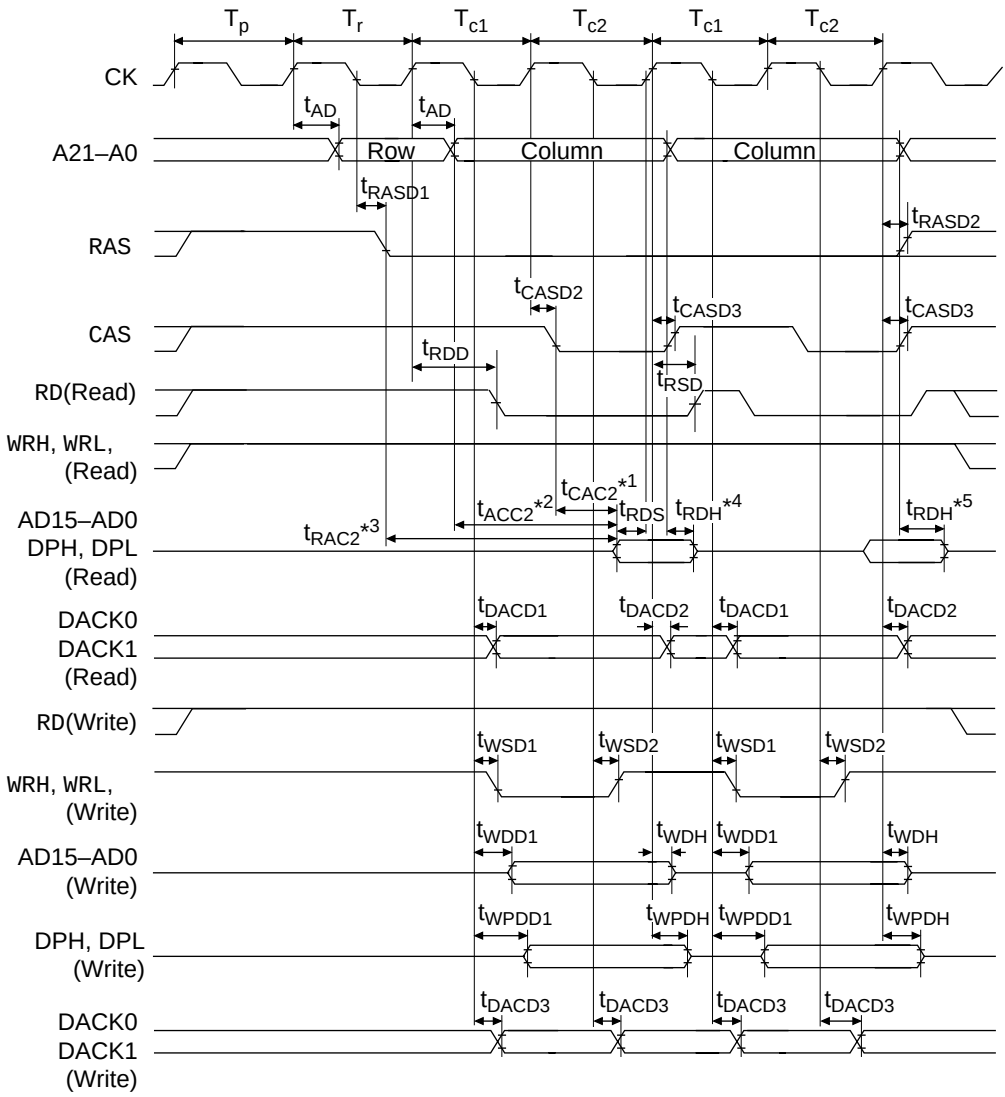
Table 19.7 Bus Timing (2) (cont)

Conditions: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 16.6 MHz, Ta = –20 to +75°C*

*: Normal products. Ta = –40 to +85°C for wide-temperature range products.

Item		Symbol	Min	Max	Unit	Figures
DACK0, DACK1 delay time 1		t_{DACD1}	—	25	ns	19.8, 19.9, 19.11–19.14, 19.19, 19.20
DACK0, DACK1 delay time 2		t_{DACD2}	—	25	ns	
DACK0, DACK1 delay time 3		t_{DACD3}	—	25	ns	19.9, 19.13, 19.14, 19.19
DACK0, DACK1 delay time 4		t_{DACD4}	—	25	ns	19.11, 19.12
DACK0, DACK1 delay time 5		t_{DACD5}	—	25	ns	
Read delay time	35% duty*2	t_{RDD}	—	$t_{cyc} \times 0.35 + 12$	ns	19.8, 19.9, 19.11-19.15, 19.19
	50% duty		—	$t_{cyc} \times 0.5 + 15$	ns	
Data setup time for CAS		t_{DS}	0*5	—	ns	19.11, 19.13
CAS setup time for RAS		t_{CSR}	10	—	ns	19.16, 19.17, 19.18
Row address hold time		t_{RAH}	10	—	ns	19.11, 19.13
Write command hold time		t_{WCH}	15	—	ns	
Write command setup time	35% duty*2	t_{WCS}	0	—	ns	19.11
	50% duty		0	—	ns	
Access time from CAS precharge*6		t_{ACP}	t_{cyc} –20	—	ns	19.12

Notes
1. HBS and LBS signals are 30 ns.
2. When frequency is 10 MHz or more
3. n is the number of wait cycles.
4. Access time from addresses A0 to A21 is tcyc-25.
5. –5 ns for parity output of DRAM long-pitch access
6. It is not necessary to meet the t_{RDS} specification as long as the access time specification is met.



Notes:
1. For t_{CAC2}, use $t_{cyc} \times (n + 1) - 25$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
2. For t_{ACC2}, use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
3. For t_{RAC2}, use $t_{cyc} \times (n + 2.5) - 20$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.
4. t_{RDH} is measured from A21–A0 or CAS, whichever is negated first.
5. t_{RDH} is measured from A21–A0, RAS, or CAS whichever is negated first.

Figure 19.14 DRAM Bus Cycle: (Long Pitch, High-Speed Page Mode)

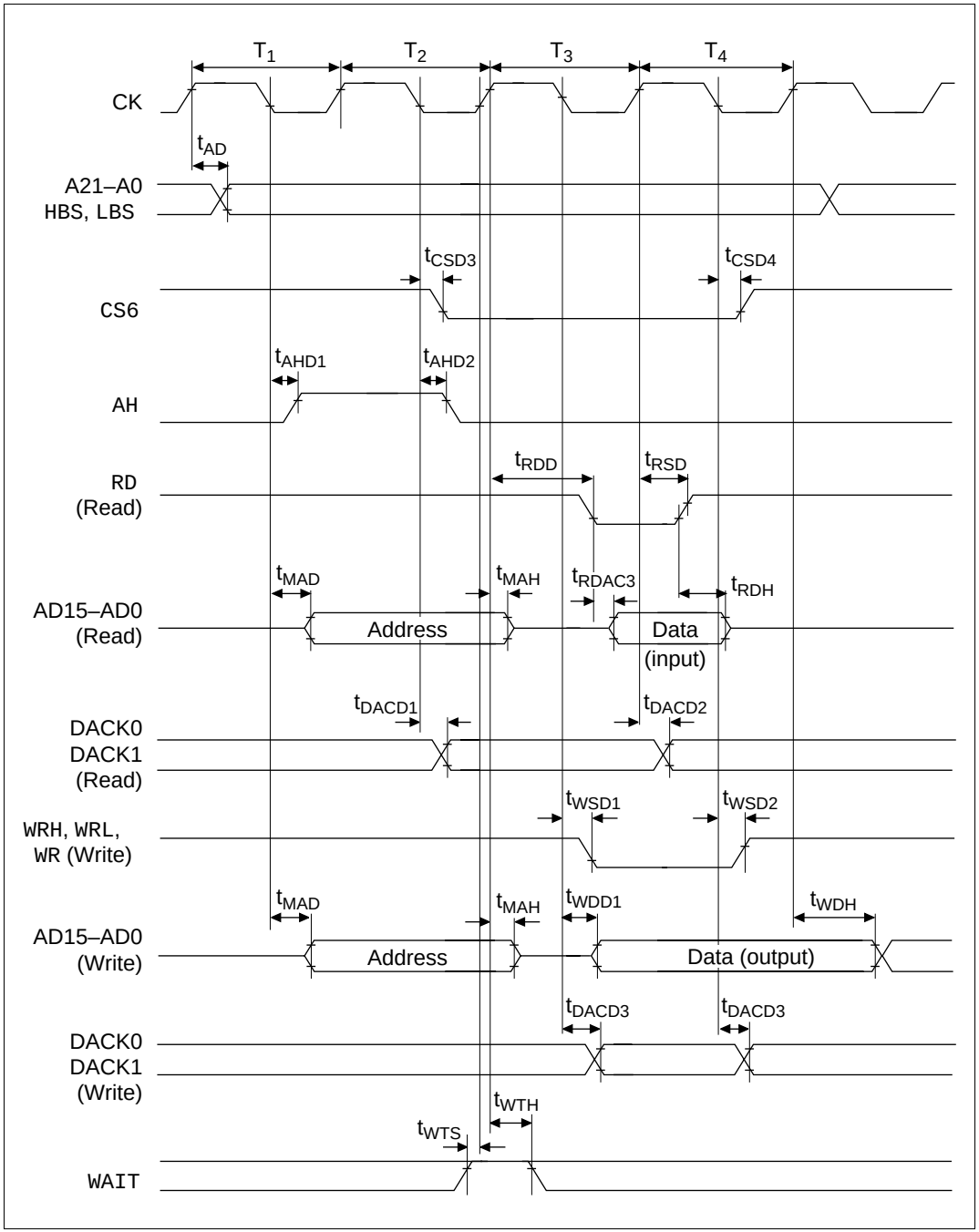


Figure 19.32 Address/Data Multiplex I/O Bus Cycle

19.4 Usage Note

The ZTAT version and the mask ROM version satisfy the electrical properties given in this document. However, effective values of the electrical properties, the operating margin, and the noise margin may differ with the manufacturing processes, on-chip ROM, and layout patterns. When conducting a system evaluation test using the ZTAT version, conduct a similar evaluation test of the mask ROM version before it replaces the ZTAT version.