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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

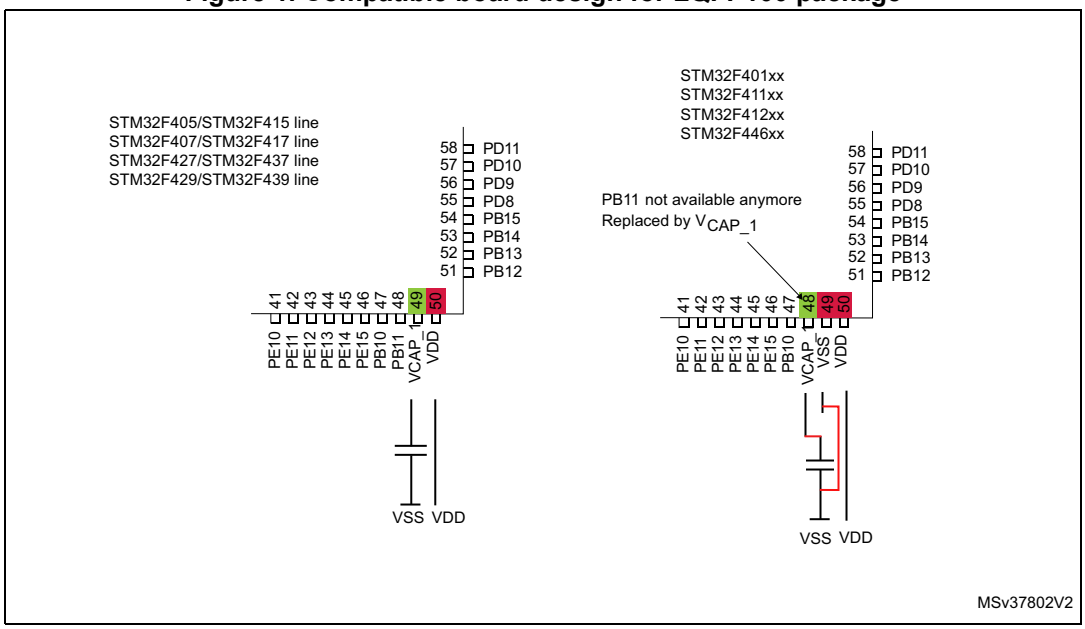
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412cgu6tr

2.1 Compatibility with STM32F4 series

The STM32F412xE/G are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F412xE/G can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

Figure 1. Compatible board design for LQFP100 package



3.16 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash memory
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using one of the interface listed in the *Table 3* or the USB OTG FS in device mode through DFU (device firmware upgrade).

Table 3. Embedded bootloader interfaces

Package	USART1 PA9/ PA10	USART2 PD6/ PD5	USART3 PB11/ PB10	I2C1 PB6/ PB7	I2C2 PF0/ PF1	I2C3 PA8/ PB4	I2C FMP1 PB14/ PB15	SPI1 PA4/ PA5/ PA6/ PA7	SPI3 PA15/ PC10/ PC11/ PC12	SPI4 PE11/ PE12/ PE13/ PE14	CAN2 PB5/ PB13	USB PA11 /P12
UFQFPN48	Y	-	-	Y	-	Y	Y	Y	-	-	Y	Y
WLCSP64	Y	-	-	Y	-	Y	Y	Y	Y	-	Y	Y
LQFP64	Y	-	-	Y	-	Y	Y	Y	Y	-	Y	Y
LQFP100	Y	Y	-	Y	-	Y	Y	Y	Y	Y	Y	Y
LQFP144	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
UFBGA100	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
UFBGA144	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

For more detailed information on the bootloader, refer to Application Note: AN2606, *STM32™ microcontroller system memory boot mode*.

3.17 Power supply schemes

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through V_{DD} pins. Requires the use of an external power supply supervisor connected to the V_{DD} and NRST pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively, with decoupling technique.

Note: The V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to Section 3.18.2: Internal reset OFF). Refer to Table 4: Regulator ON/OFF and internal power supply supervisor availability to identify the packages supporting this option.

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DDUSB} can be connected either to VDD or an external independent power supply (3.0 to 3.6 V) for USB transceivers.
  For example, when device is powered at 1.8 V, an independent power supply 3.3V can be connected to V_{DDUSB}. When the V_{DDUSB} is connected to a separated power supply,

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

The RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

3.21 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  To further reduce the power consumption, the Flash memory can be switched off before entering in Sleep mode. Note that this requires a code execution from the RAM.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm/ wakeup/ tamper/ time stamp events).

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on one of the WKUP pins, or an RTC alarm/ wakeup/ tamper/time stamp event occurs.

  Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

3.22 V_{BAT} operation

The VBAT pin allows to power the device V_{BAT} domain from an external battery, an external super-capacitor, or from V_{DD} when no external battery and an external super-capacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC and the backup registers.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation. When PDR_ON pin is not connected to V_{DD} (internal Reset OFF), the V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

3.23.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1/8) can be seen as three-phase PWM generator multiplexed on 4 independent channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as a 16-bit PWM generator, they have full modulation capability (0-100%).

The advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.23.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F412xE/G (see *Table 5* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F412xE/G devices include 4 full-featured general-purpose timers: TIM2. TIM3, TIM4 and TIM5. TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter plus a 16-bit prescaler. They all features four independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 15 input capture/output compare/PWMs

  TIM2. TIM3, TIM4 and TIM5 general-purpose timers can operate together or in conjunction with the other general-purpose timers and TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM output.

  TIM2. TIM3, TIM4 and TIM5 channels have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

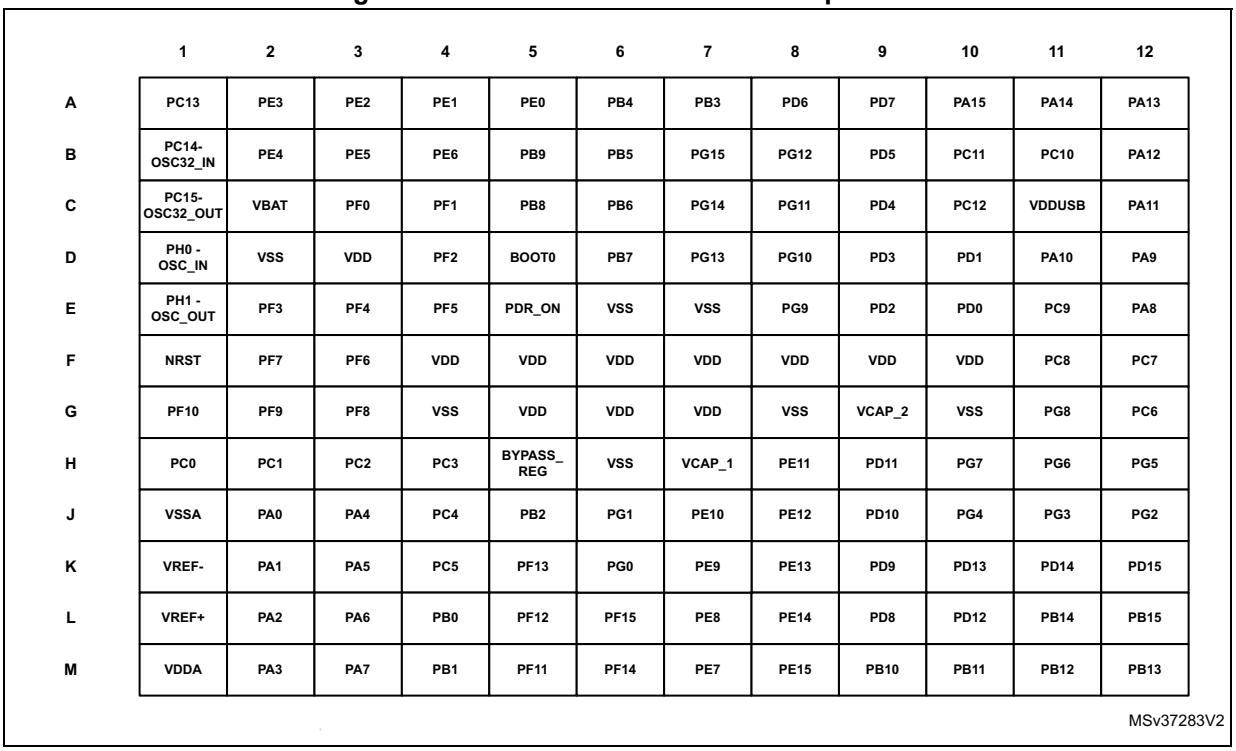
- **TIM9, TIM10, TIM11, TIM12, TIM13 and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13 and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with TIM2. TIM3, TIM4 and TIM5 full-featured general-purpose timers or used as simple time bases.

3.23.3 Basic timer (TIM6, TIM7)

TIM6 and TIM7 timers are basic 16-bit timers. They support independent DMA request generation.

Figure 17. STM32F412xE/G UFBGA144 pinout



	1	2	3	4	5	6	7	8	9	10	11	12
A	PC13	PE3	PE2	PE1	PE0	PB4	PB3	PD6	PD7	PA15	PA14	PA13
B	PC14-OSC32_IN	PE4	PE5	PE6	PB9	PB5	PG15	PG12	PD5	PC11	PC10	PA12
C	PC15-OSC32_OUT	VBAT	PF0	PF1	PB8	PB6	PG14	PG11	PD4	PC12	VDDUSB	PA11
D	PH0 - OSC_IN	VSS	VDD	PF2	BOOT0	PB7	PG13	PG10	PD3	PD1	PA10	PA9
E	PH1 - OSC_OUT	PF3	PF4	PF5	PDR_ON	VSS	VSS	PG9	PD2	PD0	PC9	PA8
F	NRST	PF7	PF6	VDD	VDD	VDD	VDD	VDD	VDD	VDD	PC8	PC7
G	PF10	PF9	PF8	VSS	VDD	VDD	VDD	VSS	VCAP_2	VSS	PG8	PC6
H	PC0	PC1	PC2	PC3	BYPASS_REG	VSS	VCAP_1	PE11	PD11	PG7	PG6	PG5
J	VSSA	PA0	PA4	PC4	PB2	PG1	PE10	PE12	PD10	PG4	PG3	PG2
K	VREF-	PA1	PA5	PC5	PF13	PG0	PE9	PE13	PD9	PD13	PD14	PD15
L	VREF+	PA2	PA6	PB0	PF12	PF15	PE8	PE14	PD8	PD12	PB14	PB15
M	VDDA	PA3	PA7	PB1	PF11	PF14	PE7	PE15	PB10	PB11	PB12	PB13

MSv37283V2

1. The above figure shows the package top view.

Table 8. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/ output pin
I/O structure	FT	5 V tolerant I/O
	TC	Standard 3.3 V I/O
	B	Dedicated BOOT0 pin
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	-	M6	54	PF14	I/O	FT	-	I2CFMP1_SCL, FSMC_A8, EVENTOUT	-
-	-	-	-	-	L6	55	PF15	I/O	FT	-	I2CFMP1_SDA, FSMC_A9, EVENTOUT	-
-	-	-	-	-	K6	56	PG0	I/O	FT	-	CAN1_RX, FSMC_A10, EVENTOUT	-
-	-	-	-	-	J6	57	PG1	I/O	FT	-	CAN1_TX, FSMC_A11, EVENTOUT	-
-	-	-	38	M7	M7	58	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, QUADSPI_BK2_IO0, FSMC_D4/FSMC_DA4, EVENTOUT	-
-	-	-	39	L7	L7	59	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, QUADSPI_BK2_IO1, FSMC_D5/FSMC_DA5, EVENTOUT	-
-	-	-	40	M8	K7	60	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, QUADSPI_BK2_IO2, FSMC_D6/FSMC_DA6, EVENTOUT	-
-	-	-	-	-	-	61	VSS	S	-	-	-	-
-	-	-	-	-	G6	62	VDD	S	-	-	-	-
-	-	-	41	L8	J7	63	PE10	I/O	FT	-	TIM1_CH2N, QUADSPI_BK2_IO3, FSMC_D7/FSMC_DA7, EVENTOUT	-
-	-	-	42	M9	H8	64	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, FSMC_D8/FSMC_DA8, EVENTOUT	-
-	-	-	43	L9	J8	65	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, FSMC_D9/FSMC_DA9, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	51	C3	78	B11	B11	111	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, QUADSPI_BK1_IO1, SDIO_D2, EVENTOUT	-
-	52	B3	79	C10	B10	112	PC11	I/O	FT	-	I2S3ext_SD, SPI3_MISO, USART3_RX, QUADSPI_BK2_NCS, FSMC_D2, SDIO_D3, EVENTOUT	-
-	53	A3	80	B10	C10	113	PC12	I/O	FT	-	SPI3_MOSI/I2S3_SD, USART3_CK, FSMC_D3, SDIO_CK, EVENTOUT	-
-	-	-	81	C9	E10	114	PD0	I/O	FT	-	CAN1_RX, FSMC_D2/FSMC_DA2, EVENTOUT	-
-	-	-	82	B9	D10	115	PD1	I/O	FT	-	CAN1_TX, FSMC_D3/FSMC_DA3, EVENTOUT	-
-	54	A4	83	C8	E9	116	PD2	I/O	FT	-	TIM3_ETR, FSMC_NWE, SDIO_CMD, EVENTOUT	-
-	-	-	84	B8	D9	117	PD3	I/O	FT	-	TRACED1, SPI2_SCK/I2S2_CK, DFSDM1_DATIN0, USART2_CTS, QUADSPI_CLK, FSMC_CLK, EVENTOUT	-
-	-	-	85	B7	C9	118	PD4	I/O	FT	-	DFSDM1_CKIN0, USART2_RTS, FSMC_NOE, EVENTOUT	-
-	-	-	86	A6	B9	119	PD5	I/O	FT	-	USART2_TX, FSMC_NWE, EVENTOUT	-
-	-	-	-	-	E7	120	VSS	S	-	-	-	-
-	-	-	-	-	F7	121	VDD	S	-	-	-	-
-	-	-	87	B6	A8	122	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, DFSDM1_DATIN1, USART2_RX, FSMC_NWAIT, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
42	58	B5	92	B5	C6	136	PB6	I/O	FT	-	TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, SDIO_D0, EVENTOUT	-
43	59	A6	93	B4	D6	137	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FSMC_NL, EVENTOUT	-
44	60	D4	94	A4	D5	138	BOOT0	I	B	-	-	VPP
45	61	C5	95	A3	C5	139	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, SPI5_MOSI/I2S5_SD, CAN1_RX, I2C3_SDA, SDIO_D4, EVENTOUT	-
46	62	B6	96	B3	B5	140	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, I2C2_SDA, SDIO_D5, EVENTOUT	-
-	-	-	97	C3	A5	141	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, EVENTOUT	-
-	-	-	98	A2	A4	142	PE1	I/O	FT	-	FSMC_NBL1, EVENTOUT	-
47	63	A7	99	-	E6	-	VSS	S	-	-	-	-
-	-	C6	-	H3	E5	143	PDR_ON	I	FT	-	-	-
48	64	A8	100	-	F5	144	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F412xE/Greference manual.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

6.3 Operating conditions

6.3.1 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale3: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x01	0	-	64	MHz
		Power Scale2: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x10	0	-	84	
		Power Scale1: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x11	0	-	100	
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	50	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	-	100	MHz
V_{DD}	Standard operating voltage	-	1.7(1)	-	3.6	V
V_{DDA}(2)(3)	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}(4)	1.7(1)	-	2.4	V
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11 and PA12 pins)	USB not used	1.7	3.3	3.6	V
		USB used(5)	3.0	-	3.6	
V_{BAT}	Backup operating voltage	-	1.65	-	3.6	V
V_{12}	Regulator ON: 1.2 V internal voltage on VCAP_1/VCAP_2 pins	VOS[1:0] bits in PWR_CR register = 0x01 Max frequency 64 MHz	1.08(6)	1.14	1.20(6)	V
		VOS[1:0] bits in PWR_CR register = 0x10 Max frequency 84 MHz	1.20(6)	1.26	1.32(6)	
		VOS[1:0] bits in PWR_CR register = 0x11 Max frequency 100 MHz	1.26	1.32	1.38	
V_{12}	Regulator OFF: 1.2 V external voltage must be supplied on VCAP_1/VCAP_2 pins	Max frequency 64 MHz	1.10	1.14	1.20	V
		Max frequency 84 MHz	1.20	1.26	1.32	
		Max frequency 100 MHz	1.26	1.32	1.38	
V_{IN}	Input voltage on RST, FT and TC pins(7)	$2\ V \le V_{DD} \le 3.6\ V$	–0.3	-	5.5	V
		$V_{DD} \le 2\ V$	–0.3	-	5.2	
	Input voltage on BOOT0 pin	-	0	-	9	

Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)	100	36.3	38.95	41.19	42.95	mA
			84	31.1	33.22	34.81	36.10	
			64	22.3	23.97	25.10	26.23	
			50	18.3	19.77	20.65	21.73	
			25	10.1	11.39	12.16	13.11	
			20	8.6	9.60	10.25	11.06	
		HSI, PLL OFF, all peripherals enabled(3)	16	6.3	6.85	7.51	8.38	
			1	1.1	1.39	1.82	2.61	
		External clock, PLL ON(2) all peripherals disabled(3)	100	22.1	23.95	25.80	27.50	
			84	19.7	20.79	22.52	24.12	
			64	14.5	15.88	17.21	18.54	
			50	12.2	13.38	14.59	15.79	
			25	7.0	8.05	8.89	10.16	
			20	6.0	6.84	7.51	8.52	
		HSI, PLL OFF, all peripherals disabled(3)	16	4.4	4.91	5.56	6.54	
			1	0.9	1.25	1.79	2.59	

1. Based on characterization, not tested in production unless otherwise specified.
2. Refer to *Table 44* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 64* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 64. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master full duplex/receiver mode, 2.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	MHz
		Master transmitter mode 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Master mode 1.7 V < V_{DD} < 3.6 V SPI1/2/3/4/5	-	-	25	
		Slave transmitter/full duplex mode 2.7 V < V_{DD} < 3.6 V SPI1//4/5	-	-	50	
		Slave transmitter/full duplex mode 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	35(2)	
		Slave receiver mode, 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Slave mode, 1.7 V < V_{DD} < 3.6 V SPI2/3	-	-	25	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, SPI presc = 2	T_{PCLK}-1.5	T_{PCLK}	T_{PCLK} +1.5	ns
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$3T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2T_{PCLK}$	-	-	ns
$t_{su(MI)}$	Data input setup time	Master mode	4.5	-	-	ns
$t_{su(SI)}$		Slave mode	1.5	-	-	ns
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	ns
$t_{h(SI)}$		Slave mode	0.5	-	-	ns

QSPI interface characteristics

Unless otherwise specified, the parameters given in the following tables for QSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C=20pF
- Measurement points are done at CMOS levels: 0.5VDD

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 66. QSPI dynamic characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	QSPI clock frequency	Write mode 1.71 V≤V_{DD}≤3.6 V C_{load} = 15 pF	-	-	80	MHz
		Read mode 2.7 V<V_{DD}<3.6 V C_{load} = 15 pF	-	-	100	
		1.71 V≤V_{DD}≤3.6 V	-	-	50	
$t_{w(CKH)}$	QSPI clock high and low	-	($T_{(CK)}$ / 2)-1	-	$T_{(CK)}$ / 2	ns
$t_{w(CKL)}$			$T_{(CK)}$ / 2)	-	($T_{(CK)}$ / 2)+1	
$t_{s(IN)}$	Data input setup time	-	0.5	-	-	
$t_{h(IN)}$	Data input hold time	-	3.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	1	1.5	
$t_{h(OUT)}$	Data output hold time	-	0.5	-	-	

1. Guaranteed by characterization results, not tested in production.

Table 67. QSPI dynamic characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	QSPI clock frequency	Write mode 1.71 V≤V_{DD}≤3.6 V C_{load} = 15 pF	-	-	80	MHz
		Read mode 2.7 V<V_{DD}<3.6 V C_{load} = 15 pF	-	-	80	
		1.71 V≤V_{DD}≤3.6 V	-	-	50	

2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Figure 45. USB OTG FS timings: definition of data signal rise and fall time

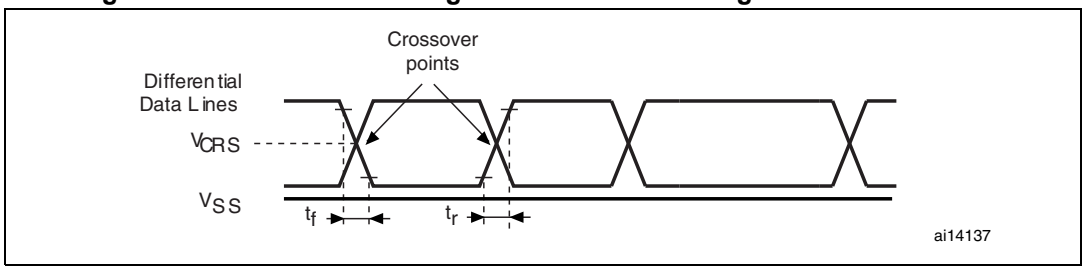


Table 70. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

CAN (controller area network) interface

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

Table 92. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period, V_{DD} range= 2.7 to 3.6 V	$2T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x= 0...2)	-	1	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	T_{HCLK} + 0.5	-	
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	4	
$t_{d(CLKL-NBLL)}$	FSMC_CLK low to FSMC_NBL low	-	3	
$t_{d(CLKH-NBLH)}$	FSMC_CLK high to FSMC_NBL high	T_{HCLK}	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 57. Synchronous non-multiplexed PSRAM write timings

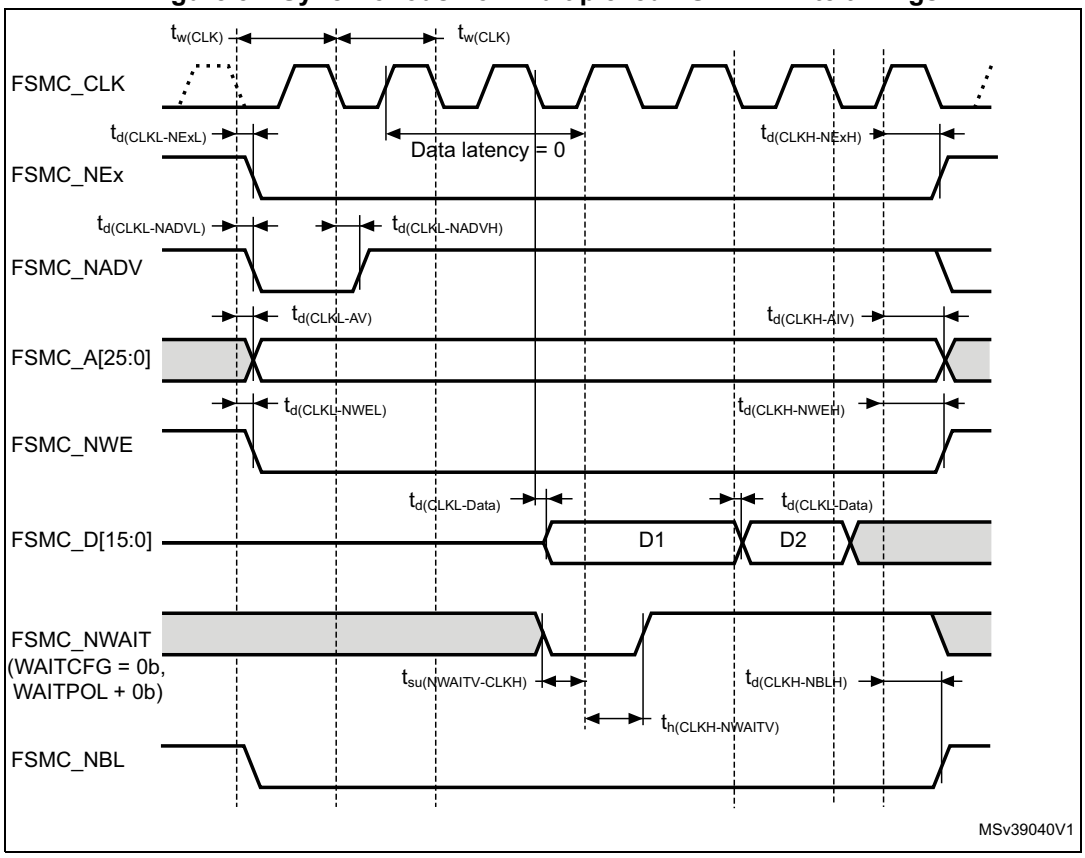


Table 98. WLCSP64 - 64-pin, 3.658 x 3.686 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.170	-	-	0.0067	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.588	3.623	3.658	0.1413	0.1426	0.1440
E	3.616	3.651	3.686	0.1424	0.1437	0.1451
e	-	0.400	-	-	0.0157	-
e1	-	2.800	-	-	0.1102	-
e2	-	2.800	-	-	0.1102	-
F	-	0.4115	-	-	0.0162	-
G	-	0.4255	-	-	0.0168	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 61. WLCSP64 - 64-pin, 3.658 x 3.686 mm, 0.4 mm pitch wafer level chip scale recommended footprint

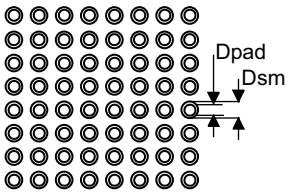


Table 99. WLCSP64 recommended PCB design rules (0.4 mm pitch)

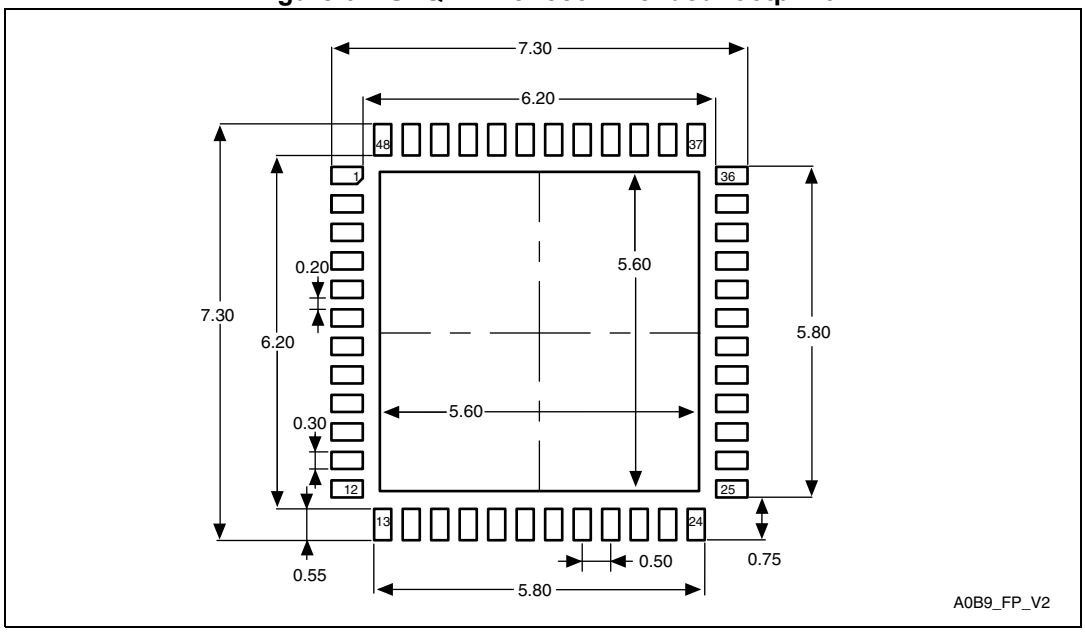
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm

Table 100. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

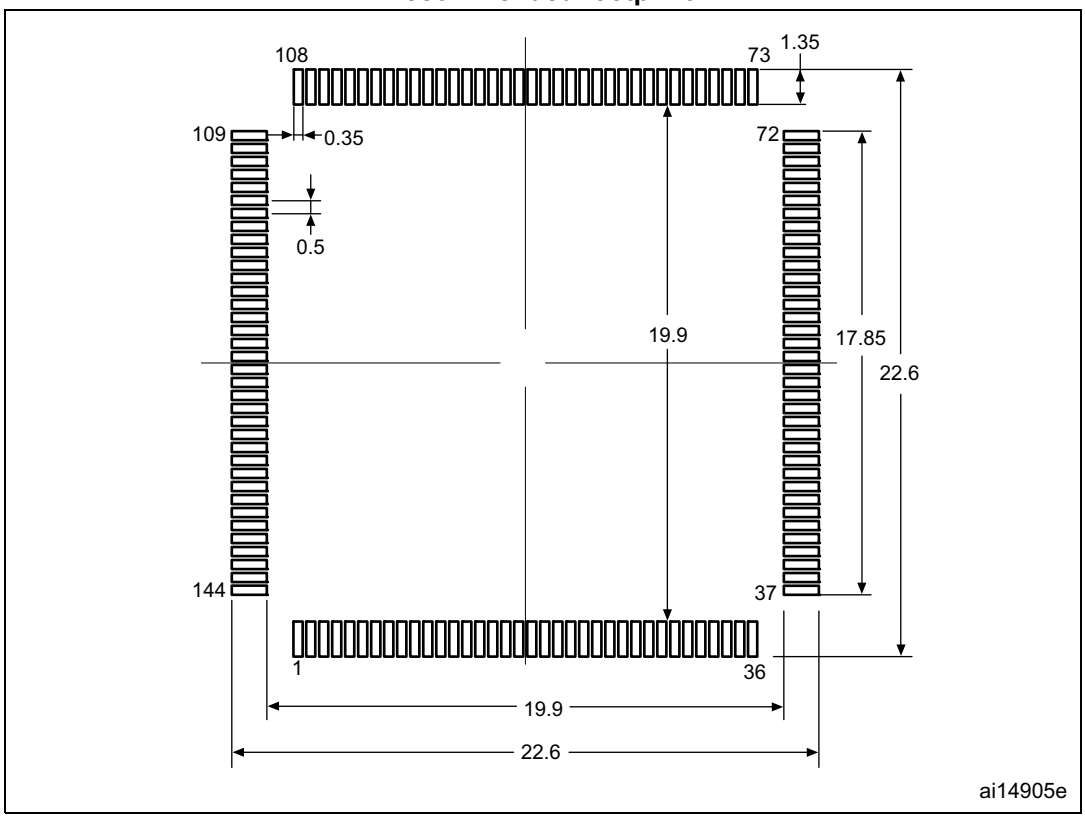
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 64. UFQFPN48 recommended footprint



1. Dimensions are in millimeters.

Figure 73. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint

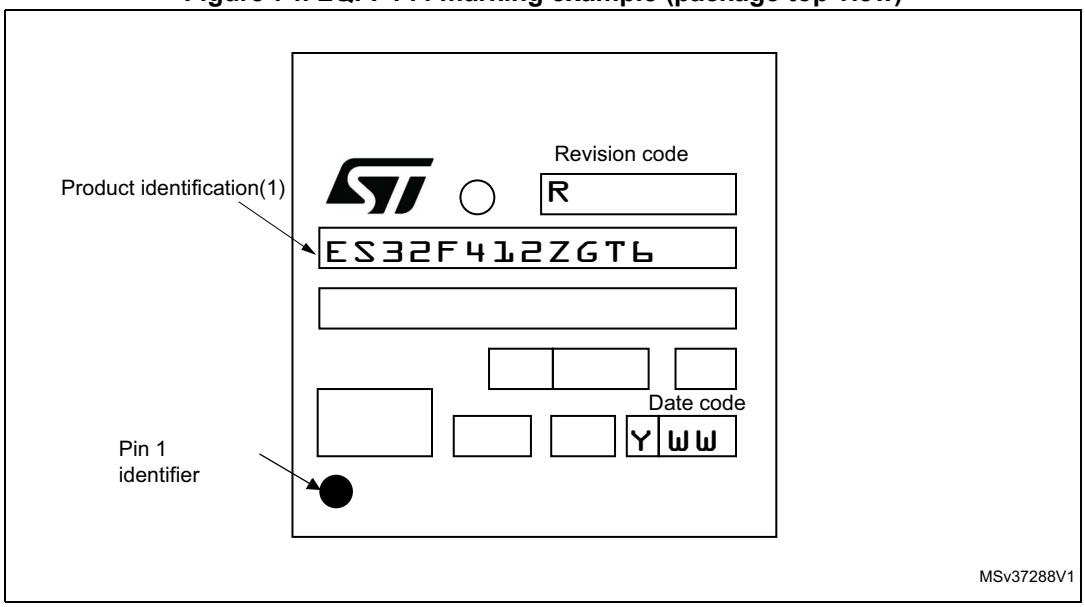


1. Dimensions are expressed in millimeters.

Device marking for LQFP144

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 74. LQFP144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Appendix A Recommendations when using the internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on-reset (POR)/power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled. By default BOR is OFF.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.