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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412ret6

3.13 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 81 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.14 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 21 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

3.15 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 100 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses and high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.19.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal power supply supervisor availability

Package	Regulator ON	Regulator OFF	Power supply supervisor ON	Power supply supervisor OFF
UFQFPN48	Yes	No	Yes	No
WLCSP64	Yes	No	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP64	Yes	No	Yes	No
LQFP100	Yes	No	Yes	No
LQFP144	Yes	No	Yes PDR_ON set to VDD	Yes PDR_ON set to V_{SS}
UFBGA100	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD		
UFBGA144	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD		

3.20 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 byte of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.21: Low-power modes*).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

The RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

3.21 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  To further reduce the power consumption, the Flash memory can be switched off before entering in Sleep mode. Note that this requires a code execution from the RAM.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm/ wakeup/ tamper/ time stamp events).

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on one of the WKUP pins, or an RTC alarm/ wakeup/ tamper/time stamp event occurs.

  Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

3.22 V_{BAT} operation

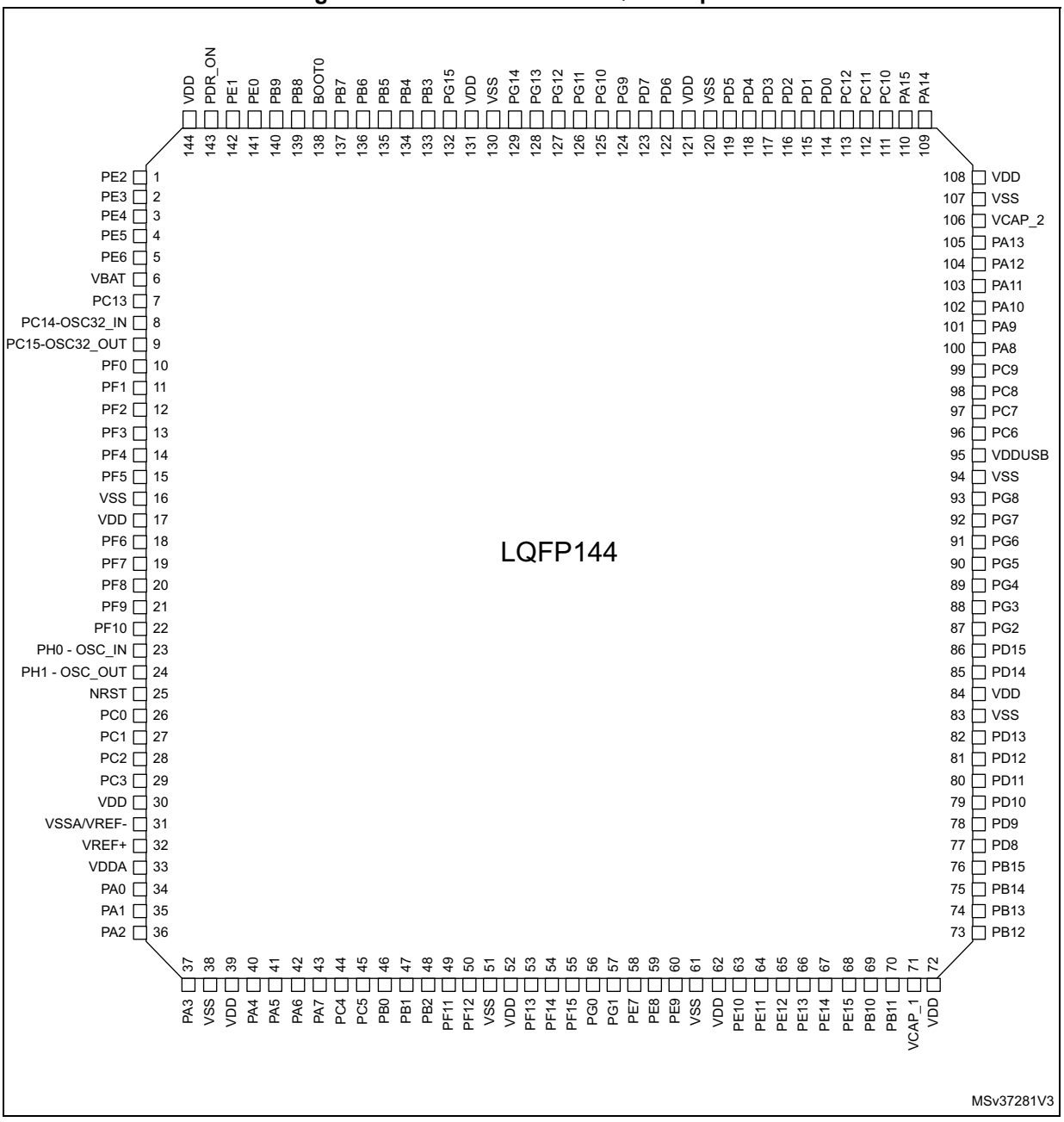
The VBAT pin allows to power the device V_{BAT} domain from an external battery, an external super-capacitor, or from V_{DD} when no external battery and an external super-capacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC and the backup registers.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation. When PDR_ON pin is not connected to V_{DD} (internal Reset OFF), the V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

Figure 15. STM32F412xE/G LQFP144 pinout



1. The above figure shows the package top view.

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
16	22	H6	31	L4	L3	42	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, I2S2_MCK, TIM13_CH1, QUADSPI_BK2_IO0, SDIO_CMD, EVENTOUT	ADC1_6
17	23	E5	32	M4	M3	43	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, QUADSPI_BK2_IO1, EVENTOUT	ADC1_7
-	24	E4	33	K5	J4	44	PC4	I/O	FT	-	I2S1_MCK, QUADSPI_BK2_IO2, FSMC_NE4, EVENTOUT	ADC1_14
-	25	G5	34	L5	K4	45	PC5	I/O	FT	-	I2CFMP1_SMBA, USART3_RX, QUADSPI_BK2_IO3, FSMC_NOE, EVENTOUT	ADC1_15
18	26	H5	35	M5	L4	46	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI5_SCK/I2S5_CK, EVENTOUT	ADC1_8
19	27	F4	36	M6	M4	47	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, SPI5_NSS/I2S5_WS, DFSDM1_DATIN0, QUADSPI_CLK, EVENTOUT	ADC1_9
20	28	G4	37	L6	J5	48	PB2	I/O	FT	-	DFSDM1_CKIN0, QUADSPI_CLK, EVENTOUT	BOOT1
-	-	-	-	-	M5	49	PF11	I/O	FT	-	TIM8_ETR, EVENTOUT	-
-	-	-	-	-	L5	50	PF12	I/O	FT	-	TIM8_BKIN, FSMC_A6, EVENTOUT	-
-	-	-	-	-	-	51	VSS	S	-	-	-	-
-	-	-	-	-	G5	52	VDD	S	-	-	-	-
-	-	-	-	-	K5	53	PF13	I/O	FT	-	I2CFMP1_SMBA, FSMC_A7, EVENTOUT	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3 σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2 σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 19*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 20*.

Figure 19. Pin loading conditions

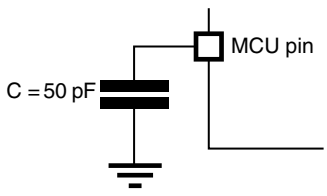
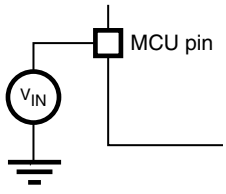


Figure 20. Input voltage measurement



6.3 Operating conditions

6.3.1 General operating conditions

Table 15. General operating conditions

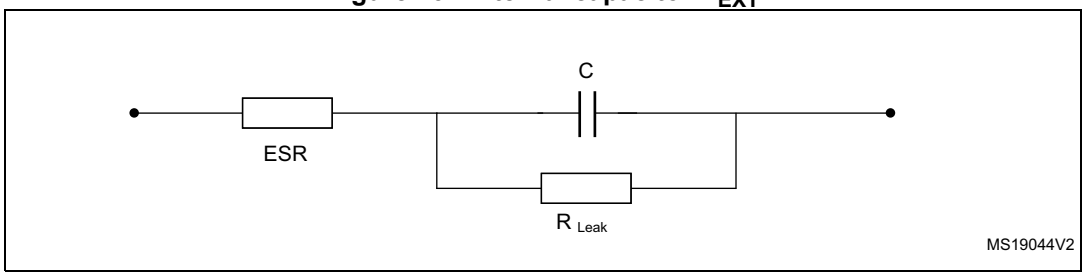
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale3: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x01	0	-	64	MHz
		Power Scale2: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x10	0	-	84	
		Power Scale1: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x11	0	-	100	
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	50	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	-	100	MHz
V_{DD}	Standard operating voltage	-	1.7(1)	-	3.6	V
V_{DDA}(2)(3)	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}(4)	1.7(1)	-	2.4	V
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11 and PA12 pins)	USB not used	1.7	3.3	3.6	V
		USB used(5)	3.0	-	3.6	
V_{BAT}	Backup operating voltage	-	1.65	-	3.6	V
V_{12}	Regulator ON: 1.2 V internal voltage on VCAP_1/VCAP_2 pins	VOS[1:0] bits in PWR_CR register = 0x01 Max frequency 64 MHz	1.08(6)	1.14	1.20(6)	V
		VOS[1:0] bits in PWR_CR register = 0x10 Max frequency 84 MHz	1.20(6)	1.26	1.32(6)	
		VOS[1:0] bits in PWR_CR register = 0x11 Max frequency 100 MHz	1.26	1.32	1.38	
V_{12}	Regulator OFF: 1.2 V external voltage must be supplied on VCAP_1/VCAP_2 pins	Max frequency 64 MHz	1.10	1.14	1.20	V
		Max frequency 84 MHz	1.20	1.26	1.32	
		Max frequency 100 MHz	1.26	1.32	1.38	
V_{IN}	Input voltage on RST, FT and TC pins(7)	$2\ V \le V_{DD} \le 3.6\ V$	–0.3	-	5.5	V
		$V_{DD} \le 2\ V$	–0.3	-	5.2	
	Input voltage on BOOT0 pin	-	0	-	9	

6.3.2 VCAP_1/VCAP_2 external capacitors

Stabilization for the main regulator is achieved by connecting the external capacitor C_{EXT} to the VCAP_1 and VCAP_2 pins. For packages supporting only 1 VCAP pin, the 2 CEXT capacitors are replaced by a single capacitor.

C_{EXT} is specified in *Table 17*.

Figure 23. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 17. VCAP_1/VCAP_2 operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor with the pins VCAP_1 and VCAP_2 available	2.2 µF
ESR	ESR of external capacitor with the pins VCAP_1 and VCAP_2 available	< 2 Ω
CEXT	Capacitance of external capacitor with a single VCAP pin available	4.7 µF
ESR	ESR of external capacitor with a single VCAP pin available	< 1 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

6.3.3 Operating conditions at power-up/power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 18. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both f_{HCLK} frequency and VDD ranges (refer to *Table 16: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 64$ MHz
  - Scale 2 for 64 MHz < $f_{HCLK} \leq 84$ MHz
  - Scale 1 for 84 MHz < $f_{HCLK} \leq 100$ MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 21. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A= 25 °C	T_A= 25 °C	T_A=85 °C	T_A=105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	28.1	30.24	31.27	32.21	mA
			84	22.7	24.05	24.54	25.11	
			64	15.7	16.99	17.47	18.03	
			50	12.3	13.36	13.82	14.36	
			25	6.5	7.44	7.82	8.30	
			20	5.6	6.16	6.66	7.20	
		HSI, PLL off, all peripherals enabled(2)(3)	16	3.9	4.70	5.31	6.08	
			1	0.6	0.78	1.33	1.98	
		External clock, PLL ON, all peripherals disabled(3)	100	14.0	15.48	16.08	16.83	
			84	11.3	12.23	12.75	13.41	
			64	7.9	8.84	9.31	10.01	
			50	6.2	7.06	7.53	8.19	
			25	3.4	4.18	4.61	5.13	
			20	2.9	3.44	3.98	4.65	
		HSI, PLL off, all peripherals disabled(3)	16	2.0	2.51	3.13	3.89	
			1	0.5	0.64	1.21	1.90	

1. Based on characterization, not tested in production unless otherwise specified
2. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.

Table 27. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	38.9	41.10	42.85	44.28	mA
			84	32.8	34.61	35.77	36.72	
			64	23.6	24.96	25.84	26.64	
			50	18.7	19.90	20.67	21.45	
			25	10.1	11.11	11.70	12.40	
			20	8.6	9.46	10.07	10.81	
		HSI, PLL OFF, all peripherals enabled	16	6.3	6.77	7.42	8.21	
			1	1.1	1.35	1.84	2.59	
		External clock, PLL ON(2) all peripherals disabled	100	24.7	26.11	27.59	28.84	
			84	21.4	22.22	23.53	24.66	
			64	15.8	16.80	17.90	18.99	
			50	12.6	13.51	14.52	15.54	
			25	7.0	7.85	8.57	9.39	
			20	6.0	6.67	7.37	8.26	
		HSI, PLL OFF, all peripherals disabled	16	4.5	4.80	5.47	6.33	
			1	0.9	1.25	1.81	2.58	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 52. EMI characteristics for LQFP144

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/100 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP144 package, conforming to IEC 61967-2, EEMBC, ART ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	20	dBµV
			30 to 130 MHz	28	
			130 MHz to 1 GHz	21	
			EMI Level	3.5	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 53. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1, UFBGA144, UFBGA100, LQFP100, LQFP64, UFQFPN48	4	500	
		T_A = +25 °C conforming to ANSI/ESD STM5.3.1, WLCSP64	3	400	
		T_A = +25 °C conforming to ANSI/ESD STM5.3.1, LQFP144	3	250	

1. Guaranteed by characterization, not tested in production.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 54. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 55*.

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 65* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 65. I²S dynamic characteristics(1)

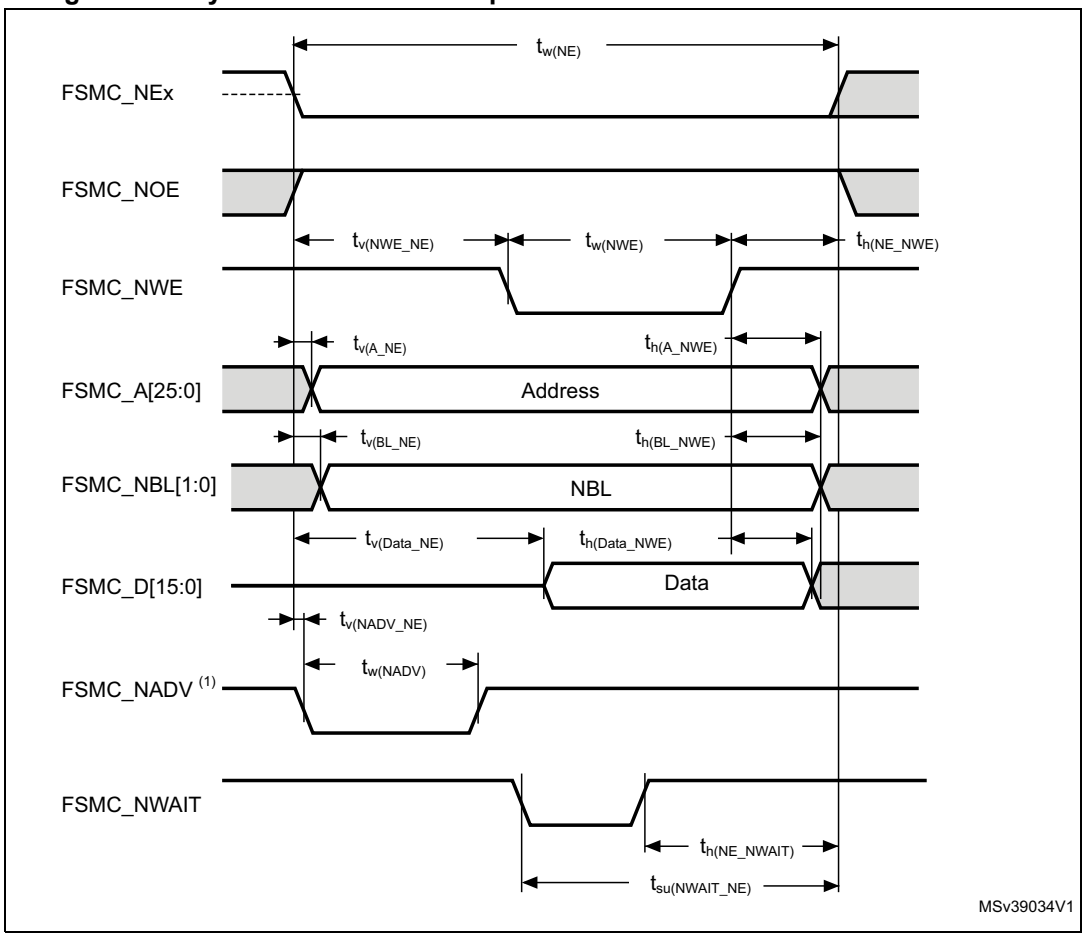
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	2	-	
$t_{h(WS)}$	WS hold time	Slave mode	0.5	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	0	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	15	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	2.5	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	6	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization, not tested in production.
2. The maximum value of 256xFs is 50 MHz (APB1 maximum frequency).

Note: Refer to the I2S section of RM0383 reference manual for more details on the sampling frequency (F_S).

*f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Figure 51. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 85. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	3 T_{HCLK} - 1	3 T_{HCLK} +0.5	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	T_{HCLK} + 0.5	T_{HCLK} + 0.5	
$t_{w(NWE)}$	FSMC_NWE low time	T_{HCLK} – 1.5	T_{HCLK}+ 1	
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK} - 1	-	
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0.5	
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK} - 0.5	-	
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1	
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	T_{HCLK} - 1	-	
$t_{v(Data\_NE)}$	Data to FSMC_NEx low to Data valid	-	T_{HCLK} + 2	
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK} + 0.5	-	
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	1	
$t_{w(NADV)}$	FSMC_NADV low time	-	T_{HCLK}+ 0.5	

Figure 53. Asynchronous multiplexed PSRAM/NOR write waveforms

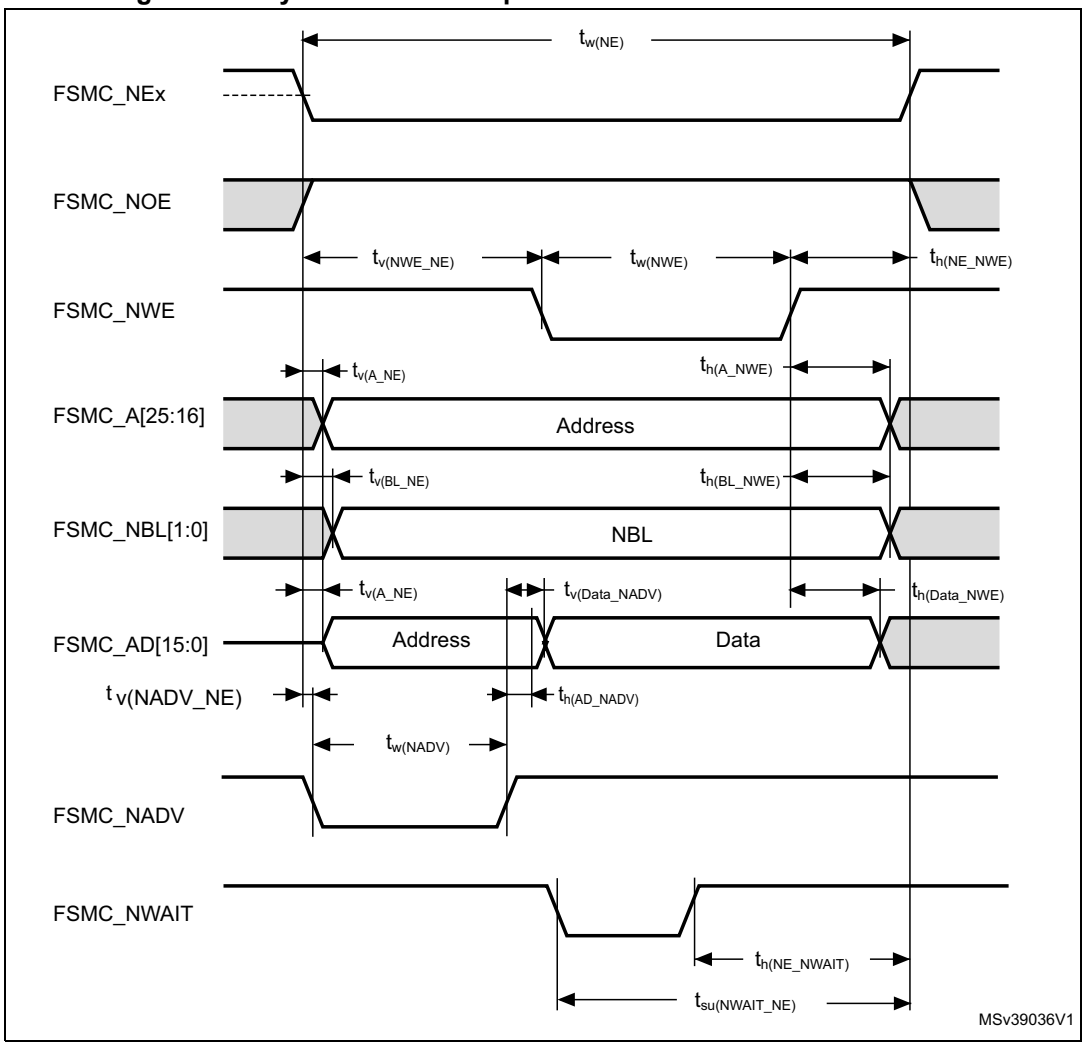


Figure 58. SDIO high-speed mode

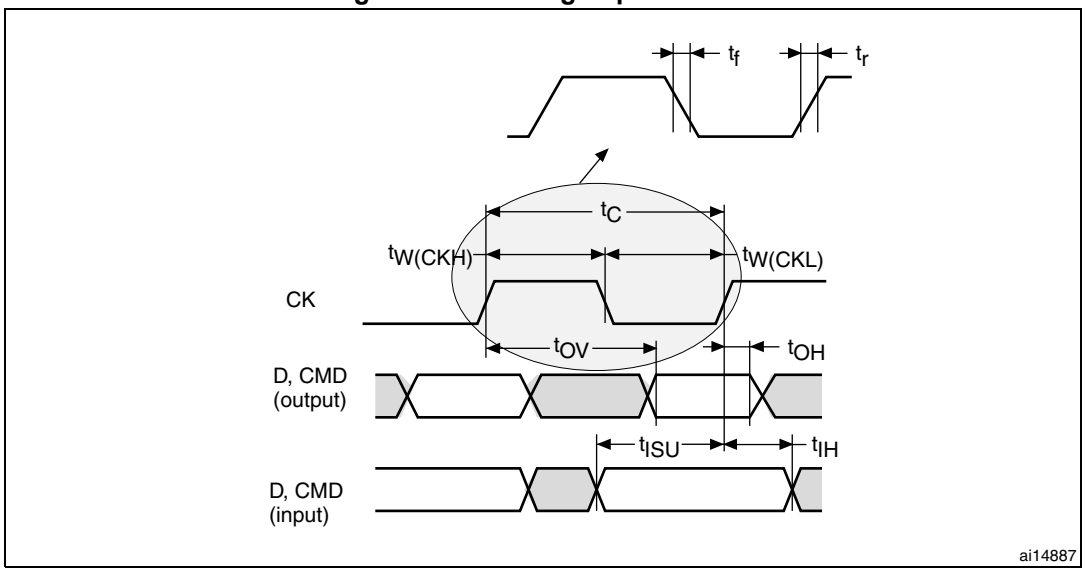


Figure 59. SD default mode

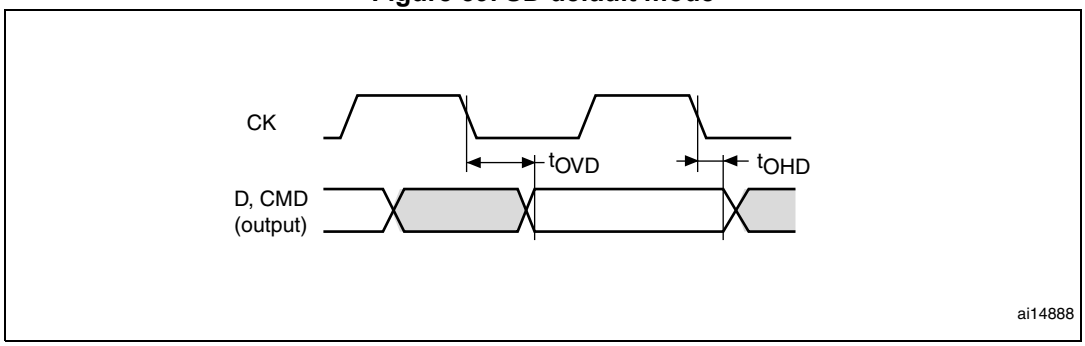


Table 95. Dynamic characteristics: SD / MMC characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50MHz	4	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	13	13.5	ns
t_{OH}	Output hold time HS	fpp =50MHz	11	-	-	

Table 95. Dynamic characteristics: SD / MMC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	fpp =25MHz	2.5	-	-	ns
t_{IHD}	Input hold time SD	fpp =25MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	fpp =25 MHz	-	1.5	2	ns
t_{OHD}	Output hold default time SD	fpp =25 MHz	0.5	-	-	

1. Guaranteed by characterization results, not tested in production.
2. V_{DD} = 2.7 to 3.6 V.

Table 96. Dynamic characteristics: eMMC characteristics V_{DD} = 1.7 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	fpp =50MHz	3.5	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	4	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	13.5	15	ns
t_{OH}	Output hold time HS	fpp =50MHz	12	-	-	

1. Guaranteed by characterization results, not tested in production.
2. C_{LOAD} = 20 pF.

6.3.27 RTC characteristics

Table 97. RTC characteristics

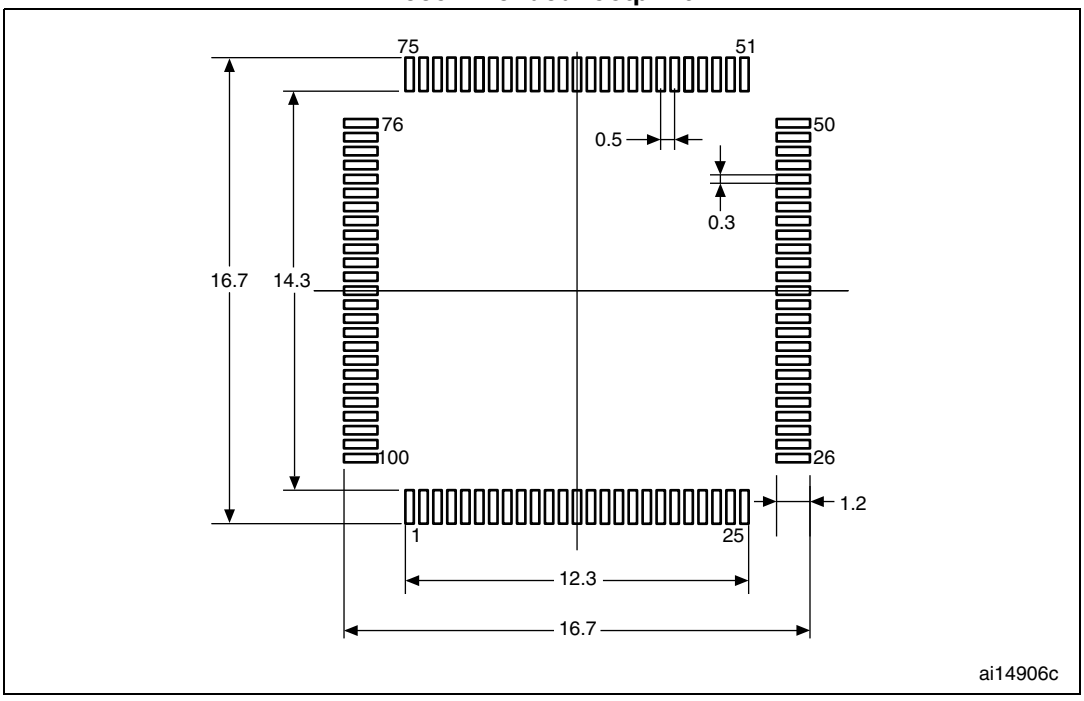
Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

Table 102. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 70. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

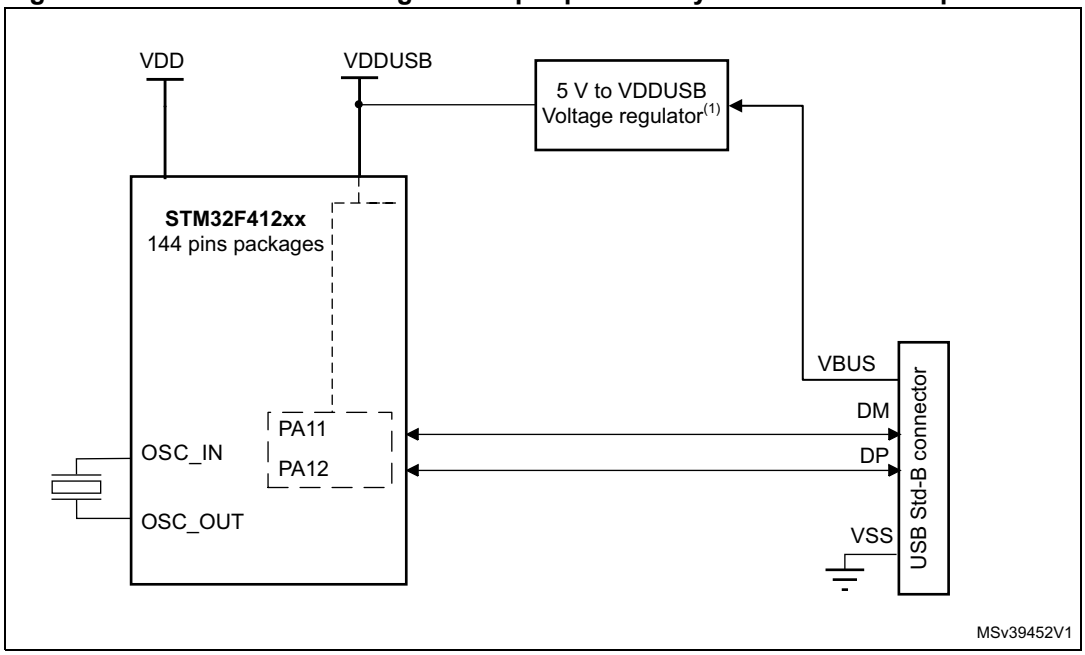


1. Dimensions are in millimeters.

Appendix B Application block diagrams

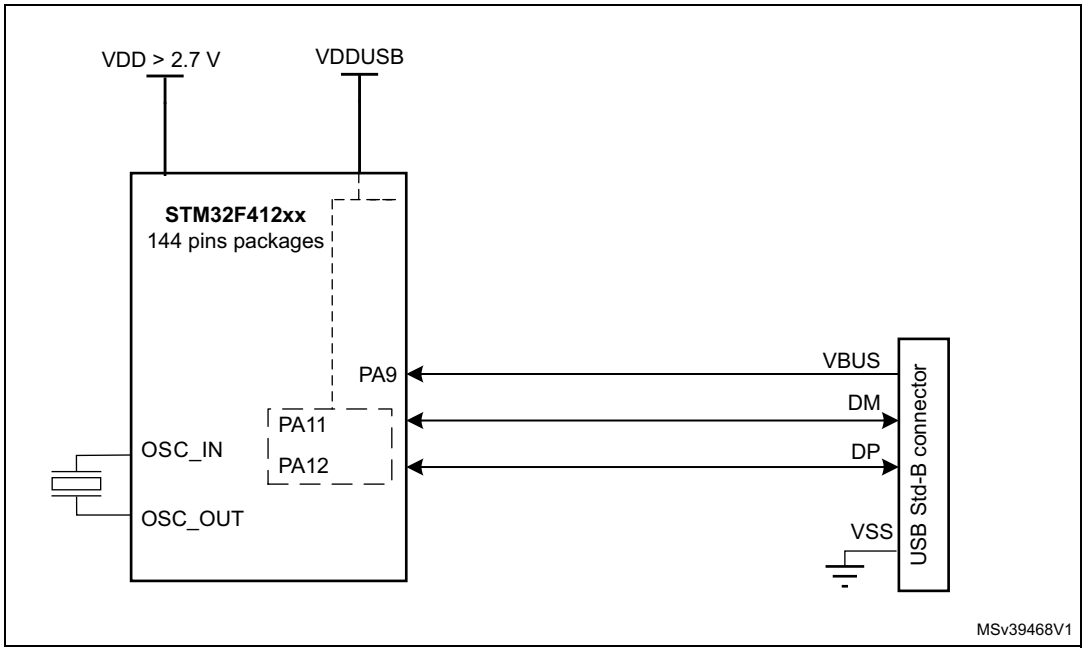
B.1 USB OTG full speed (FS) interface solutions

Figure 81. USB controller configured as peripheral-only and used in Full speed mode



1. External voltage regulator only needed when building a V_{BUS} powered device.

Figure 82. USB peripheral-only Full speed mode with direct connection for VBUS sense



1. External voltage regulator only needed when building a V_{BUS} powered device.