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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412ret6tr

1 Introduction

This datasheet provides the description of the STM32F412xE/G microcontrollers.

For information on the Cortex®-M4 core, refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

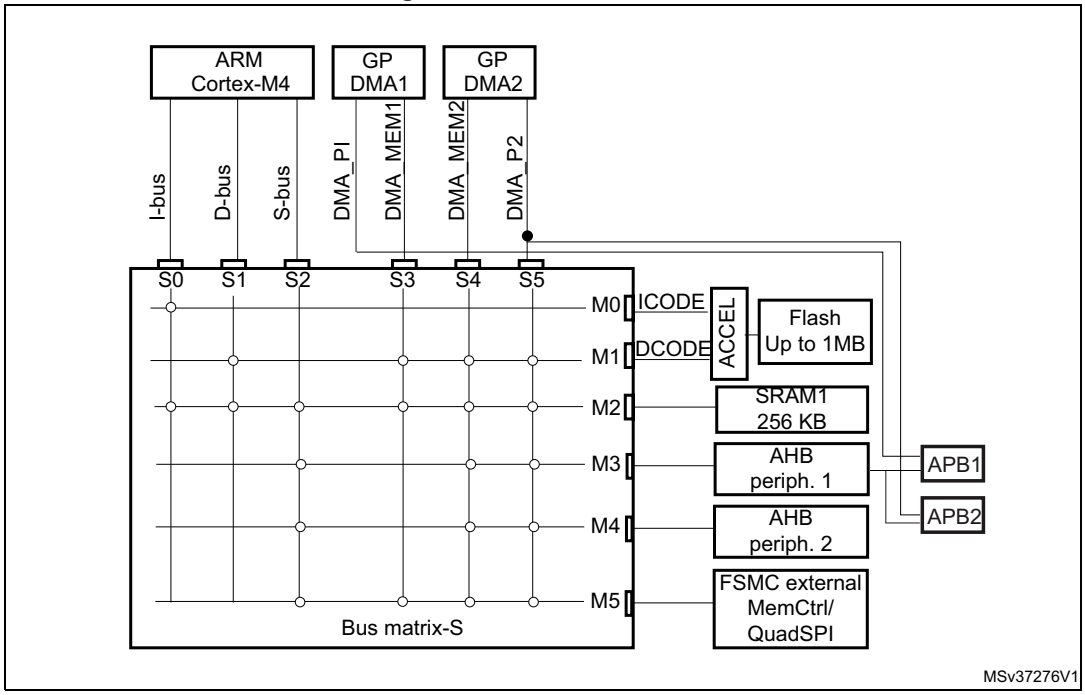
3.8 Embedded SRAM

All devices embed 256 Kbyte of system SRAM which can be accessed (read/write) at CPU clock speed with 0 wait states

3.9 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. Multi-AHB matrix



3.10 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

3.19.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal power supply supervisor availability

Package	Regulator ON	Regulator OFF	Power supply supervisor ON	Power supply supervisor OFF
UFQFPN48	Yes	No	Yes	No
WLCSP64	Yes	No	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP64	Yes	No	Yes	No
LQFP100	Yes	No	Yes	No
LQFP144	Yes	No	Yes PDR_ON set to VDD	Yes PDR_ON set to V_{SS}
UFBGA100	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD		
UFBGA144	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD		

3.20 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 byte of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.21: Low-power modes*).

3.33 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.34 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

3.35 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	-	M6	54	PF14	I/O	FT	-	I2CFMP1_SCL, FSMC_A8, EVENTOUT	-
-	-	-	-	-	L6	55	PF15	I/O	FT	-	I2CFMP1_SDA, FSMC_A9, EVENTOUT	-
-	-	-	-	-	K6	56	PG0	I/O	FT	-	CAN1_RX, FSMC_A10, EVENTOUT	-
-	-	-	-	-	J6	57	PG1	I/O	FT	-	CAN1_TX, FSMC_A11, EVENTOUT	-
-	-	-	38	M7	M7	58	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, QUADSPI_BK2_IO0, FSMC_D4/FSMC_DA4, EVENTOUT	-
-	-	-	39	L7	L7	59	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, QUADSPI_BK2_IO1, FSMC_D5/FSMC_DA5, EVENTOUT	-
-	-	-	40	M8	K7	60	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, QUADSPI_BK2_IO2, FSMC_D6/FSMC_DA6, EVENTOUT	-
-	-	-	-	-	-	61	VSS	S	-	-	-	-
-	-	-	-	-	G6	62	VDD	S	-	-	-	-
-	-	-	41	L8	J7	63	PE10	I/O	FT	-	TIM1_CH2N, QUADSPI_BK2_IO3, FSMC_D7/FSMC_DA7, EVENTOUT	-
-	-	-	42	M9	H8	64	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, FSMC_D8/FSMC_DA8, EVENTOUT	-
-	-	-	43	L9	J8	65	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, FSMC_D9/FSMC_DA9, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
42	58	B5	92	B5	C6	136	PB6	I/O	FT	-	TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, SDIO_D0, EVENTOUT	-
43	59	A6	93	B4	D6	137	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FSMC_NL, EVENTOUT	-
44	60	D4	94	A4	D5	138	BOOT0	I	B	-	-	VPP
45	61	C5	95	A3	C5	139	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, SPI5_MOSI/I2S5_SD, CAN1_RX, I2C3_SDA, SDIO_D4, EVENTOUT	-
46	62	B6	96	B3	B5	140	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, I2C2_SDA, SDIO_D5, EVENTOUT	-
-	-	-	97	C3	A5	141	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, EVENTOUT	-
-	-	-	98	A2	A4	142	PE1	I/O	FT	-	FSMC_NBL1, EVENTOUT	-
47	63	A7	99	-	E6	-	VSS	S	-	-	-	-
-	-	C6	-	H3	E5	143	PDR_ON	I	FT	-	-	-
48	64	A8	100	-	F5	144	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F412xE/Greference manual.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

Table 10. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-	-	-	-	FSMC_NBL0	EVENTOUT
	PE1	-	-	-	-	-	-	-	-	-	-	-	FSMC_NBL1	EVENTOUT
	PE2	TRACECLK	-	-	-	-	SPI4_SCK/ I2S4_CK	SPI5_SCK/ I2S5_CK	-	-	QUADSPI_ BK1_IO2	-	FSMC_A23	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	-	-	-	-	-	FSMC_A19	EVENTOUT
	PE4	TRACED1	-	-	-	-	SPI4_NSS/ I2S4_WS	SPI5_NSS/ I2S5_WS	-	DFSDM1_ DATIN3	-	-	FSMC_A20	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	SPI4_MISO	SPI5_MISO	-	DFSDM1_ CKIN3	-	-	FSMC_A21	EVENTOUT
	PE6	TRACED3	-	-	TIM9_CH2	-	SPI4_MOSI/I 2S4_SD	SPI5_MOSI/ I2S5_SD	-	-	-	-	FSMC_A22	EVENTOUT
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_ DATIN2	-	-	-	QUADSPI_ BK2_IO0	FSMC_D4/ FSMC_DA4	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_ CKIN2	-	-	-	QUADSPI_ BK2_IO1	FSMC_D5/ FSMC_DA5	EVENTOUT
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_ CKOUT	-	-	-	QUADSPI_ BK2_IO2	FSMC_D6/ FSMC_DA6	EVENTOUT
	PE10	-	TIM1_CH2N	-	-	-	-	-	-	-	-	QUADSPI_ BK2_IO3	FSMC_D7/ FSMC_DA7	EVENTOUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS/ I2S4_WS	SPI5_NSS/ I2S5_WS	-	-	-		FSMC_D8/ FSMC_DA8	EVENTOUT
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK/ I2S4_CK	SPI5_SCK/ I2S5_CK	-	-	-	-	FSMC_D9/ FSMC_DA9	EVENTOUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	SPI5_MISO	-	-	-	-	FSMC_D10/ FSMC_DA10	EVENTOUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI/I 2S4_SD	SPI5_MOSI/ I2S5_SD	-	-	-	-	FSMC_D11/ FSMC_DA11	EVENTOUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	FSMC_D12/ FSMC_DA12	EVENTOUT

Table 31. Typical and maximum current consumption in Stop mode - V_{DD}=3.6 V

Symbol	Conditions	Parameter	Typ	Max(1)			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	124.0	179.0(2)	907.2	1762.0(2)	µA
		Low power regulator usage	52.8	104.9(2)	773.8	1559.0	
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	87.6	123.0	698.5	1374.0	
		Low power regulator usage	26.2	74.7	737.2	1515.0	
		Low power low voltage regulator usage	20.1	58.5(2)	629.1	1299.0(2)	

1. Based on characterization, not tested in production.
2. Tested in production.

Table 32. Typical and maximum current consumption in Standby mode - V_{DD}= 1.7 V

Symbol	Parameter	Conditions	Typ(1)	Max(2)			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE in low drive mode) and RTC ON	1.8	3.7	12.9	23.7	µA
		Low-speed oscillator (LSE in high drive mode) and RTC ON	2.6	4.5	13.7	24.5	
		RTC and LSE OFF	1.1	3.0	13.1	25.0	

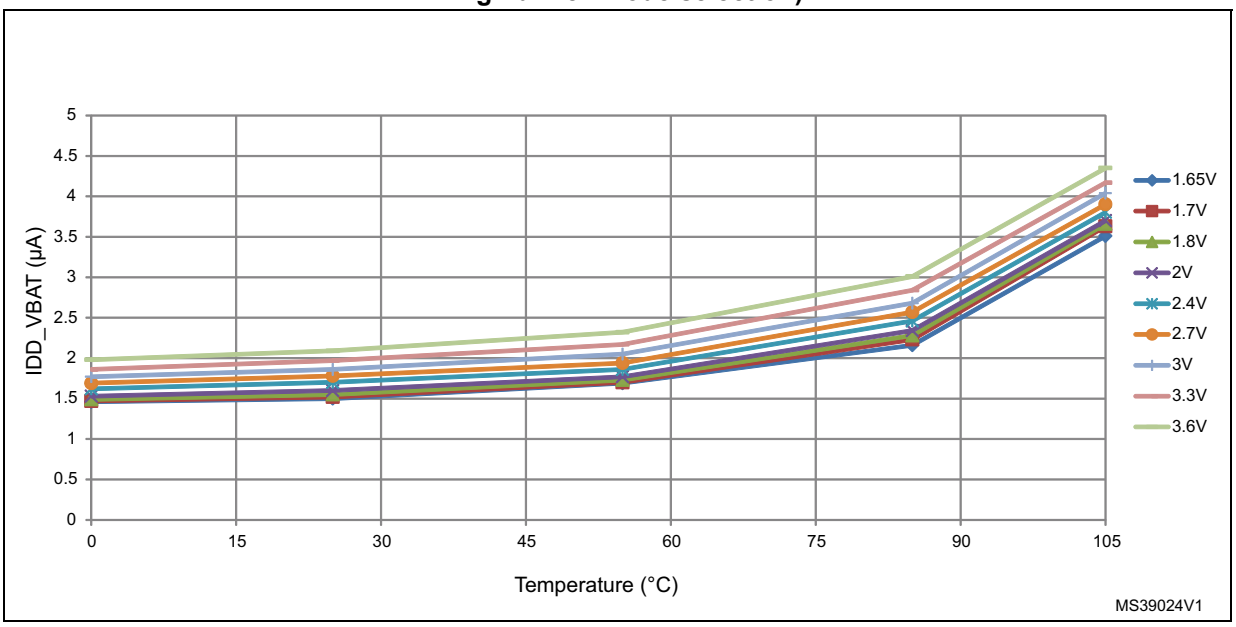
1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Based on characterization, not tested in production unless otherwise specified.

Table 33. Typical and maximum current consumption in Standby mode - V_{DD}= 3.6 V

Symbol	Parameter	Conditions	Typ(1)	Max(2)			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE in low drive mode) and RTC ON	3.7	5.4	16.0	28.4	µA
		Low-speed oscillator (LSE in high drive mode) and RTC ON	4.5	6.2	16.8	29.2	
		RTC and LSE OFF	2.6	4.0	16.0	30.0(3)	

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Guaranteed by characterization, not tested in production unless otherwise specified.
3. Tested in production.

Figure 25. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "high drive" mode selection)



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 56: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O

Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI} (2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$ (3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Figure 32. ACC_{LSI} versus temperature

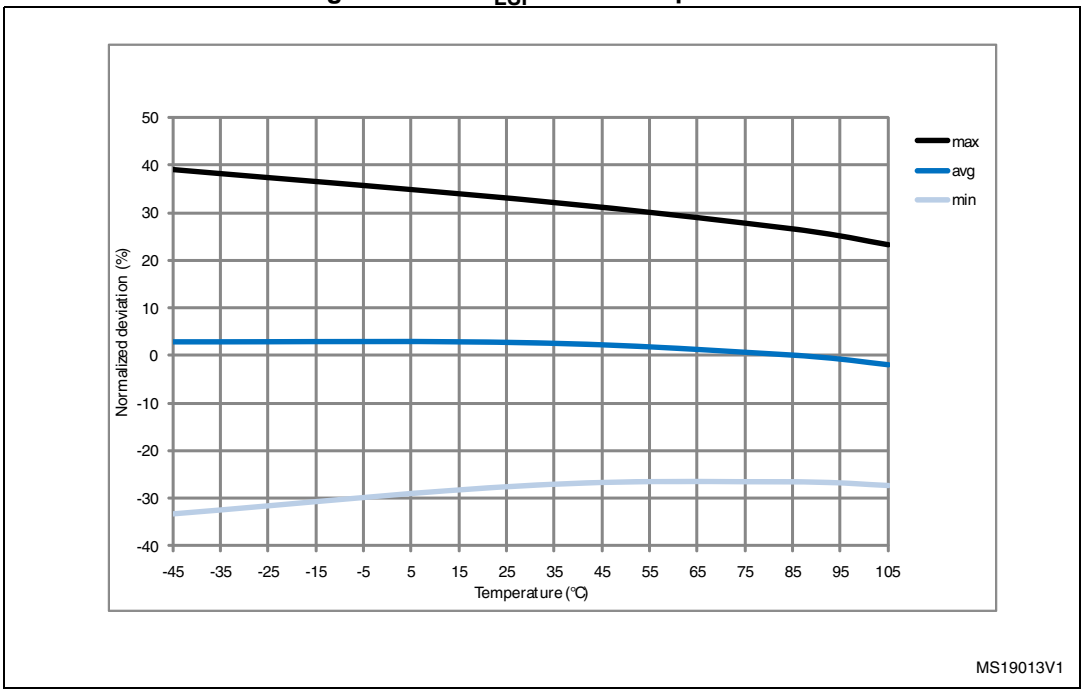


Table 45. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(1)	-		0.95(2)	1	2.10	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock	-		-	-	216	
f_{VCO_OUT}	PLLI2S VCO output	-		100	-	432	
t_{LOCK}	PLLI2S lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48 kHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design, not tested in production.
3. Value given with main PLL running.
4. Guaranteed by characterization, not tested in production.

The test results are given in *Table 52*. They are based on the EMS levels and classes defined in application note AN1709.

Table 51. EMS characteristics for LQFP144 package

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-4	4B

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP144 packages and PDR_ON on WLCSP49.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 65* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 65. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	2	-	
$t_{h(WS)}$	WS hold time	Slave mode	0.5	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	0	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	15	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	2.5	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	6	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization, not tested in production.
2. The maximum value of 256xFs is 50 MHz (APB1 maximum frequency).

Note: Refer to the I2S section of RM0383 reference manual for more details on the sampling frequency (F_S).

*f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Table 71. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S(2)	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.18.2: Internal reset OFF*).
2. Guaranteed by characterization, not tested in production.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 71*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 72. ADC accuracy at f_{ADC} = 18 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization, not tested in production.

Table 95. Dynamic characteristics: SD / MMC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	fpp =25MHz	2.5	-	-	ns
t_{IHD}	Input hold time SD	fpp =25MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	fpp =25 MHz	-	1.5	2	ns
t_{OHD}	Output hold default time SD	fpp =25 MHz	0.5	-	-	

1. Guaranteed by characterization results, not tested in production.
2. V_{DD} = 2.7 to 3.6 V.

Table 96. Dynamic characteristics: eMMC characteristics V_{DD} = 1.7 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	fpp =50MHz	3.5	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	4	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	13.5	15	ns
t_{OH}	Output hold time HS	fpp =50MHz	12	-	-	

1. Guaranteed by characterization results, not tested in production.
2. C_{LOAD} = 20 pF.

6.3.27 RTC characteristics

Table 97. RTC characteristics

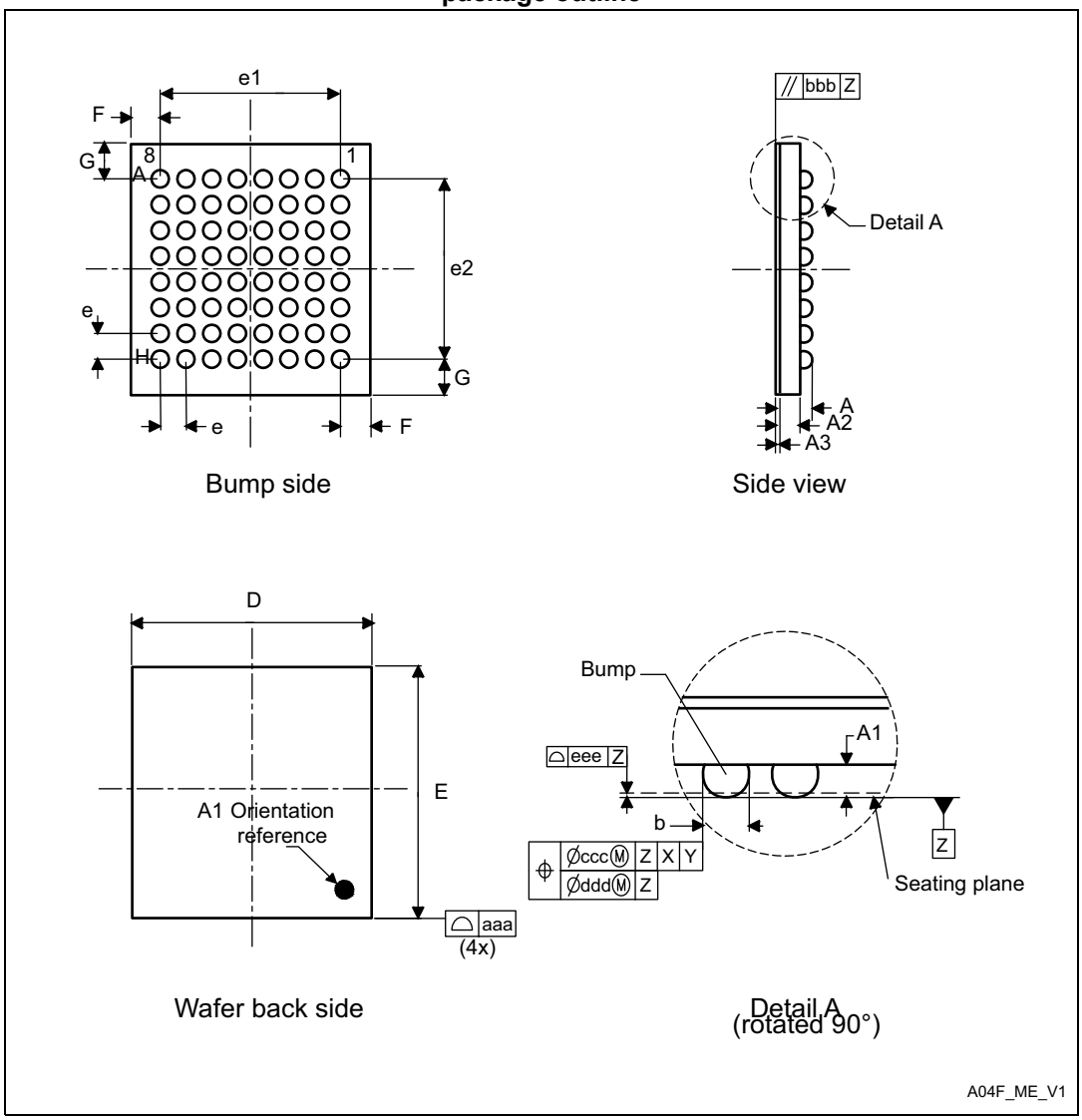
Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

7.1 WLCSP64 package information

Figure 60. WLCSP64 - 64-pin, 3.658 x 3.686 mm, 0.4 mm pitch wafer level chip scale package outline

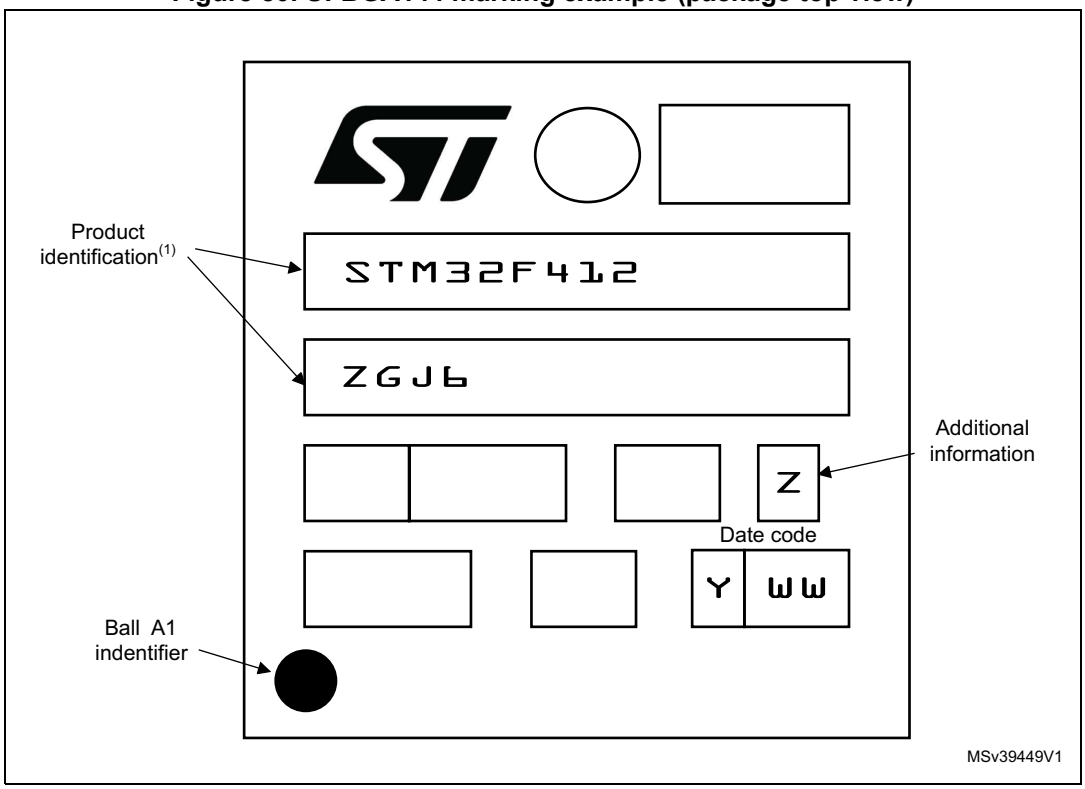


1. Drawing is not to scale.

Device marking for UFBGA144

The following figure gives an example of topside marking and ball A1 position identifier location.

Figure 80. UFBGA144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

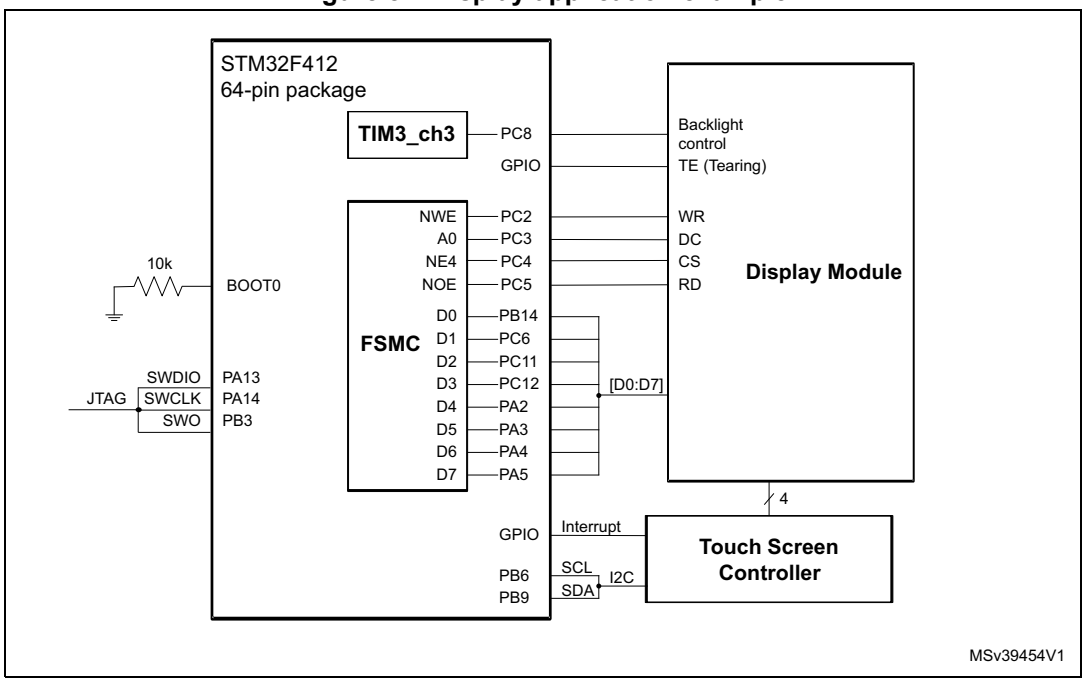
Appendix A Recommendations when using the internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on-reset (POR)/power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled. By default BOR is OFF.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

B.3 Display application example

Figure 87. Display application example



Note: 16 bit displays interfaces can be addressed with 100 and 144 pins packages.

Revision history

Table 110. Document revision history

Date	Revision	Changes
10-Nov-2015	1	Initial release.
01-Feb-2016	2	Added – *Table 3: Embedded bootloader interfaces* – *Figure 3: Compatible board design for LQFP144 package* – *Figure 62: WLCSP64 marking example (package top view)* – *Figure 77: UFBGA100 marking example (package top view)* Updated – *Section 3.17: Power supply schemes* – *Section 3.23: Timers and watchdogs* – *Section 3.32: Universal serial bus on-the-go full-speed (USB_OTG_FS)* – *Figure 1: Compatible board design for LQFP100 package* – *Figure 2: Compatible board design for LQFP64 package* – *Figure 14: STM32F412xE/G LQFP100 pinout* – *Figure 16: STM32F412xE/G UFBGA100 pinout* – *Figure 17: STM32F412xE/G UFBGA144 pinout* – *Figure 20: Input voltage measurement* – *Figure 80: UFBGA144 marking example (package top view)* – *Table 2: STM32F412xE/G features and peripheral counts* – *Table 9: STM32F412xE/G pin definition* – *Table 12: Voltage characteristics* – *Table 13: Current characteristics* – *Table 15: General operating conditions* – *Table 36: Peripheral current consumption* – *Table 51: EMS characteristics for LQFP144 package* – *Table 63: FMPI2C characteristics*