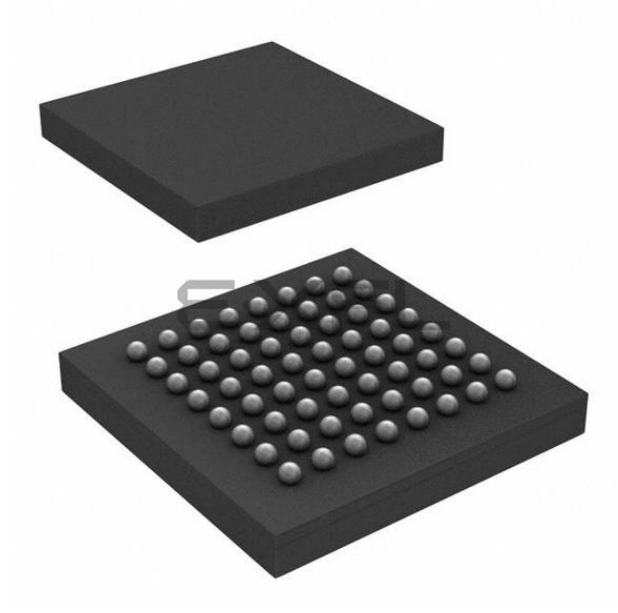

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (3.62x3.65)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412rey6tr

1 Introduction

This datasheet provides the description of the STM32F412xE/G microcontrollers.

For information on the Cortex®-M4 core, refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

3.25 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6).

These four interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. USART1 and USART6 interfaces are able to communicate at speeds of up to 12.5 Mbit/s. USART2 and USART3 interfaces communicate at up to 6.25 bit/s.

All USART interfaces provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 7. USART feature comparison

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	6.25	12.5	APB2 (max. 100 MHz)
USART2	X	X	X	X	X	X	3.12	6.25	APB1 (max. 50 MHz)
USART3	X	X	X	X	X	X	3.12	6.25	APB1 (max. 50 MHz)
USART6	X	X	X	X	X	X	6.25	12.5	APB2 (max. 100 MHz)

3.26 Serial peripheral interface (SPI)

The devices feature five SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4 and SPI5 can communicate at up to 50 Mbit/s, SPI2 and SPI3 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interfaces can be configured to operate in TI mode for communications in master mode and slave mode.

Table 9. STM32F412xE/G pin definition

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	1	B2	A3	1	PE2	I/O	FT	-	TRACECLK, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, QUADSPI_BK1_IO2, FSMC_A23, EVENTOUT	-
-	-	-	2	A1	A2	2	PE3	I/O	FT	-	TRACED0, FSMC_A19, EVENTOUT	-
-	-	-	3	B1	B2	3	PE4	I/O	FT	-	TRACED1, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, DFSDM1_DATIN3, FSMC_A20, EVENTOUT	-
-	-	-	4	C2	B3	4	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SPI5_MISO, DFSDM1_CKIN3, FSMC_A21, EVENTOUT	-
-	-	-	5	D2	B4	5	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, FSMC_A22, EVENTOUT	-
1	1	B7	6	E2	C2	6	VBAT	S	-	-	-	VBAT
2	2	B8	7	C1	A1	7	PC13	I/O	FT	(2)(3)	EVENTOUT	TAMP_1
3	3	C8	8	D1	B1	8	PC14-OSC32_IN	I/O	FT	(2)(3)(4)	EVENTOUT	OSC32_IN
4	4	C7	9	E1	C1	9	PC15-OSC32_OUT	I/O	FT	(2)(4)	EVENTOUT	OSC32_OUT
-	-	-	-	-	C3	10	PF0	I/O	FT	-	I2C2_SDA, FSMC_A0, EVENTOUT	-
-	-	-	-	-	C4	11	PF1	I/O	FT	-	I2C2_SCL, FSMC_A1, EVENTOUT	-
-	-	-	-	-	D4	12	PF2	I/O	FT	-	I2C2_SMBA, FSMC_A2, EVENTOUT	-
-	-	-	-	-	E2	13	PF3	I/O	FT	-	TIM5_CH1, FSMC_A3, EVENTOUT	-
-	-	-	-	-	E3	14	PF4	I/O	FT	-	TIM5_CH2, FSMC_A4, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	88	A5	A9	123	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, FSMC_NE1, EVENTOUT	-
-	-	-	-	-	E8	124	PG9	I/O	FT	-	USART6_RX, QUADSPI_BK2_IO2, FSMC_NE2, EVENTOUT	-
-	-	-	-	-	D8	125	PG10	I/O	FT	-	FSMC_NE3, EVENTOUT	-
-	-	-	-	-	C8	126	PG11	I/O	FT	-	CAN2_RX, EVENTOUT	-
-	-	-	-	-	B8	127	PG12	I/O	FT	-	USART6_RTS, CAN2_TX, FSMC_NE4, EVENTOUT	-
-	-	-	-	-	D7	128	PG13	I/O	FT	-	TRACED2, USART6_CTS, FSMC_A24, EVENTOUT	-
-	-	-	-	-	C7	129	PG14	I/O	FT	-	TRACED3, USART6_TX, QUADSPI_BK2_IO3, FSMC_A25, EVENTOUT	-
-	-	-	-	-	-	130	VSS	S	-	-	-	-
-	-	-	-	-	F6	131	VDD	S	-	-	-	-
-	-	-	-	-	B7	132	PG15	I/O	FT	-	USART6_CTS, EVENTOUT	-
39	55	A5	89	A8	A7	133	PB3	I/O	FT	-	JTDO-SWO, TIM2_CH2, I2CFMP1_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, I2C2_SDA, EVENTOUT	-
40	56	B4	90	A7	A6	134	PB4	I/O	FT	-	JTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, I2C3_SDA, SDIO_D0, EVENTOUT	-
41	57	C4	91	C5	B6	135	PB5	I/O	FT	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, CAN2_RX, SDIO_D3, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
42	58	B5	92	B5	C6	136	PB6	I/O	FT	-	TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, SDIO_D0, EVENTOUT	-
43	59	A6	93	B4	D6	137	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FSMC_NL, EVENTOUT	-
44	60	D4	94	A4	D5	138	BOOT0	I	B	-	-	VPP
45	61	C5	95	A3	C5	139	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, SPI5_MOSI/I2S5_SD, CAN1_RX, I2C3_SDA, SDIO_D4, EVENTOUT	-
46	62	B6	96	B3	B5	140	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, I2C2_SDA, SDIO_D5, EVENTOUT	-
-	-	-	97	C3	A5	141	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, EVENTOUT	-
-	-	-	98	A2	A4	142	PE1	I/O	FT	-	FSMC_NBL1, EVENTOUT	-
47	63	A7	99	-	E6	-	VSS	S	-	-	-	-
-	-	C6	-	H3	E5	143	PDR_ON	I	FT	-	-	-
48	64	A8	100	-	F5	144	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F412xE/Greference manual.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

Table 10. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port C	PC0	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	I2S2ext_SD	-	DFSDM1_ CKOUT	-	-	FSMC_NWE	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI/I 2S2_SD	-	-	-	-	-	FSMC_A0	EVENTOUT
	PC4	-	-	-	-	-	I2S1_MCK	-	-	-	-	QUADSPI_ BK2_IO2	FSMC_NE4	EVENTOUT
	PC5	-	-	-	-	I2CFMP1_ SMBA	-	-	USART3_RX	-	-	QUADSPI_ BK2_IO3	FSMC_NOE	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	I2CFMP1_ SCL	I2S2_MCK	DFSDM1_ CKIN3	-	USART6_ TX	-	FSMC_D1	SDIO_D6	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	I2CFMP1_ SDA	SPI2_SCK/ I2S2_CK	I2S3_MCK	-	USART6_ RX	-	DFSDM1_ DATIN3	SDIO_D7	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_ CK	QUADSPI_ BK1_IO2	-	SDIO_D0	EVENTOUT
	PC9	MCO_2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	-	-	-	QUADSPI_ BK1_IO0	-	SDIO_D1	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK/ I2S3_CK	USART3_TX	-	QUADSPI_ BK1_IO1	-	SDIO_D2	EVENTOUT
	PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO	USART3_RX	-	QUADSPI_ BK2_NCS	FSMC_D2	SDIO_D3	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/ I2S3_SD	USART3_CK	-	-	FSMC_D3	SDIO_CK	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 11. STM32F412xE/G register boundary addresses

Bus	Boundary address	Peripheral
	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex®-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
AHB3	0xA000 2000 - 0xDFFF FFFF	Reserved
	0xA000 1000 - 0xA000 1FFF	QuadSPI control register
	0xA000 0000 - 0xA000 0FFF	FSMC control register
	0x9000 0000 - 0x9FFF FFFF	QUADSPI
	0x7000 0000 - 0x08FFF FFFF	Reserved
	0x6000 0000 - 0x6FFF FFFF	FSMC
AHB2	0x5006 0C00 - 0x5FFF FFFF	Reserved
	0x5006 0800 0x5006 0BFF	RNG
	0x5004 000- 0x5006 07FF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS
AHB1	0x4002 6800 - 0x4FFF FFFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 4FFF	Reserved
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2000 - 0x4002 2FFF	Reserved
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Table 27. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	38.9	41.10	42.85	44.28	mA
			84	32.8	34.61	35.77	36.72	
			64	23.6	24.96	25.84	26.64	
			50	18.7	19.90	20.67	21.45	
			25	10.1	11.11	11.70	12.40	
			20	8.6	9.46	10.07	10.81	
		HSI, PLL OFF, all peripherals enabled	16	6.3	6.77	7.42	8.21	
			1	1.1	1.35	1.84	2.59	
		External clock, PLL ON(2) all peripherals disabled	100	24.7	26.11	27.59	28.84	
			84	21.4	22.22	23.53	24.66	
			64	15.8	16.80	17.90	18.99	
			50	12.6	13.51	14.52	15.54	
			25	7.0	7.85	8.57	9.39	
			20	6.0	6.67	7.37	8.26	
		HSI, PLL OFF, all peripherals disabled	16	4.5	4.80	5.47	6.33	
			1	0.9	1.25	1.81	2.58	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 35. Switching output I/O current consumption

Symbol	Parameter	Conditions(1)	I/O toggling frequency (f_{SW})	Typ	Unit
IDDIO	I/O switching current	V_{DD} = 3.3 V C = C_{INT}	2 MHz	0.05	mA
			8 MHz	0.15	
			25 MHz	0.45	
			50 MHz	0.85	
			60 MHz	1.00	
			84 MHz	1.40	
			90 MHz	1.67	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.10	
			8 MHz	0.35	
			25 MHz	1.05	
			50 MHz	2.20	
			60 MHz	2.40	
			84 MHz	3.55	
			90 MHz	4.23	
		V_{DD} = 3.3 V C_{EXT} =10 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.20	
			8 MHz	0.65	
			25 MHz	1.85	
			50 MHz	2.45	
			60 MHz	4.70	
			84 MHz	8.80	
			90 MHz	10.47	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.25	
			8 MHz	1.00	
			25 MHz	3.45	
			50 MHz	7.15	
			60 MHz	11.55	
		V_{DD} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.32	
			8 MHz	1.27	
			25 MHz	3.88	
			50 MHz	12.34	

1. CS is the PCB board capacitance including the pad pin. CS = 7 pF (estimated value).

Table 38. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)		1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance(1)		-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 56*. However, the recommended clock input waveform is shown in *Figure 28*.

The characteristics given in *Table 39* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 15*.

Table 39. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

The LSE high-power mode allows to cover a wider range of possible crystals but with a cost of higher power consumption.

Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	MΩ
I_{DD}	LSE current consumption	Low-power mode (default)	-	-	1	µA
		High-drive mode	-	-	3	
ACC_{LSE} (2)	LSE accuracy	-	-500	-	500	ppm
G_m_crit_max	Maximum critical crystal g_m	Startup, low-power mode	-	-	0.56	µA/V
		Startup, high-drive mode	-	-	1.50	
$t_{SU(LSE)}$ (3)	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.
2. This parameter depends on the crystal used in the application. Refer to the application note AN2867.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is guaranteed by characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

For information about the LSE high-power mode, refer to the reference manual RM0383.

Figure 30. Typical application with a 32.768 kHz crystal

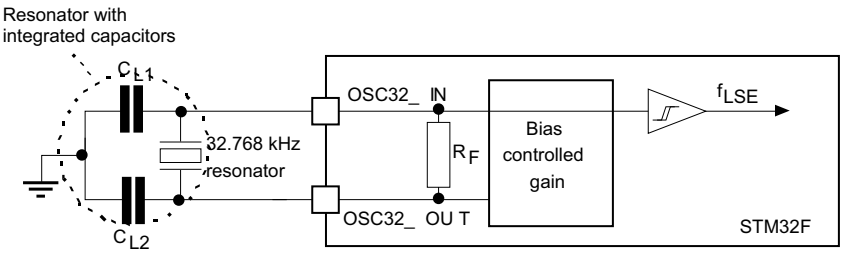


Table 45. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(1)	-		0.95(2)	1	2.10	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock	-		-	-	216	
f_{VCO_OUT}	PLLI2S VCO output	-		100	-	432	
t_{LOCK}	PLLI2S lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48 kHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design, not tested in production.
3. Value given with main PLL running.
4. Guaranteed by characterization, not tested in production.

The test results are given in *Table 52*. They are based on the EMS levels and classes defined in application note AN1709.

Table 51. EMS characteristics for LQFP144 package

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-4	4B

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP144 packages and PDR_ON on WLCSP49.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

6.3.22 V_{BAT} monitoring characteristics

Table 79. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.23 Embedded reference voltage

The parameters given in *Table 80* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

Table 80. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production

Table 81. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C V_{DDA} = 3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

Table 83. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$2T_{HCLK} – 1$	$2\ T_{HCLK} + 0.5$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0	1	
$t_{w(NOE)}$	FSMC_NOE low time	$2T_{HCLK}$ - 1.5	$2T_{HCLK}$	
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	1.5	
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	T_{HCLK} - 1	-	
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	T_{HCLK} - 1	-	
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	0	
$t_{w(NADV)}$	FSMC_NADV low time	-	$T_{HCLK} + 0.5$	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Table 84. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7T_{HCLK}$ - 1	$7T_{HCLK} + 0.5$	ns
$t_{w(NOE)}$	FSMC_NWE low time	$5T_{HCLK} – 1.5$	$5T_{HCLK}$	
$t_{w(NWAIT)}$	FSMC_NWAIT low time	$T_{HCLK} – 0.5$	-	
$t_{su(NWAIT\_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$5T_{HCLK}$ -1	-	
$t_{h(NE\_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4T_{HCLK} + 1$	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 56. Synchronous non-multiplexed NOR/PSRAM read timings

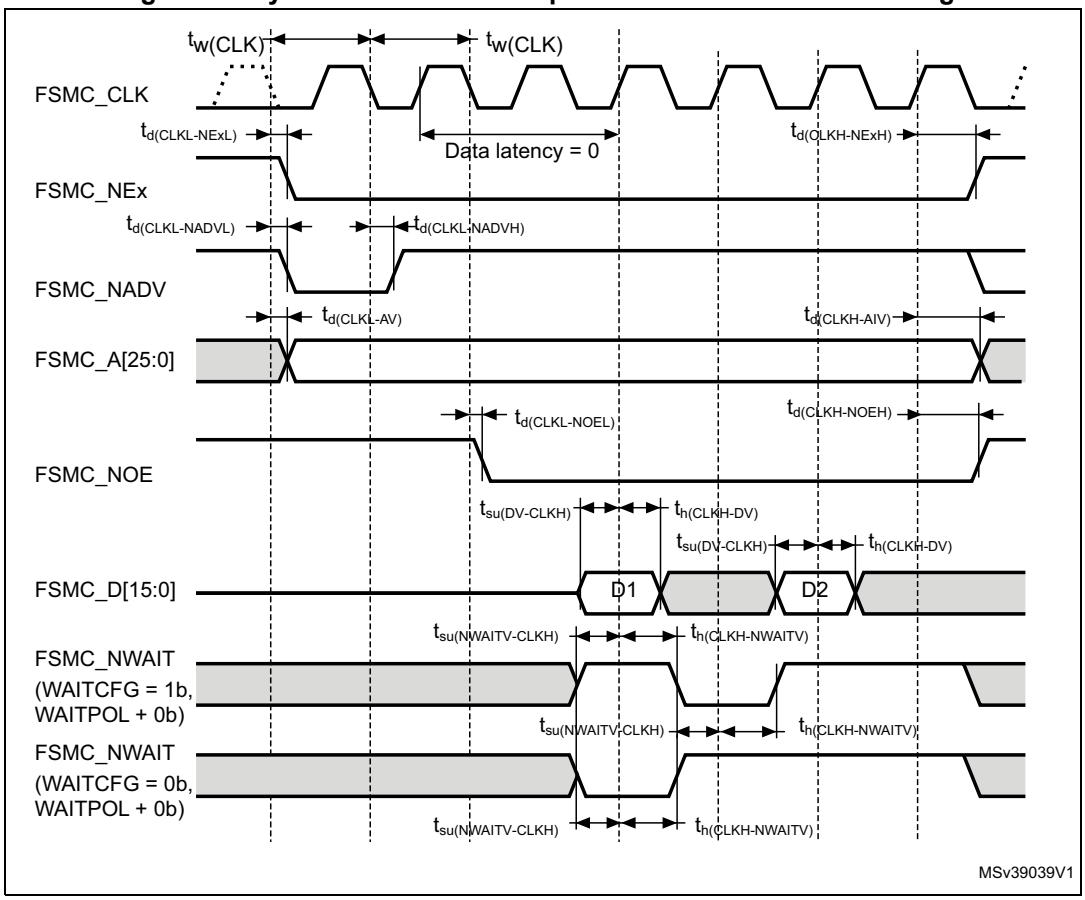


Table 93. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

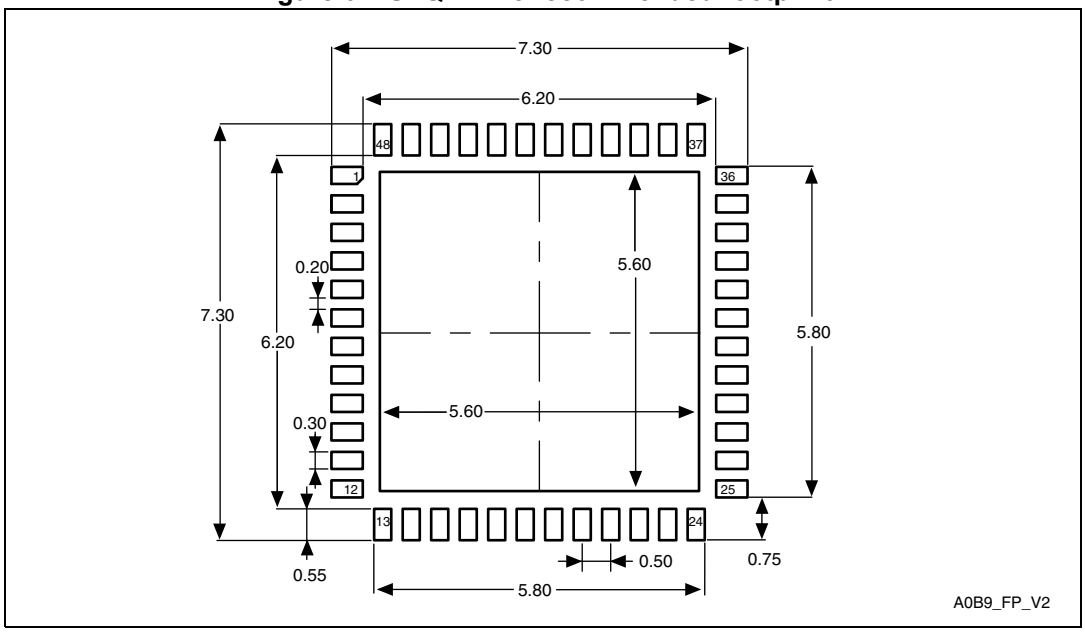
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK} - 0.5$	-	ns
$t_{(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} +0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	T_{HCLK}	-	
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	1	-	
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	2	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

Table 100. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

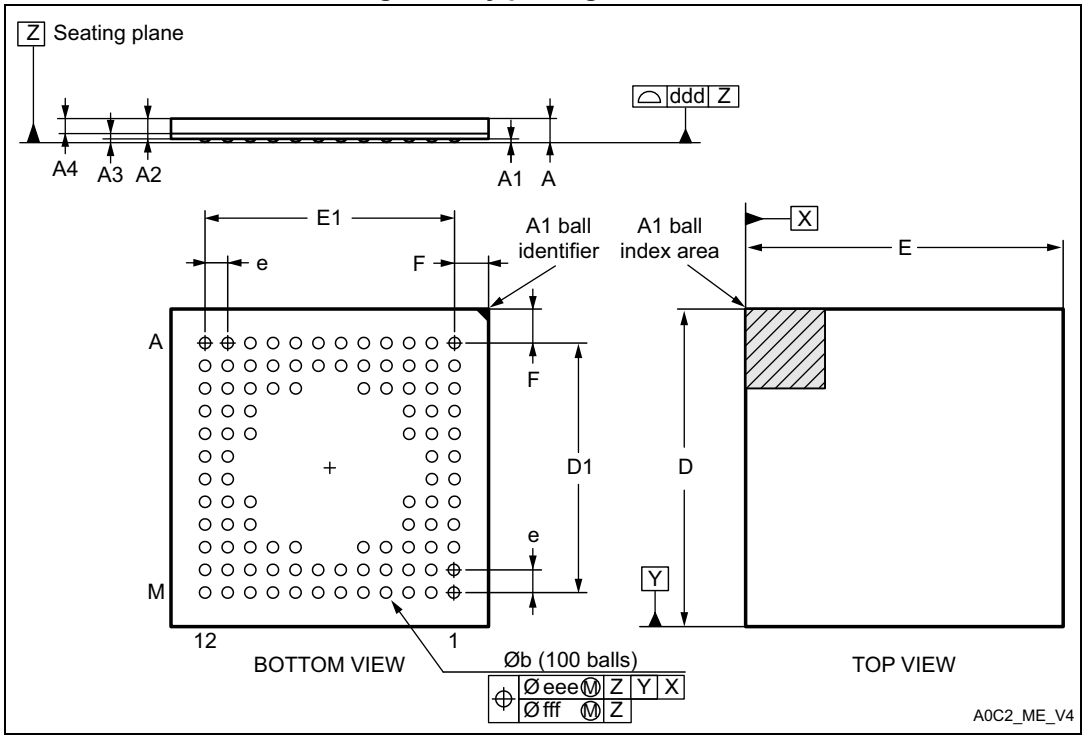
Figure 64. UFQFPN48 recommended footprint



1. Dimensions are in millimeters.

7.6 UFBGA100 package information

Figure 75. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 104. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315