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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412rgt6

1 Introduction

This datasheet provides the description of the STM32F412xE/G microcontrollers.

For information on the Cortex®-M4 core, refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

3.23.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1/8) can be seen as three-phase PWM generator multiplexed on 4 independent channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as a 16-bit PWM generator, they have full modulation capability (0-100%).

The advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.23.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F412xE/G (see *Table 5* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F412xE/G devices include 4 full-featured general-purpose timers: TIM2. TIM3, TIM4 and TIM5. TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter plus a 16-bit prescaler. They all features four independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 15 input capture/output compare/PWMs

  TIM2. TIM3, TIM4 and TIM5 general-purpose timers can operate together or in conjunction with the other general-purpose timers and TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM output.

  TIM2. TIM3, TIM4 and TIM5 channels have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13 and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13 and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with TIM2. TIM3, TIM4 and TIM5 full-featured general-purpose timers or used as simple time bases.

3.23.3 Basic timer (TIM6, TIM7)

TIM6 and TIM7 timers are basic 16-bit timers. They support independent DMA request generation.

3.38 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F412xE/G through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using any high-speed channel available. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	51	C3	78	B11	B11	111	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, QUADSPI_BK1_IO1, SDIO_D2, EVENTOUT	-
-	52	B3	79	C10	B10	112	PC11	I/O	FT	-	I2S3ext_SD, SPI3_MISO, USART3_RX, QUADSPI_BK2_NCS, FSMC_D2, SDIO_D3, EVENTOUT	-
-	53	A3	80	B10	C10	113	PC12	I/O	FT	-	SPI3_MOSI/I2S3_SD, USART3_CK, FSMC_D3, SDIO_CK, EVENTOUT	-
-	-	-	81	C9	E10	114	PD0	I/O	FT	-	CAN1_RX, FSMC_D2/FSMC_DA2, EVENTOUT	-
-	-	-	82	B9	D10	115	PD1	I/O	FT	-	CAN1_TX, FSMC_D3/FSMC_DA3, EVENTOUT	-
-	54	A4	83	C8	E9	116	PD2	I/O	FT	-	TIM3_ETR, FSMC_NWE, SDIO_CMD, EVENTOUT	-
-	-	-	84	B8	D9	117	PD3	I/O	FT	-	TRACED1, SPI2_SCK/I2S2_CK, DFSDM1_DATIN0, USART2_CTS, QUADSPI_CLK, FSMC_CLK, EVENTOUT	-
-	-	-	85	B7	C9	118	PD4	I/O	FT	-	DFSDM1_CKIN0, USART2_RTS, FSMC_NOE, EVENTOUT	-
-	-	-	86	A6	B9	119	PD5	I/O	FT	-	USART2_TX, FSMC_NWE, EVENTOUT	-
-	-	-	-	-	E7	120	VSS	S	-	-	-	-
-	-	-	-	-	F7	121	VDD	S	-	-	-	-
-	-	-	87	B6	A8	122	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, DFSDM1_DATIN1, USART2_RX, FSMC_NWAIT, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

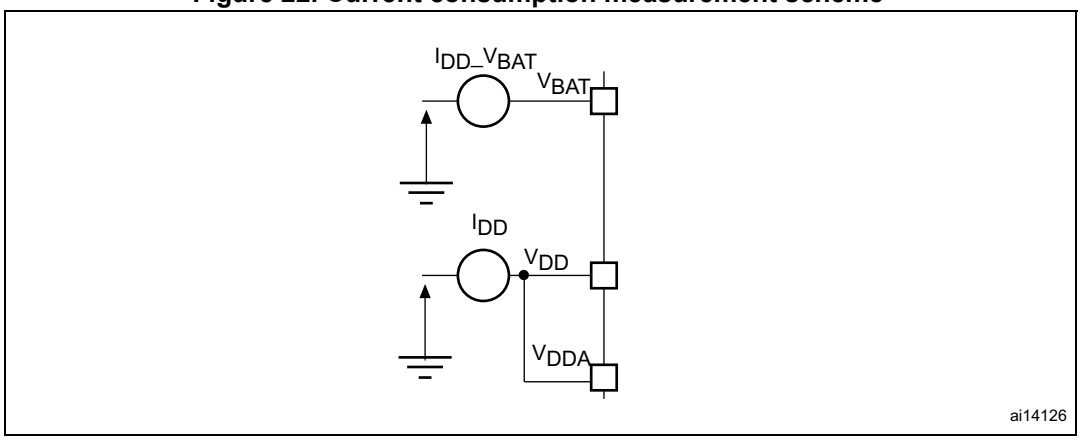
Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	88	A5	A9	123	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, FSMC_NE1, EVENTOUT	-
-	-	-	-	-	E8	124	PG9	I/O	FT	-	USART6_RX, QUADSPI_BK2_IO2, FSMC_NE2, EVENTOUT	-
-	-	-	-	-	D8	125	PG10	I/O	FT	-	FSMC_NE3, EVENTOUT	-
-	-	-	-	-	C8	126	PG11	I/O	FT	-	CAN2_RX, EVENTOUT	-
-	-	-	-	-	B8	127	PG12	I/O	FT	-	USART6_RTS, CAN2_TX, FSMC_NE4, EVENTOUT	-
-	-	-	-	-	D7	128	PG13	I/O	FT	-	TRACED2, USART6_CTS, FSMC_A24, EVENTOUT	-
-	-	-	-	-	C7	129	PG14	I/O	FT	-	TRACED3, USART6_TX, QUADSPI_BK2_IO3, FSMC_A25, EVENTOUT	-
-	-	-	-	-	-	130	VSS	S	-	-	-	-
-	-	-	-	-	F6	131	VDD	S	-	-	-	-
-	-	-	-	-	B7	132	PG15	I/O	FT	-	USART6_CTS, EVENTOUT	-
39	55	A5	89	A8	A7	133	PB3	I/O	FT	-	JTDO-SWO, TIM2_CH2, I2CFMP1_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, I2C2_SDA, EVENTOUT	-
40	56	B4	90	A7	A6	134	PB4	I/O	FT	-	JTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, I2C3_SDA, SDIO_D0, EVENTOUT	-
41	57	C4	91	C5	B6	135	PB5	I/O	FT	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, CAN2_RX, SDIO_D3, EVENTOUT	-

Table 11. STM32F412xE/G register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 6400- 0x4001 FFFF	Reserved
	0x4001 6000 - 0x4001 63FF	DFSDM1
	0x4001 5400 - 0x4001 5FFF	Reserved
	0x4001 5000 - 0x4001 53FF	SPI5/I2S5
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4/I2S4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7400 - 0x4000 FFFF	Reserved

6.1.7 Current consumption measurement

Figure 22. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 12: Voltage characteristics*, *Table 13: Current characteristics*, and *Table 14: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 12. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD}, V_{DDUSB} and V_{BAT})(1)	–0.3	4.0	V
V_{IN}	Input voltage on FT and TC pins(2)	V_{SS}–0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
	Input voltage for BOOT0	V_{SS}	9.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.14: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}, V_{DDUSB}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 13* for the values of the maximum allowed injected current.

Table 26. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	35.9	38.55	40.77	42.52	mA
			84	29.4	31.59	33.12	34.42	
			64	22.4	24.02	25.15	26.28	
			50	18.6	20.07	21.08	22.05	
			25	10.3	11.62	12.39	13.34	
			20	8.9	9.85	10.59	11.32	
		HSI, PLL OFF, all peripherals enabled(2)(3)	16	6.7	7.26	8.04	8.80	
			1	1.1	1.44	1.99	2.66	
		External clock, PLL ON(3) all peripherals disabled	100	21.7	23.55	25.48	27.07	
			84	18.0	19.16	20.93	22.39	
			64	14.6	15.93	17.32	18.59	
			50	12.5	13.63	14.90	16.07	
			25	7.2	8.25	9.26	10.26	
			20	6.3	7.15	7.99	8.84	
		HSI, PLL OFF, all peripherals disabled(3)	16	4.9	5.37	6.20	7.03	
			1	1.0	1.30	1.91	2.65	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.

Table 27. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	38.9	41.10	42.85	44.28	mA
			84	32.8	34.61	35.77	36.72	
			64	23.6	24.96	25.84	26.64	
			50	18.7	19.90	20.67	21.45	
			25	10.1	11.11	11.70	12.40	
			20	8.6	9.46	10.07	10.81	
		HSI, PLL OFF, all peripherals enabled	16	6.3	6.77	7.42	8.21	
			1	1.1	1.35	1.84	2.59	
		External clock, PLL ON(2) all peripherals disabled	100	24.7	26.11	27.59	28.84	
			84	21.4	22.22	23.53	24.66	
			64	15.8	16.80	17.90	18.99	
			50	12.6	13.51	14.52	15.54	
			25	7.0	7.85	8.57	9.39	
			20	6.0	6.67	7.37	8.26	
		HSI, PLL OFF, all peripherals disabled	16	4.5	4.80	5.47	6.33	
			1	0.9	1.25	1.81	2.58	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 29. Typical and maximum current consumption in Sleep mode - V_{DD} = 1.7 V (continued)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Sleep mode**	All peripherals disabled, External clock, PLL ON(2), Flash deep power down	100	2.9	3.51	4.14	4.90	mA
			84	2.4	2.83	3.46	4.16	
			64	1.7	2.08	2.59	3.18	
			50	1.4	1.77	2.23	2.84	
			25	1.0	1.37	1.88	2.50	
			20	1.3	1.37	1.88	2.50	
		All peripherals disabled, HSI, PLL OFF(2), Flash deep power down	16	0.5	0.63	1.23	1.91	
			1	0.4	0.52	1.13	1.81	
		All peripherals disabled, External clock, PLL ON(2), Flash ON	100	3.3	3.22	3.98	4.90	
			84	2.8	2.62	3.30	4.16	
			64	2.1	1.89	2.50	3.18	
			50	1.7	1.58	2.16	2.84	
			25	1.2	1.28	1.82	2.50	
			20	1.3	1.28	1.82	2.50	
		All peripherals disabled, HSI, PLL OFF(2), Flash ON	16	0.8	0.88	1.36	1.91	
			1	0.7	0.77	1.26	1.81	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 30. Typical and maximum current consumptions in Stop mode - V_{DD} = 1.7 V

Symbol	Conditions	Parameter	Typ(1)	Max(1)			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	121.1	168.0	648.7	1213.0	µA
		Low power regulator usage	50.8	104.7	667.4	1328.0	
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	79.1	122.0	609.1	1181.0	
		Low power regulator usage	22.4	74.7	631.9	1286.0	
		Low power low voltage regulator usage	18.5	58.5	558.3	1145.0	

1. Based on characterization, not tested in production.

Table 34. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions[1]	Typ				Max[2]		Unit
			T_A = 25 °C				T_A = 85 °C	T_A = 105 °C	
			V_{BAT} = 1.7 V	V_{BAT}= 2.4 V	V_{BAT} = 3.3 V	V_{BAT} = 3.6 V	V_{BAT} = 3.6 V		
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator (LSE in low-drive mode) and RTC ON	0.74	0.87	1.04	1.11	3.0	5.0	µA
		Low-speed oscillator (LSE in high-drive mode) and RTC ON	1.52	1.70	1.97	2.09	3.8	5.8	
		RTC and LSE OFF	0.04	0.04	0.05	0.05	2.0	4.0	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization, not tested in production.

Figure 24. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "low power" mode selection)

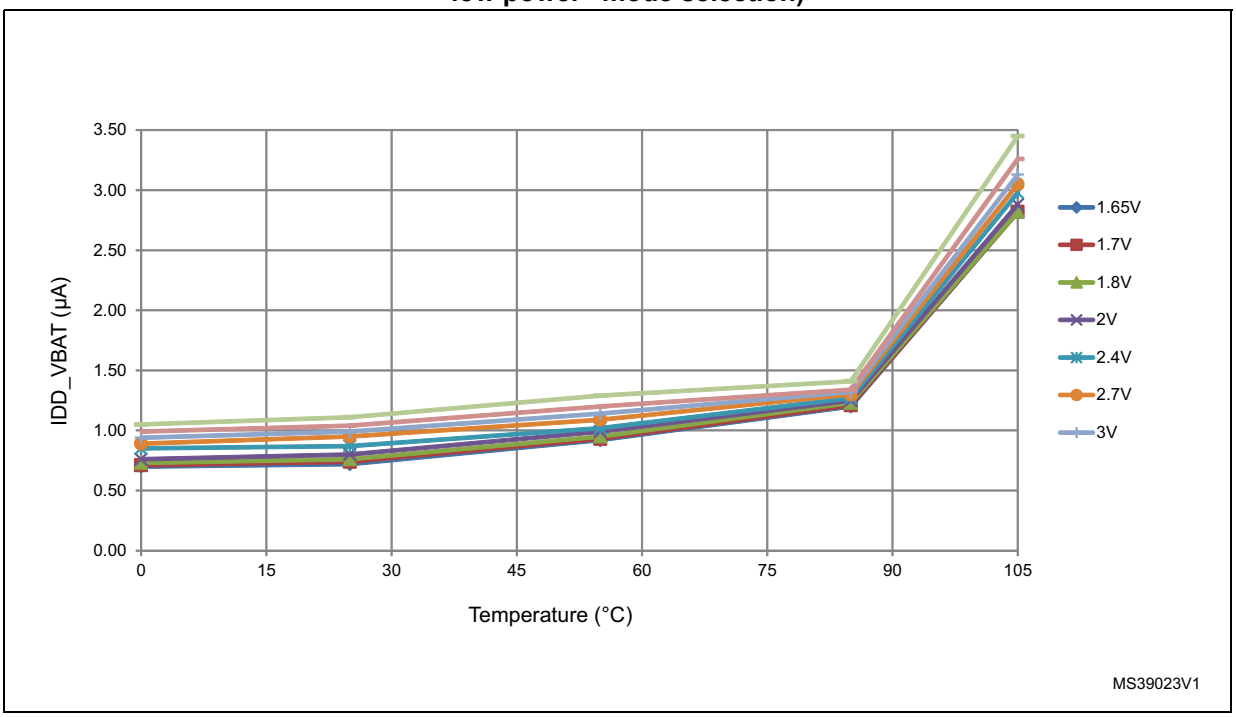


Table 71. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S(2)	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.18.2: Internal reset OFF*).
2. Guaranteed by characterization, not tested in production.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 71*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 72. ADC accuracy at f_{ADC} = 18 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization, not tested in production.

Figure 56. Synchronous non-multiplexed NOR/PSRAM read timings

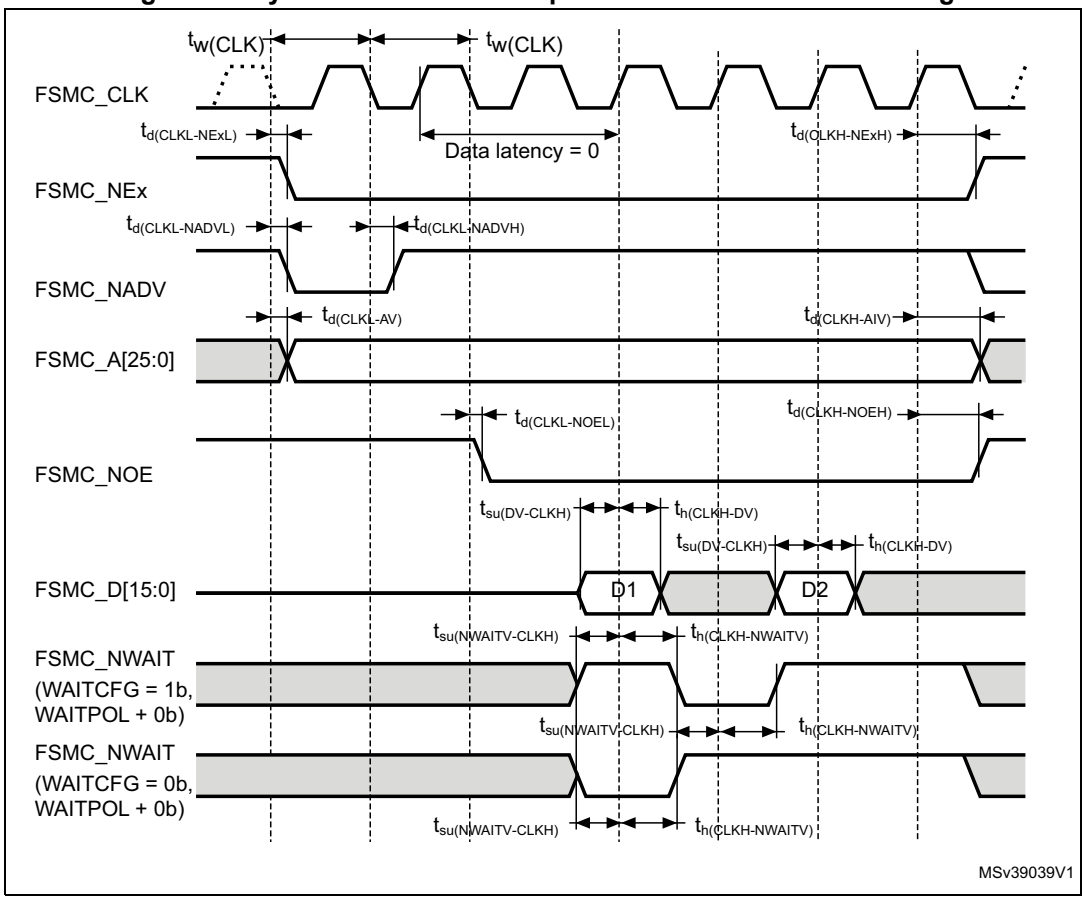


Table 93. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK} - 0.5$	-	ns
$t_{(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} +0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	T_{HCLK}	-	
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	1	-	
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	2	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

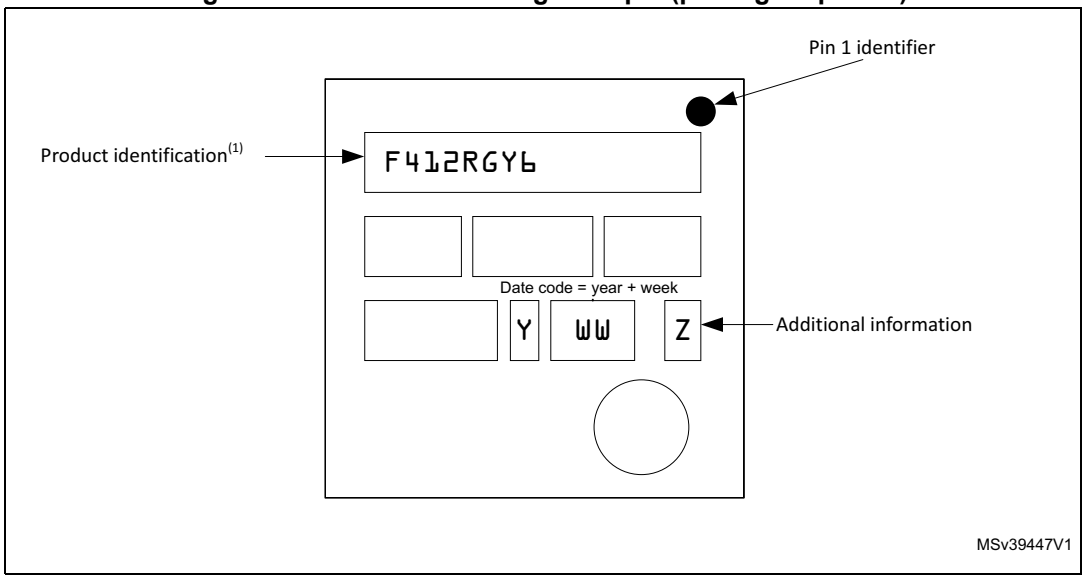
Table 99. WLCSP64 recommended PCB design rules (0.4 mm pitch) (continued)

Dimension	Recommended values
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking for WLCSP64

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 62. WLCSP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 101. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 103. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

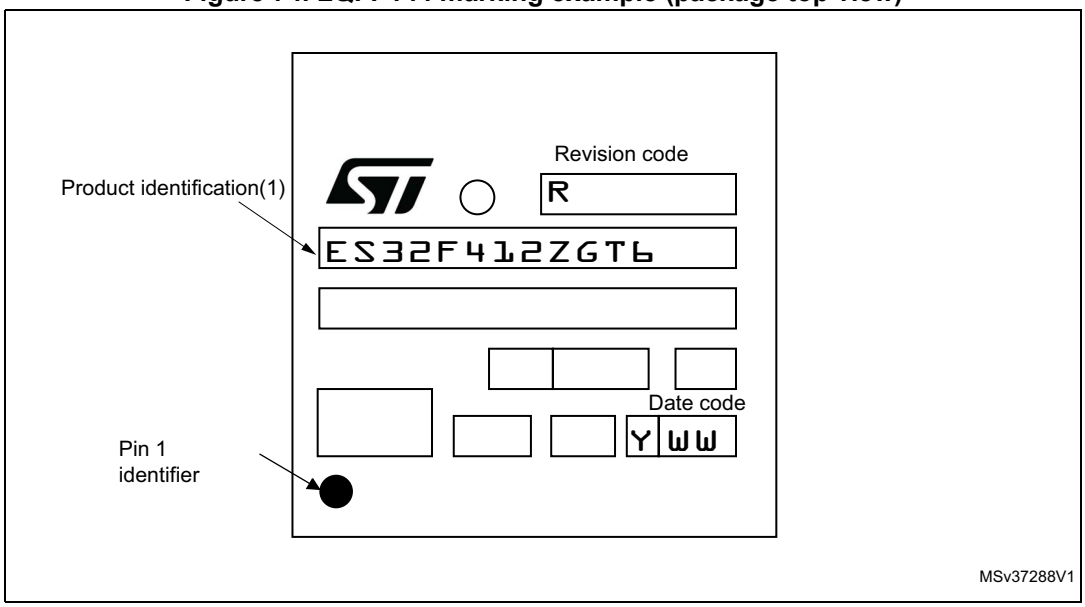
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking for LQFP144

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 74. LQFP144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

8 Part numbering

Table 109. Ordering information scheme

Example: STM32 F 412 C E T 6 TR

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = General-purpose

Device subfamily

412 = 412 line

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Z = 144 pins

Flash memory size

E = 512 Kbytes of Flash memory

G = 1024 Kbytes of Flash memory

Package

H = UFBGA 7 x 7 mm

J = UFBGA 10 x 10 mm

T = LQFP

U = UFQFPN

Y = WLCSP

Temperature range

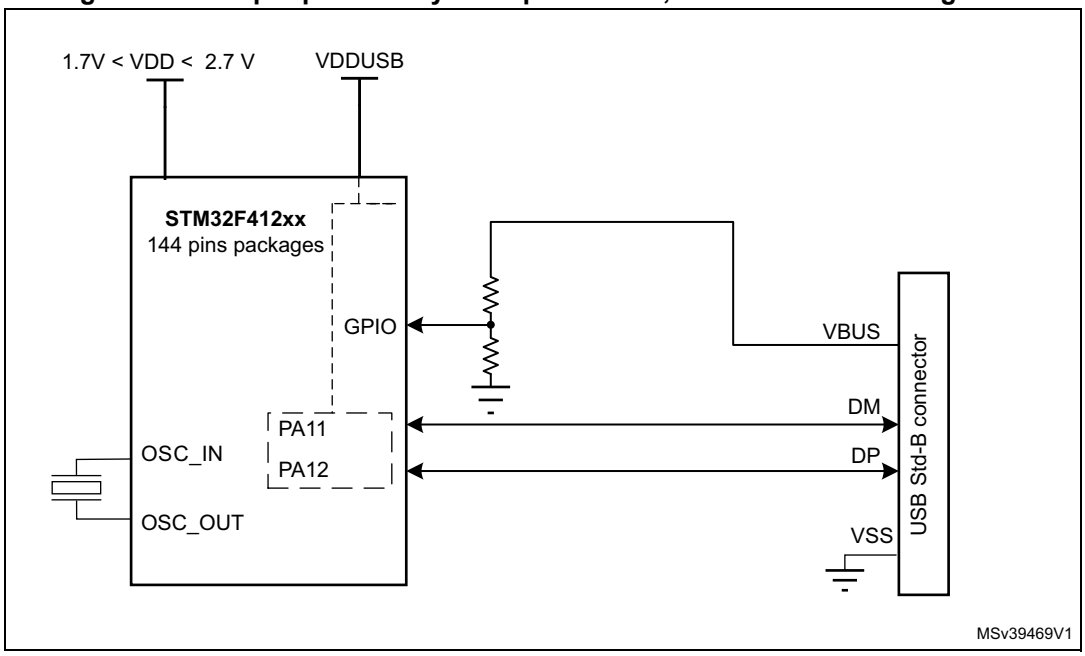
6 = Industrial temperature range, –40 to 85 °C

Packing

TR = tape and reel

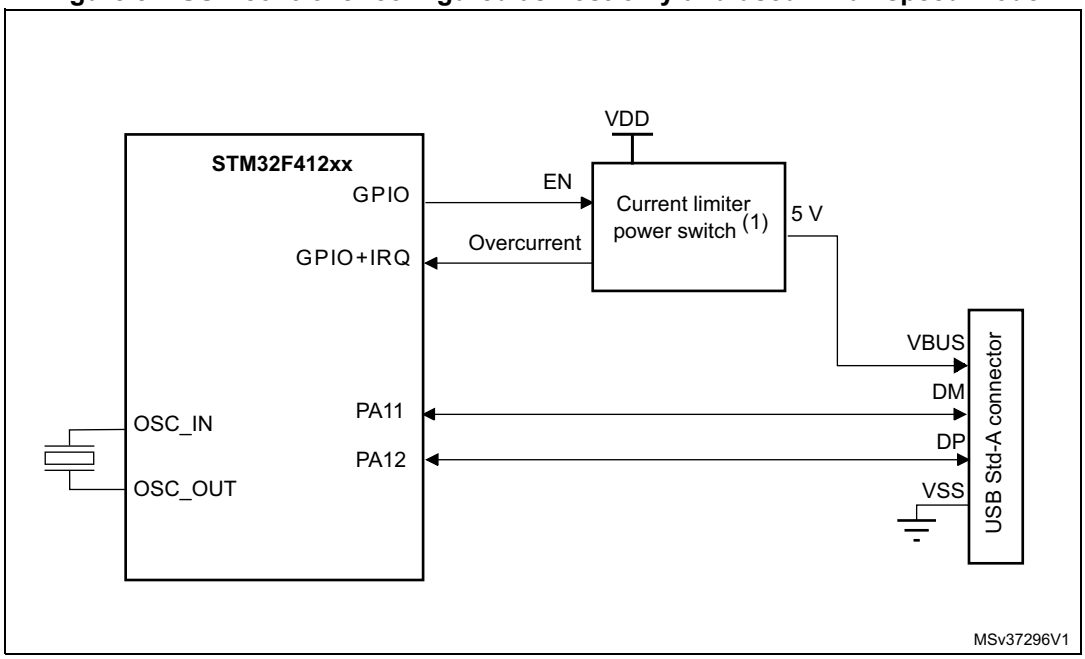
No character = tray or tube

Figure 83. USB peripheral-only Full speed mode, VBUS detection using GPIO



1. External voltage regulator only needed when building a V_{BUS} powered device.

Figure 84. USB controller configured as host-only and used in full speed mode



1. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.