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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412rgt6tr

Contents

List of tables

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
27	35	G1	53	K11	L11	75	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, I2CFMP1_SDA, SPI2_MISO, I2S2ext_SD, USART3_RTS, DFSDM1_DATIN2, TIM12_CH1, FSMC_D0, SDIO_D6, EVENTOUT	-
28	36	F2	54	K10	L12	76	PB15	I/O	FT	-	RTC_50Hz, TIM1_CH3N, TIM8_CH3N, I2CFMP1_SCL, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, TIM12_CH2, SDIO_CK, EVENTOUT	-
-	-	-	55	-	L9	77	PD8	I/O	FT	-	USART3_TX, FSMC_D13/ FSMC_DA13, EVENTOUT	-
-	-	-	56	K8	K9	78	PD9	I/O	FT	-	USART3_RX, FSMC_D14/FSMC_DA14, EVENTOUT	-
-	-	-	57	J12	J9	79	PD10	I/O	FT	-	USART3_CK, FSMC_D15/FSMC_DA15, EVENTOUT	-
-	-	-	58	J11	H9	80	PD11	I/O	FT	-	I2CFMP1_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FSMC_A16, EVENTOUT	-
-	-	-	59	J10	L10	81	PD12	I/O	FT	-	TIM4_CH1, I2CFMP1_SCL, USART3_RTS, QUADSPI_BK1_IO1, FSMC_A17, EVENTOUT	-
-	-	-	60	H12	K10	82	PD13	I/O	FT	-	TIM4_CH2, I2CFMP1_SDA, QUADSPI_BK1_IO3, FSMC_A18, EVENTOUT	-
-	-	-	-	-	G8	83	VSS	S	-	-	-	-
-	-	-	-	-	F8	84	VDD	S	-	-	-	-

Table 10. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	FSMC_D2/FSMC_DA2	EVENTOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	FSMC_D3/FSMC_DA3	EVENTOUT
	PD2	-	-	TIM3_ETR	-	-	-	-	-	-	-	FSMC_NWE	SDIO_CMD	EVENTOUT
	PD3	TRACED1	-	-	-	-	SPI2_SCK/ I2S2_CK	DFSDM1_ DATIN0	USART2_ CTS	-	QUADSPI_ CLK	-	FSMC_CLK	EVENTOUT
	PD4	-	-	-	-	-	-	DFSDM1_ CKIN0	USART2_ RTS	-	-	-	FSMC_NOE	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	FSMC_NWE	EVENTOUT
	PD6	-	-	-	-	-	SPI3_MOSI/I 2S3_SD	DFSDM1_ DATIN1	USART2_RX	-	-	-	FSMC_ NWAIT	EVENTOUT
	PD7	-	-	-	-	-	-	DFSDM1_ CKIN1	USART2_CK	-	-	-	FSMC_NE1	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	FSMC_D13/ FSMC_DA13	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	FSMC_D14/ FSMC_DA14	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	FSMC_D15/ FSMC_DA15	EVENTOUT
	PD11	-	-	-	-	I2CFMP1_ SMBA	-	-	USART3_ CTS	-	QUADSPI_ BK1_IO0	-	FSMC_A16	EVENTOUT
	PD12	-	-	TIM4_CH1	-	I2CFMP1_ SCL			USART3_ RTS	-	QUADSPI_ BK1_IO1	-	FSMC_A17	EVENTOUT
	PD13	-	-	TIM4_CH2	-	I2CFMP1_ SDA	-	-	-	-	QUADSPI_ BK1_IO3	-	FSMC_A18	EVENTOUT
	PD14	-	-	TIM4_CH3	-	I2CFMP1_ SCL	-	-	-	-	-	-	FSMC_D0/ FSMC_DA0	EVENTOUT
	PD15	-	-	TIM4_CH4	-	I2CFMP1_ SDA	-	-	-	-	-	-	FSMC_D1/ FSMC_DA1	EVENTOUT

Table 11. STM32F412xE/G register boundary addresses

Bus	Boundary address	Peripheral
	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex®-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
AHB3	0xA000 2000 - 0xDFFF FFFF	Reserved
	0xA000 1000 - 0xA000 1FFF	QuadSPI control register
	0xA000 0000 - 0xA000 0FFF	FSMC control register
	0x9000 0000 - 0x9FFF FFFF	QUADSPI
	0x7000 0000 - 0x08FFF FFFF	Reserved
	0x6000 0000 - 0x6FFF FFFF	FSMC
AHB2	0x5006 0C00 - 0x5FFF FFFF	Reserved
	0x5006 0800 0x5006 0BFF	RNG
	0x5004 000- 0x5006 07FF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS
AHB1	0x4002 6800 - 0x4FFF FFFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 4FFF	Reserved
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2000 - 0x4002 2FFF	Reserved
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Table 22. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A= 25 °C	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	28.4	28.80(3)	30.84	32.39(3)	mA
			84	23.0	24.09(3)	25.20	26.57(3)	
			64	16.0	16.83(3)	17.77	19.12(3)	
			50	12.6	13.46	13.98	14.68	
			25	6.8	7.63	8.14	8.61	
			20	5.8	6.31	6.74	7.43	
		HSI, PLL OFF(4), all peripherals enabled(2)	16	3.9	4.65	5.33	6.11	
			1	0.6	0.78	1.34	2.00	
		External clock, PLL ON, all peripherals disabled(2)	100	14.3	15.09(3)	16.22	17.90(3)	
			84	11.6	12.28(3)	13.36	14.99(3)	
			64	8.2	8.75(3)	9.68	11.21(3)	
			50	6.5	7.21	7.69	8.47	
			25	3.6	4.22	4.68	5.29	
			20	3.2	3.65	4.18	4.94	
		HSI, PLL OFF, all peripherals disabled(2)	16	2.0	2.48	3.12	3.94	
			1	0.5	0.65	1.26	1.94	

1. Based on characterization, not tested in production unless otherwise specified
2. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
3. Tested in production
4. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 64* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

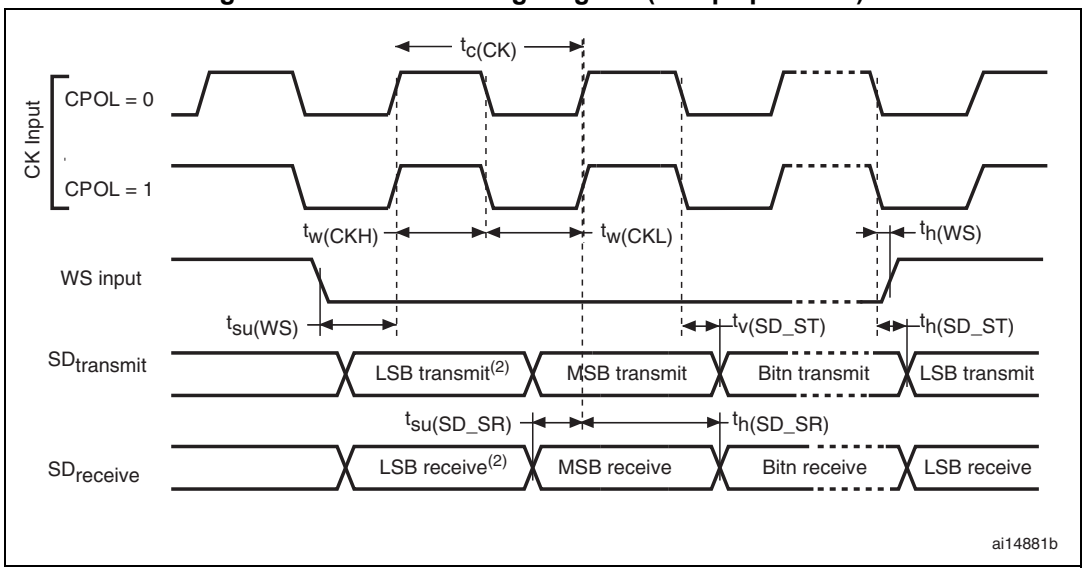
- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 64. SPI dynamic characteristics(1)

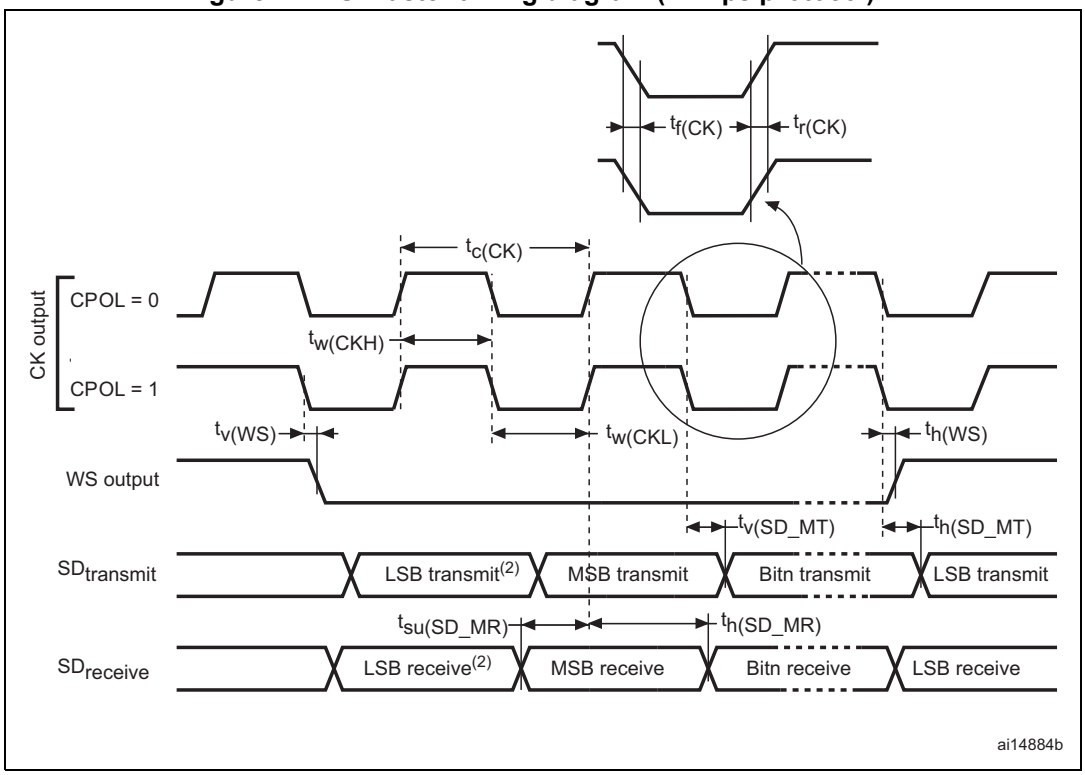
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master full duplex/receiver mode, 2.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	MHz
		Master transmitter mode 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Master mode 1.7 V < V_{DD} < 3.6 V SPI1/2/3/4/5	-	-	25	
		Slave transmitter/full duplex mode 2.7 V < V_{DD} < 3.6 V SPI1//4/5	-	-	50	
		Slave transmitter/full duplex mode 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	35(2)	
		Slave receiver mode, 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Slave mode, 1.7 V < V_{DD} < 3.6 V SPI2/3	-	-	25	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, SPI presc = 2	T_{PCLK}-1.5	T_{PCLK}	T_{PCLK} +1.5	ns
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$3T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2T_{PCLK}$	-	-	ns
$t_{su(MI)}$	Data input setup time	Master mode	4.5	-	-	ns
$t_{su(SI)}$		Slave mode	1.5	-	-	ns
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	ns
$t_{h(SI)}$		Slave mode	0.5	-	-	ns

Figure 43. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 44. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 71* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 15*.

Table 71. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	V_{DDA} –V_{REF+} < 1.2 V	1.7(1)	-	3.6	V
V_{REF+}	Positive reference voltage		1.7(1)	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	V_{DDA} = 1.7(1) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance	-	-	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	4	7	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Table 73. ADC accuracy at f_{ADC} = 30 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V, V_{DDA} –V_{REF} < 1.2 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±4	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization, not tested in production.

Table 74. ADC accuracy at f_{ADC} = 36 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V V_{DDA} –V_{REF} < 1.2 V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization, not tested in production.

Table 75. ADC dynamic accuracy at f_{ADC} = 18 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =18 MHz V_{DDA} = V_{REF+}= 1.7 V Input Frequency = 20 kHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		-	-72	-67	

1. Guaranteed by characterization, not tested in production.

Table 76. ADC dynamic accuracy at f_{ADC} = 36 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 36 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 20 kHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		-	-72	-70	

1. Guaranteed by characterization, not tested in production.

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics.

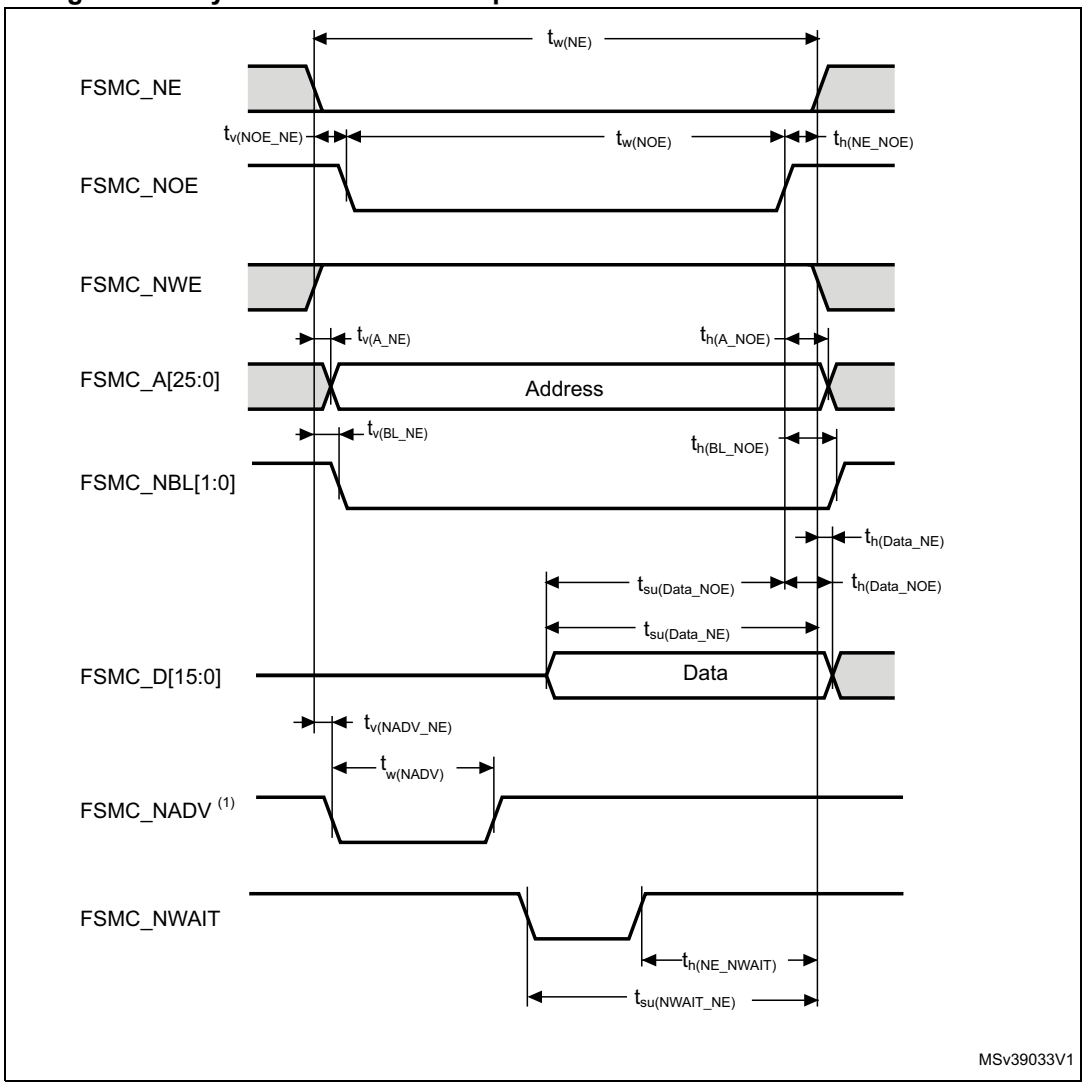
Asynchronous waveforms and timings

Figure 50 through *Figure 53* represent asynchronous waveforms and *Table 83* through *Table 90* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 50. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Table 86. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$8T_{HCLK}$ - 1	$8T_{HCLK}$ + 0.5	ns
$t_{w(NWE)}$	FSMC_NWE low time	$6T_{HCLK}$ + 0.5	$6T_{HCLK}$ + 1	
$t_{su(NWAIT\_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$6T_{HCLK}$ + 0.5	-	
$t_{h(NE\_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4T_{HCLK}$ + 1	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 52. Asynchronous multiplexed PSRAM/NOR read waveforms

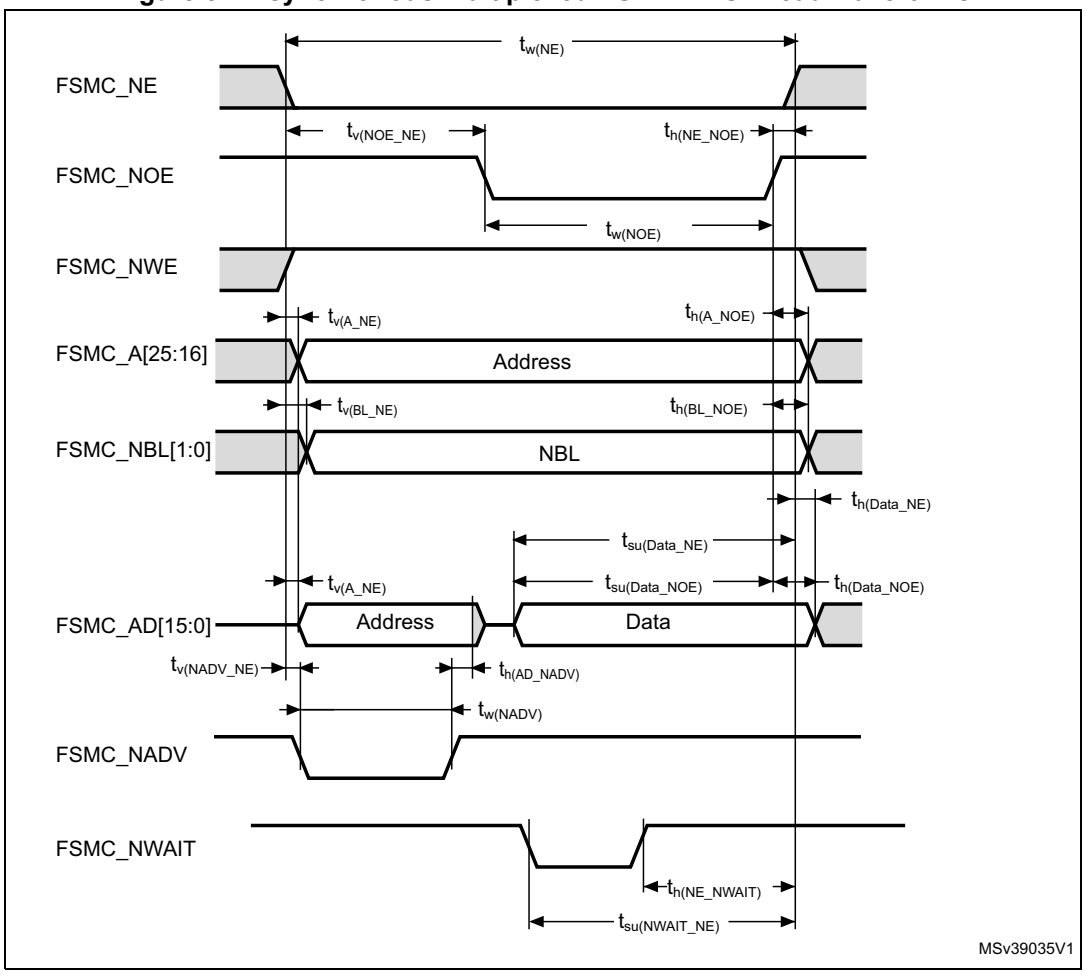
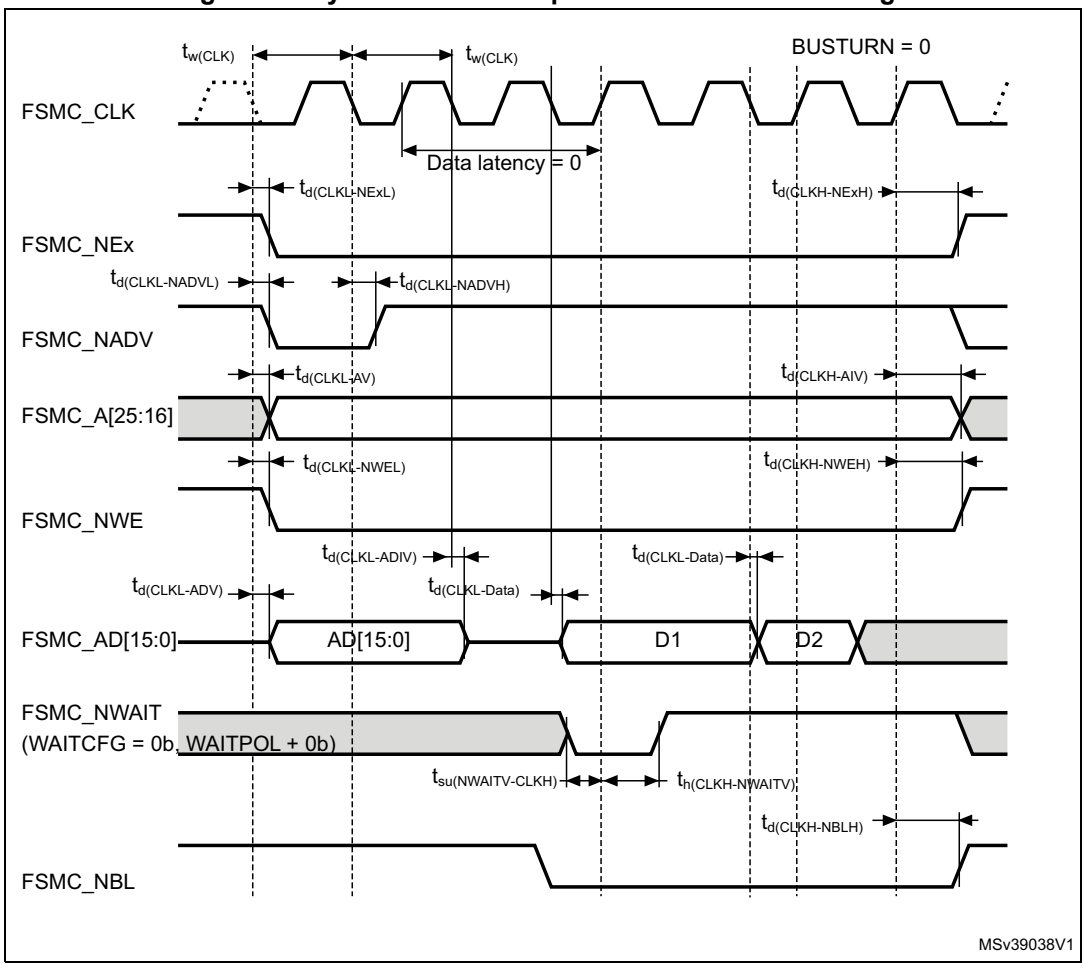


Table 91. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH\_NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	T_{HCLK}	-	
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	1	-	
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	2	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 55. Synchronous multiplexed PSRAM write timings

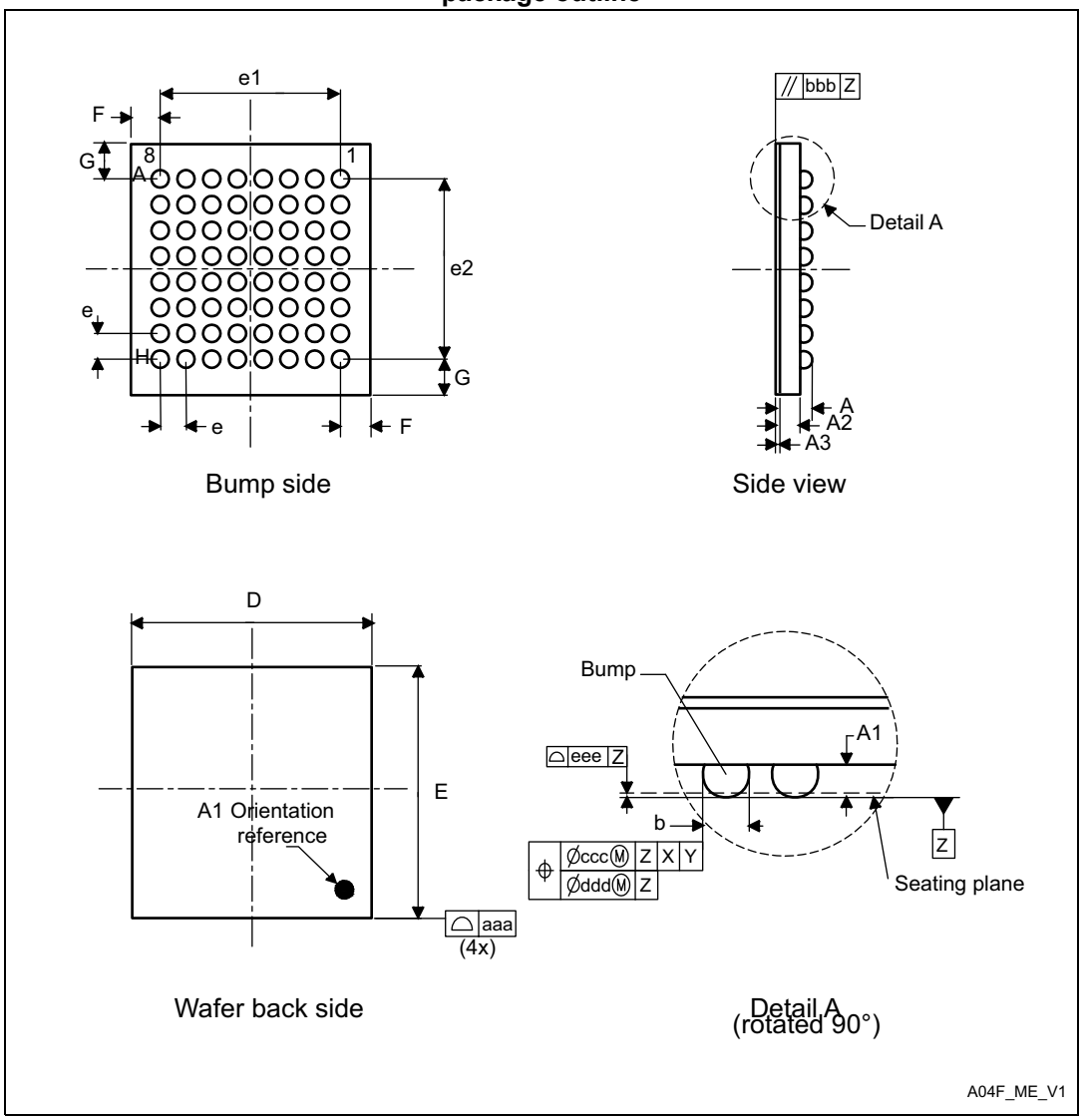


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

7.1 WLCSP64 package information

Figure 60. WLCSP64 - 64-pin, 3.658 x 3.686 mm, 0.4 mm pitch wafer level chip scale package outline



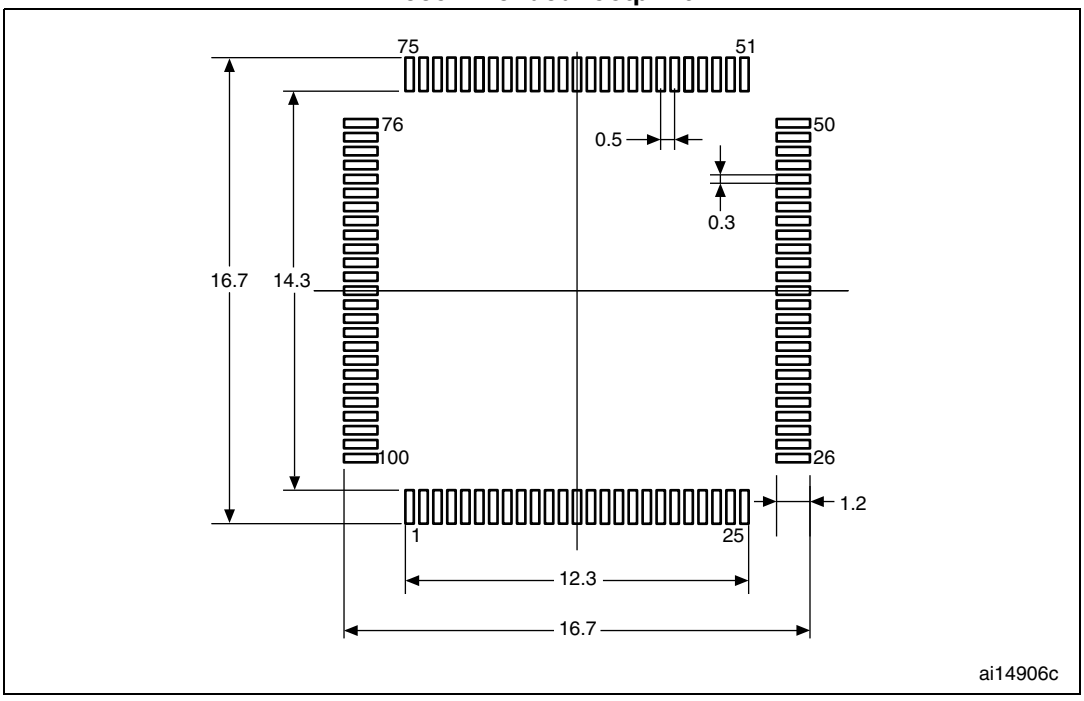
1. Drawing is not to scale.

Table 102. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 70. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

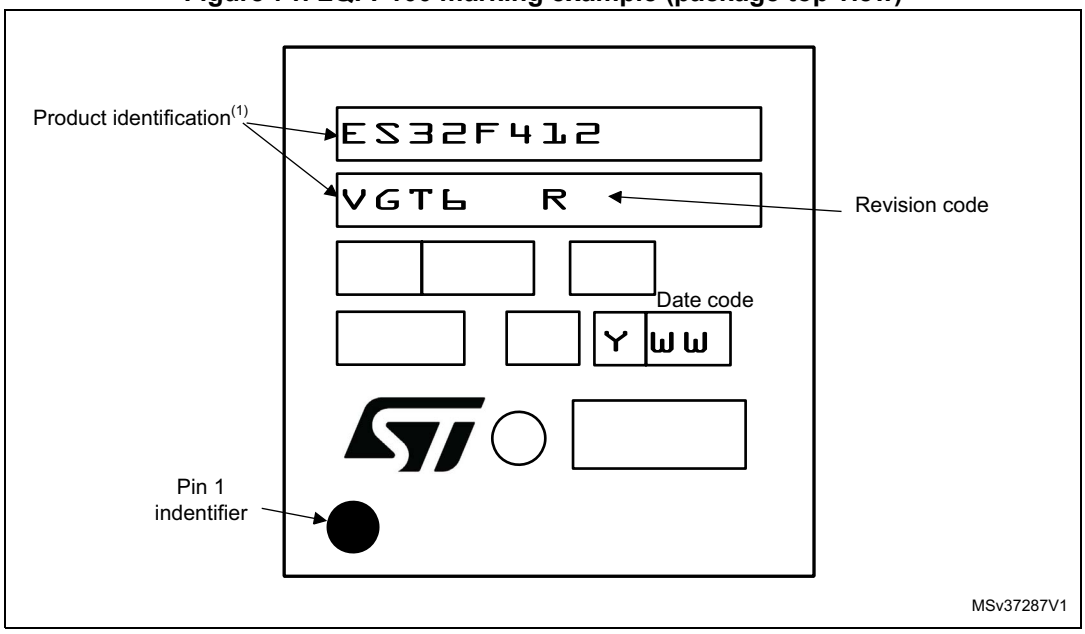


1. Dimensions are in millimeters.

Device marking for LQFP100

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 71. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.