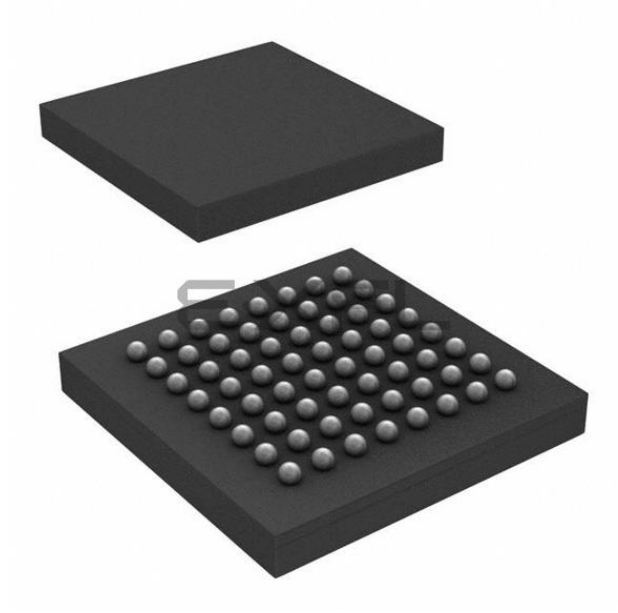

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (3.62x3.65)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412rgy6tr

3.18 Power supply supervisor

3.18.1 Internal reset ON

This feature is available for V_{DD} operating voltage range 1.8 V to 3.6 V.

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other package, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

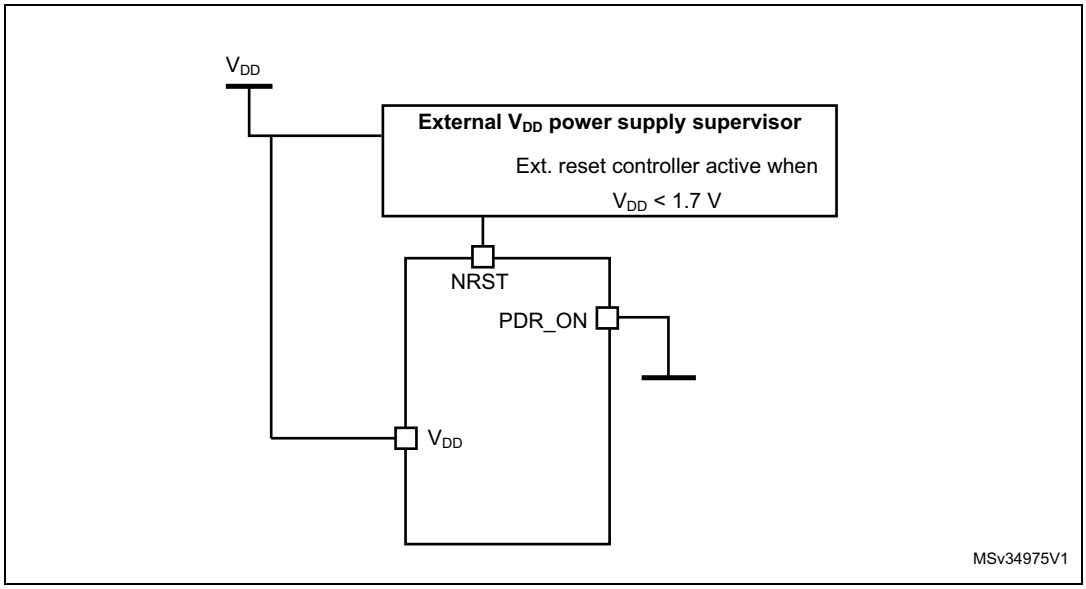
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.18.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor V_{DD} and should set the device in reset mode when V_{DD} is below 1.7 V. NRST should be connected to this external power supply supervisor. Refer to *Figure 7: Power supply supervisor interconnection with internal reset OFF*.

Figure 7. Power supply supervisor interconnection with internal reset OFF(1)



1. The PRD_ON pin is available only on WLCSP64, UFBGA100, UFBGA144 and LQFP144 packages.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

3.19 Voltage regulator

The regulator has three operating modes:

– Main regulator mode (MR)
– Low power regulator (LPR)
– Power-down

3.19.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

3.23.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.23.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.23.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.24 Inter-integrated circuit interface (I^2C)

The devices feature up to four I^2C bus interfaces which can operate in multimaster and slave modes:

- One I^2C interface supports the Standard mode (up to 100 kHz), Fast-mode (up to 400 kHz) modes and Fast-mode plus (up to 1 MHz).
- Three I^2C interfaces support the Standard mode (up to 100 KHz) and the Fast mode (up to 400 KHz). Their frequency can be increased up to 1 MHz. For more details on the complete solution, refer to the nearest STMicroelectronics sales office.

All I^2C interfaces features 7/10-bit addressing mode and 7-bit addressing mode (as slave) and embed a hardware CRC generation/verification.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 6*).

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks

3.27 Inter-integrated sound (I^2S)

Five standard I^2S interfaces (multiplexed with SPI1 to SPI5) are available. They can be operated in master or slave mode, in simplex communication mode, and full duplex mode for I2S2 and I2S3. All I^2S interfaces can be configured to operate with a 16-/32-bit resolution as an input or output channel. I2Sx audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I^2Sx interfaces can be served by the DMA controller.

3.28 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S applications. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

Different sources can be selected for the I2S master clock of the APB1 and the I2S master clock of the APB2. This gives the flexibility to work with two different audio sampling frequencies. The different possible sources are the main PLL, the PLLI2S, HSE or HSI clocks or an external clock provided through a pin (external PLL or Codec output)

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

3.29 Digital filter for sigma-delta modulators (DFSDM)

The device embeds one DFSDM with 2 digital filters modules and 4 external input serial channels (transceivers) or alternately 2 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

3.33 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.34 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

3.35 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	-	E4	15	PF5	I/O	FT	-	TIM5_CH3, FSMC_A5, EVENTOUT	-
-	-	-	10	F2	D2	16	VSS	S	-	-	-	-
-	-	-	11	G2	D3	17	VDD	S	-	-	-	-
-	-	-	-	-	F3	18	PF6	I/O	FT	-	TRACED0, TIM10_CH1, QUADSPI_BK1_IO3, EVENTOUT	-
-	-	-	-	-	F2	19	PF7	I/O	FT	-	TRACED1, TIM11_CH1, QUADSPI_BK1_IO2, EVENTOUT	-
-	-	-	-	-	G3	20	PF8	I/O	FT	-	TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	-
-	-	-	-	-	G2	21	PF9	I/O	FT	-	TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	-
-	-	-	-	-	G1	22	PF10	I/O	FT	-	TIM1_ETR, TIM5_CH4, EVENTOUT	-
5	5	D8	12	F1	D1	23	PH0 - OSC_IN	I/O	FT	(4)	EVENTOUT	OSC_IN
6	6	E8	13	G1	E1	24	PH1 - OSC_OUT	I/O	FT	(4)	EVENTOUT	OSC_OUT
7	7	D7	14	H2	F1	25	NRST	I/O	RST	-	-	NRST
-	8	D5	15	H1	H1	26	PC0	I/O	FT	-	EVENTOUT	ADC1_10, WKUP2
-	9	F8	16	J2	H2	27	PC1	I/O	FT	-	EVENTOUT	ADC1_11, WKUP3
-	10	E7	17	J3	H3	28	PC2	I/O	FT	-	SPI2_MISO, I2S2ext_SD, DFSDM1_CKOUT, FSMC_NWE, EVENTOUT	ADC1_12
-	11	D6	18	K2	H4	29	PC3	I/O	FT	-	SPI2_MOSI/I2S2_SD, FSMC_A0, EVENTOUT	ADC1_13
-	-	-	19	-	-	30	VDD	S	-	-	-	-
8	12	G8	20	-	-	31	VSSA/ VREF	S	-	-	-	-
-	-	-	-	J1	J1	-	VSSA	S	-	-	-	-

Table 10. STM32F412xE/G alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port A	PA0	-	TIM2_CH1/ TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	-	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	SPI4_MOSI/I 2S4_SD	-	USART2_RTS	-	QUADSPI_ BK1_IO3	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	I2S2_CKIN	-	USART2_TX	-	-	-	FSMC_D4	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	I2S2_MCK	-	USART2_RX	-	-	-	FSMC_D5	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS/I2 S1_WS	SPI3_NSS/ I2S3_WS	USART2_CK	DFSDM1_ DATIN1	-	-	FSMC_D6	EVENTOUT
	PA5	-	TIM2_CH1/ TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/ I2S1_CK	-	-	DFSDM1_ CKIN1	-	-	FSMC_D7	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	I2S2_MCK	-	-	TIM13_ CH1	QUADSPI_ BK2_IO0	SDIO_CMD	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I 2S1_SD	-	-	-	TIM14_ CH1	QUADSPI_ BK2_IO1	-	EVENTOUT
	PA8	MCO_1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	USB_FS_ SOF	SDIO_D1	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_ SMBA	-	-	USART1_TX	-	-	USB_FS_ VBUS	SDIO_D2	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	SPI5_MOSI/ I2S5_SD	USART1_RX	-	-	USB_FS_ID	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	SPI4_MISO	USART1_CTS	USART6_ TX	CAN1_RX	USB_FS_DM	-	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	SPI5_MISO	USART1_RTS	USART6_ RX	CAN1_TX	USB_FS_DP	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	-	-	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	USART1_TX	-	-	-	-	EVENTOUT

6.3 Operating conditions

6.3.1 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale3: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x01	0	-	64	MHz
		Power Scale2: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x10	0	-	84	
		Power Scale1: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x11	0	-	100	
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	50	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	-	100	MHz
V_{DD}	Standard operating voltage	-	1.7(1)	-	3.6	V
V_{DDA}(2)(3)	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}(4)	1.7(1)	-	2.4	V
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11 and PA12 pins)	USB not used	1.7	3.3	3.6	V
		USB used(5)	3.0	-	3.6	
V_{BAT}	Backup operating voltage	-	1.65	-	3.6	V
V_{12}	Regulator ON: 1.2 V internal voltage on VCAP_1/VCAP_2 pins	VOS[1:0] bits in PWR_CR register = 0x01 Max frequency 64 MHz	1.08(6)	1.14	1.20(6)	V
		VOS[1:0] bits in PWR_CR register = 0x10 Max frequency 84 MHz	1.20(6)	1.26	1.32(6)	
		VOS[1:0] bits in PWR_CR register = 0x11 Max frequency 100 MHz	1.26	1.32	1.38	
V_{12}	Regulator OFF: 1.2 V external voltage must be supplied on VCAP_1/VCAP_2 pins	Max frequency 64 MHz	1.10	1.14	1.20	V
		Max frequency 84 MHz	1.20	1.26	1.32	
		Max frequency 100 MHz	1.26	1.32	1.38	
V_{IN}	Input voltage on RST, FT and TC pins(7)	$2\ V \le V_{DD} \le 3.6\ V$	–0.3	-	5.5	V
		$V_{DD} \le 2\ V$	–0.3	-	5.2	
	Input voltage on BOOT0 pin	-	0	-	9	

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. Tested in production.

Table 29. Typical and maximum current consumption in Sleep mode - V_{DD} = 1.7 V

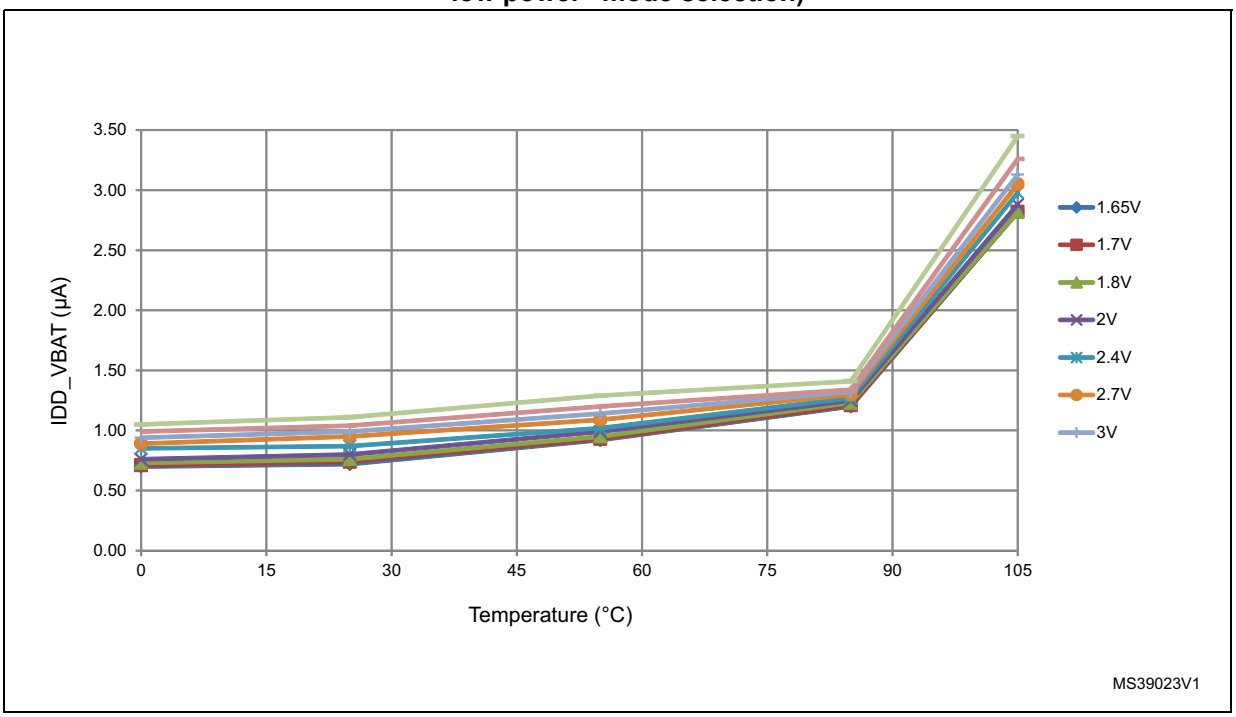
Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Sleep mode**	External clock, PLL ON, Flash deep power down, all peripherals enabled(2)	100	17.3	18.62	19.90	21.40	mA
			84	14.0	15.08	16.04	17.16	
			64	9.7	10.41	11.02	11.80	
			50	7.6	8.27	8.89	9.62	
			25	4.2	4.79	5.35	6.00	
			20	3.7	4.11	4.67	5.31	
		HSI, PLL OFF(2), Flash deep power down, all peripherals enabled	16	2.4	2.81	3.45	4.20	
			1	0.5	0.67	1.27	1.91	
		External clock, PLL ON(2) all peripherals enabled, Flash ON	100	17.8	19.08	20.35	21.90	
			84	14.4	15.49	16.42	17.59	
			64	10.0	10.76	11.43	12.18	
			50	7.9	8.58	9.19	9.94	
			25	4.4	4.99	5.54	6.21	
			20	4.0	4.42	4.95	5.64	
		HSI, PLL OFF(2), all peripherals enabled, Flash ON	16	2.7	3.09	3.75	4.49	
			1	0.8	0.93	1.52	2.18	

Table 34. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions[1]	Typ				Max[2]		Unit
			T_A = 25 °C				T_A = 85 °C	T_A = 105 °C	
			V_{BAT} = 1.7 V	V_{BAT}= 2.4 V	V_{BAT} = 3.3 V	V_{BAT} = 3.6 V	V_{BAT} = 3.6 V		
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator (LSE in low-drive mode) and RTC ON	0.74	0.87	1.04	1.11	3.0	5.0	µA
		Low-speed oscillator (LSE in high-drive mode) and RTC ON	1.52	1.70	1.97	2.09	3.8	5.8	
		RTC and LSE OFF	0.04	0.04	0.05	0.05	2.0	4.0	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization, not tested in production.

Figure 24. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "low power" mode selection)



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off,
  - with only one peripheral clocked on,
  - scale 1 with f_{HCLK} = 100 MHz,
  - scale 2 with f_{HCLK} = 84 MHz,
  - scale 3 with f_{HCLK} = 64 MHz.
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 36. Peripheral current consumption

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
AHB1	GPIOA	1.84	1.75	1.55	µA/MHz
	GPIOB	1.90	1.80	1.61	
	GPIOC	1.77	1.67	1.50	
	GPIOD	1.67	1.58	1.42	
	GPIOE	1.75	1.67	1.48	
	GPIOF	1.65	1.56	1.39	
	GPIOG	1.65	1.56	1.39	
	GPIOH	0.62	0.57	0.53	
	CRC	0.26	0.25	0.22	
	DMA1(1)	1,71N+2,98	1,62N+2,87	1,45N+2,58	
	DMA2(1)	1,78N+2,62	1,70N+2.53	1,52N+2.26	
AHB2	RNG	0.77	0.74	0.66	
	USB_OTG_FS	19.68	18.73	16.78	
AHB3	FSMC	5.36	5.11	4.56	
	QSPI	9.99	9.51	8.53	

Table 49. Flash memory programming with V_{PP} voltage

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 50. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycle(2) at T_A = 55 °C	20	

1. Guaranteed by characterization, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 64* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 64. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master full duplex/receiver mode, 2.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	MHz
		Master transmitter mode 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Master mode 1.7 V < V_{DD} < 3.6 V SPI1/2/3/4/5	-	-	25	
		Slave transmitter/full duplex mode 2.7 V < V_{DD} < 3.6 V SPI1//4/5	-	-	50	
		Slave transmitter/full duplex mode 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	35(2)	
		Slave receiver mode, 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Slave mode, 1.7 V < V_{DD} < 3.6 V SPI2/3	-	-	25	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, SPI presc = 2	T_{PCLK}-1.5	T_{PCLK}	T_{PCLK} +1.5	ns
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$3T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2T_{PCLK}$	-	-	ns
$t_{su(MI)}$	Data input setup time	Master mode	4.5	-	-	ns
$t_{su(SI)}$		Slave mode	1.5	-	-	ns
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	ns
$t_{h(SI)}$		Slave mode	0.5	-	-	ns

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Table 86. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$8T_{HCLK}$ - 1	$8T_{HCLK}$ + 0.5	ns
$t_{w(NWE)}$	FSMC_NWE low time	$6T_{HCLK}$ + 0.5	$6T_{HCLK}$ + 1	
$t_{su(NWAIT\_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$6T_{HCLK}$ + 0.5	-	
$t_{h(NE\_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4T_{HCLK}$ + 1	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 52. Asynchronous multiplexed PSRAM/NOR read waveforms

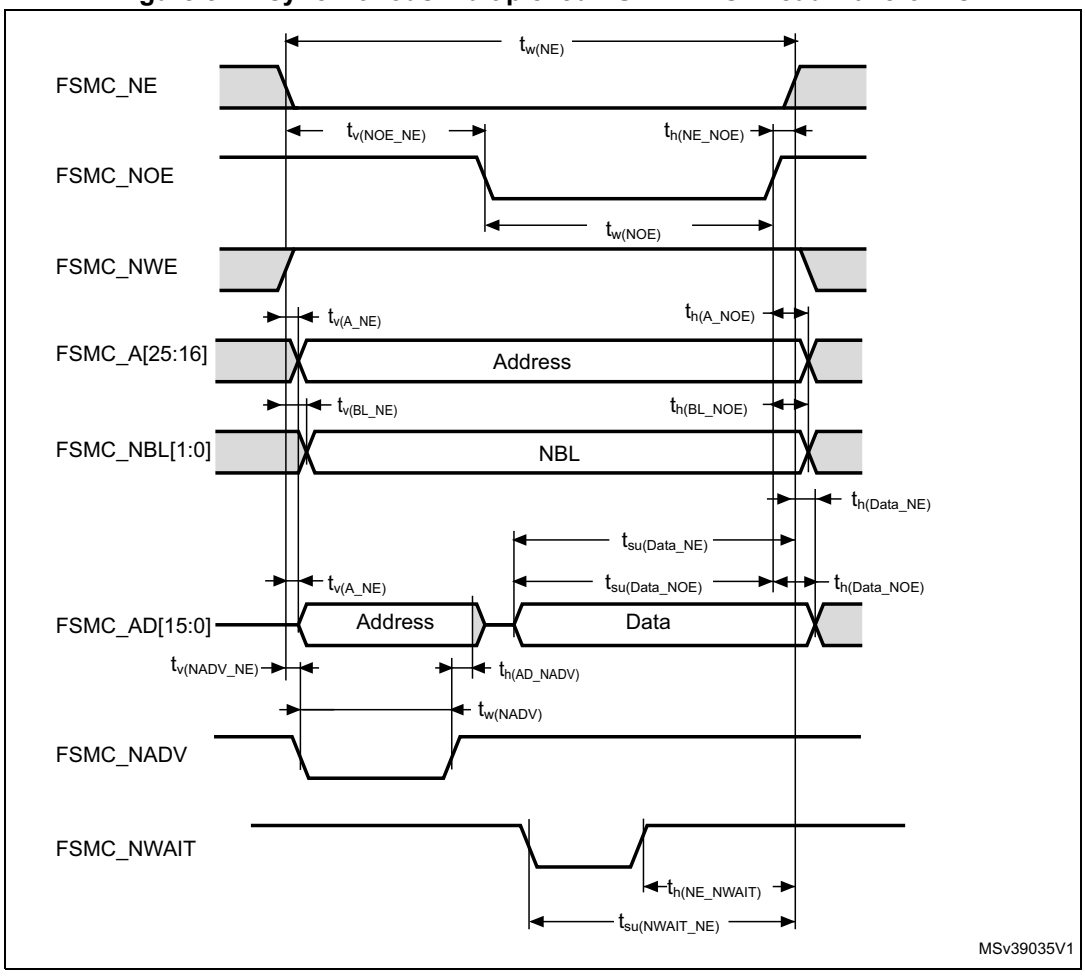
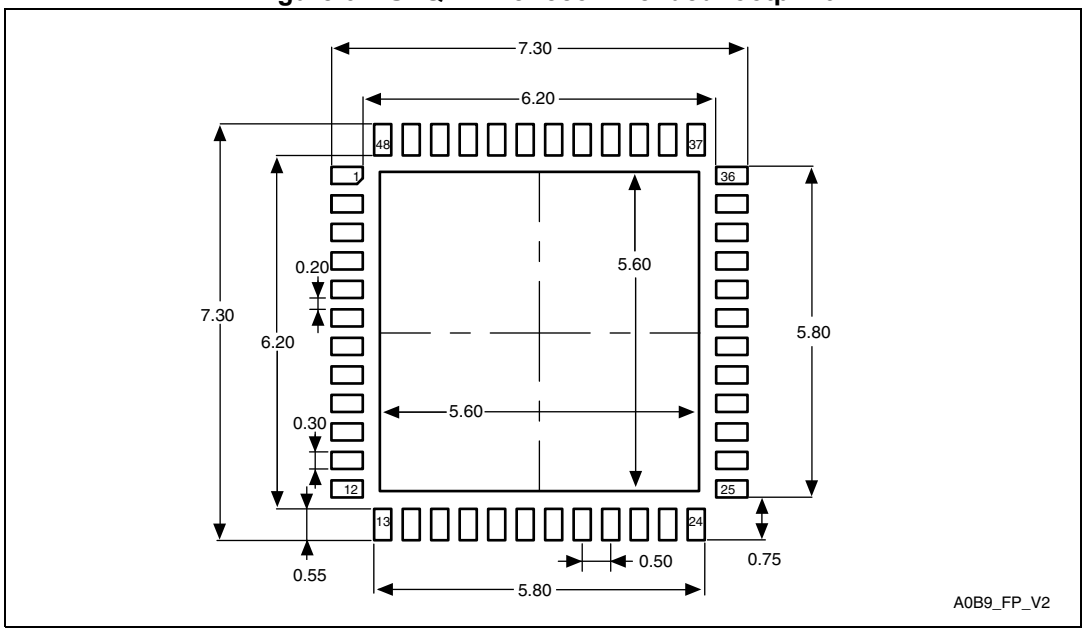


Table 100. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

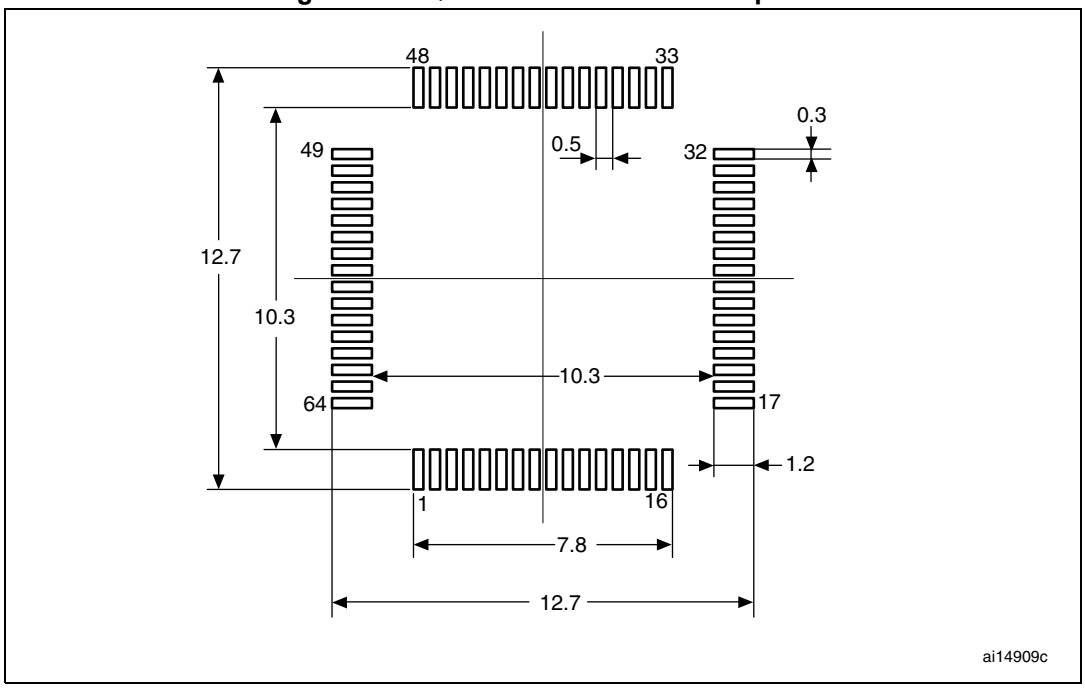
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 64. UFQFPN48 recommended footprint



1. Dimensions are in millimeters.

Figure 67. LQFP64 recommended footprint

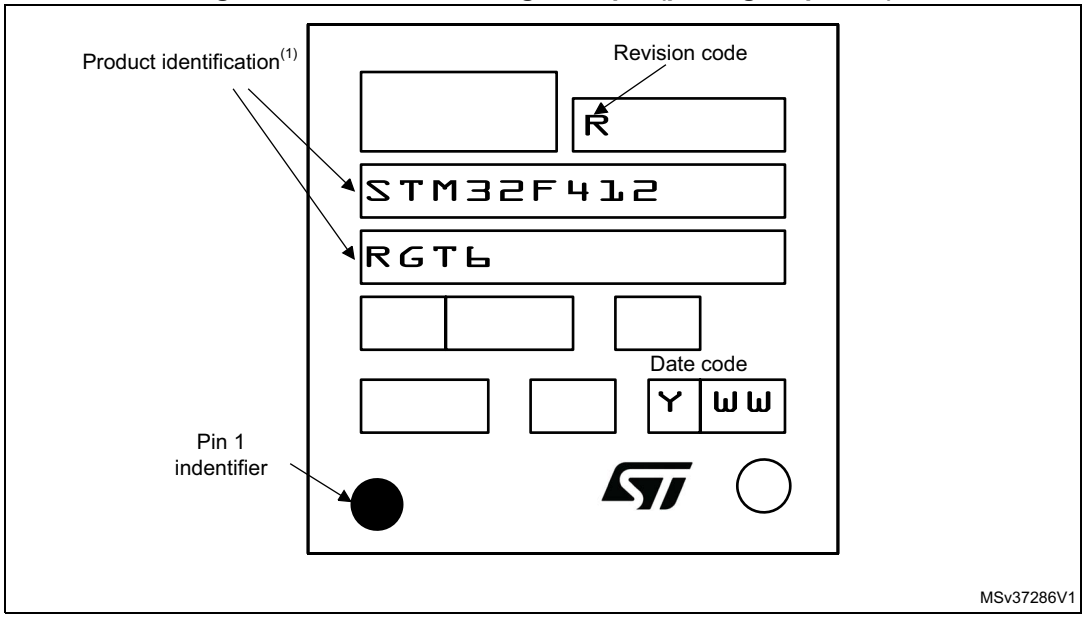


1. Dimensions are in millimeters.

Device marking for LQFP64

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 68. LQFP64 marking example (package top view)

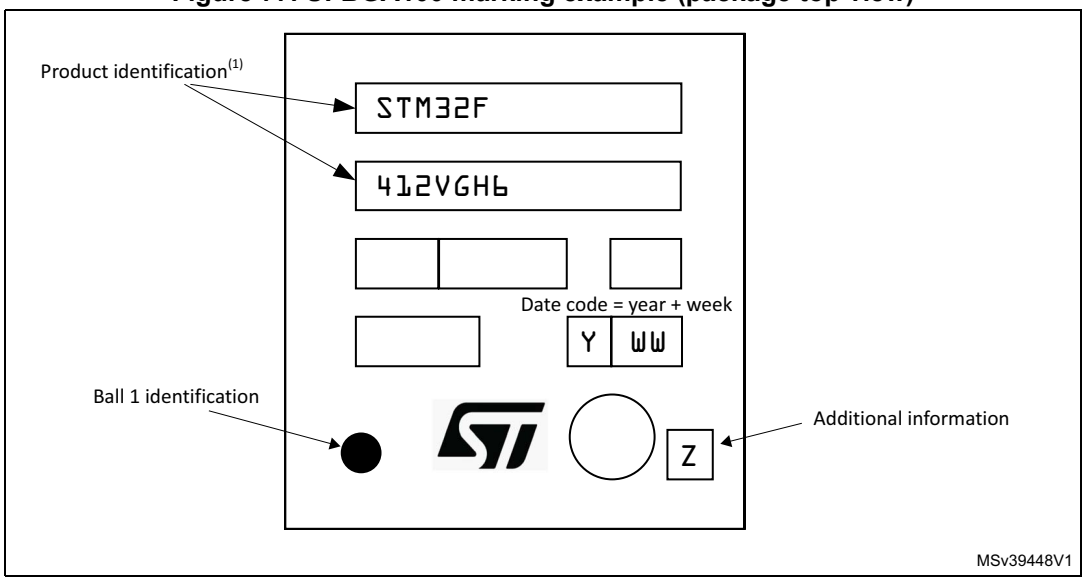


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking for UFBGA100

The following figure gives an example of topside marking and ball 1 position identifier location.

Figure 77. UFBGA100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Revision history

Table 110. Document revision history

Date	Revision	Changes
10-Nov-2015	1	Initial release.
01-Feb-2016	2	Added – *Table 3: Embedded bootloader interfaces* – *Figure 3: Compatible board design for LQFP144 package* – *Figure 62: WLCSP64 marking example (package top view)* – *Figure 77: UFBGA100 marking example (package top view)* Updated – *Section 3.17: Power supply schemes* – *Section 3.23: Timers and watchdogs* – *Section 3.32: Universal serial bus on-the-go full-speed (USB_OTG_FS)* – *Figure 1: Compatible board design for LQFP100 package* – *Figure 2: Compatible board design for LQFP64 package* – *Figure 14: STM32F412xE/G LQFP100 pinout* – *Figure 16: STM32F412xE/G UFBGA100 pinout* – *Figure 17: STM32F412xE/G UFBGA144 pinout* – *Figure 20: Input voltage measurement* – *Figure 80: UFBGA144 marking example (package top view)* – *Table 2: STM32F412xE/G features and peripheral counts* – *Table 9: STM32F412xE/G pin definition* – *Table 12: Voltage characteristics* – *Table 13: Current characteristics* – *Table 15: General operating conditions* – *Table 36: Peripheral current consumption* – *Table 51: EMS characteristics for LQFP144 package* – *Table 63: FMPI2C characteristics*