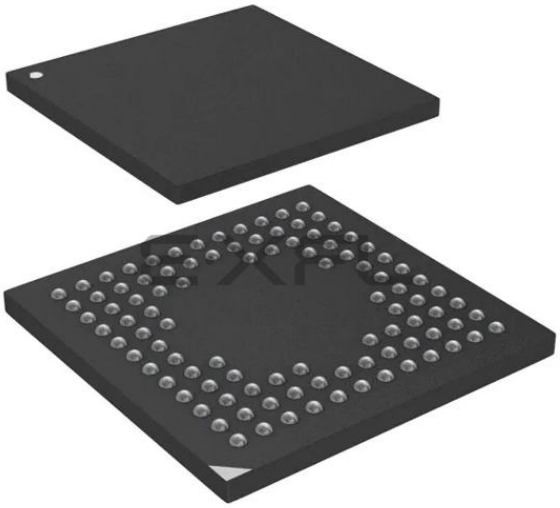

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 81 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-UFBGA |
| Supplier Device Package | 100-UFBGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412veh3tr |

**Figure 2. Compatible board design for LQFP64 package**

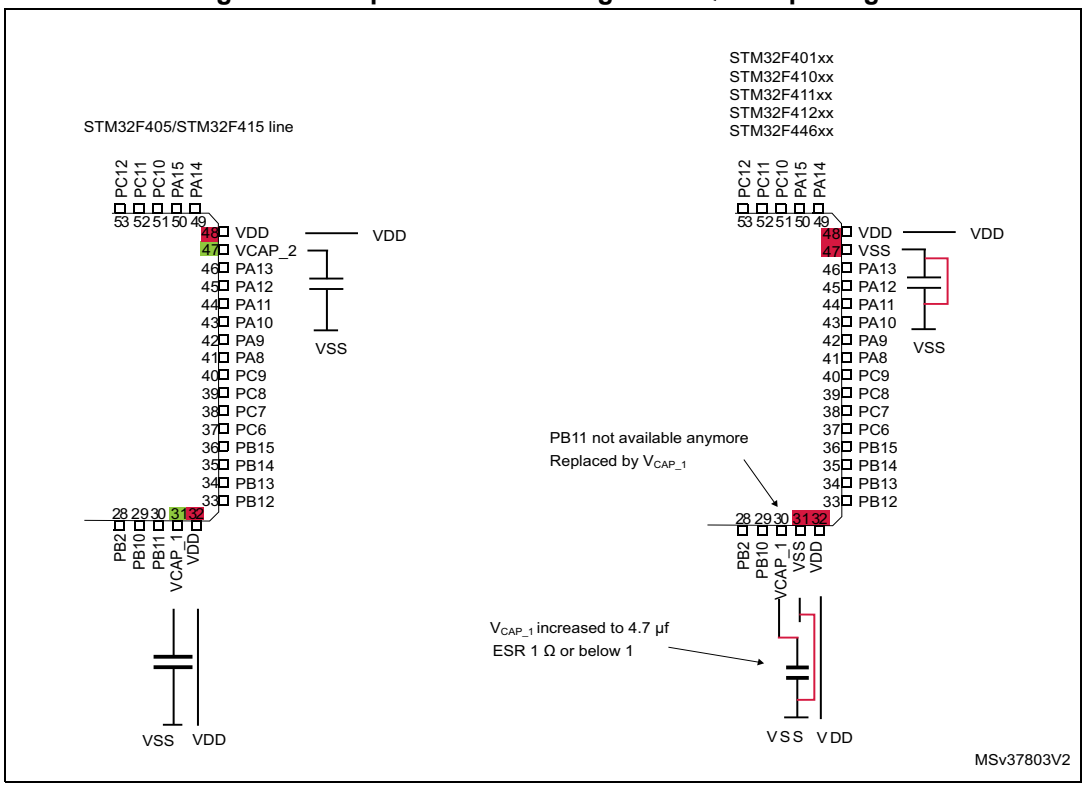
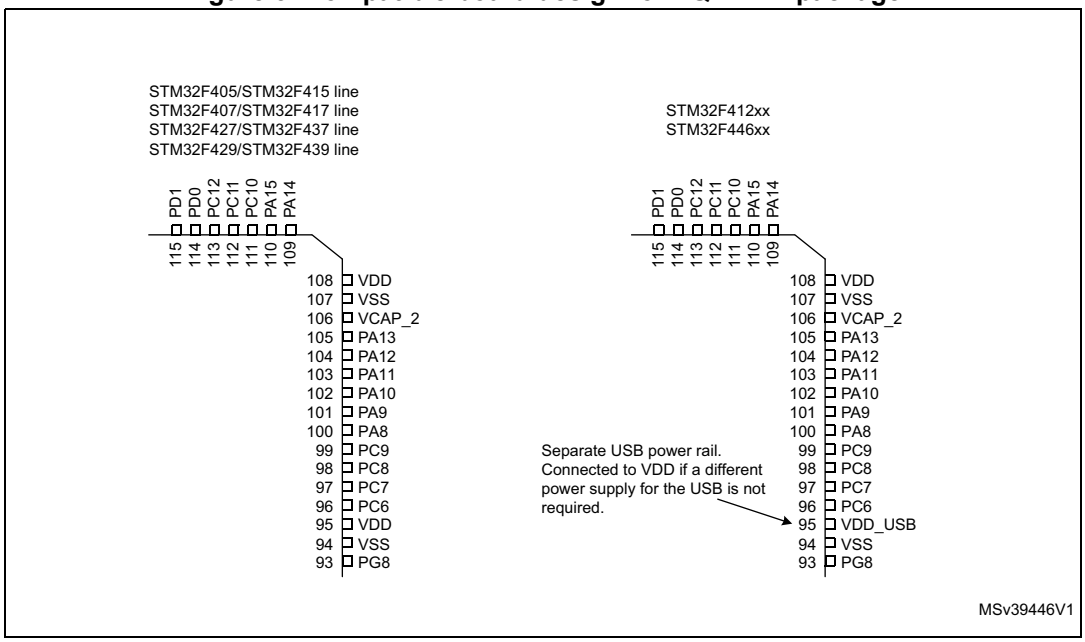



**Figure 3. Compatible board design for LQFP144 package**



## 3.13 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 81 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

## 3.14 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 21 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

## 3.15 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 100 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses and high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

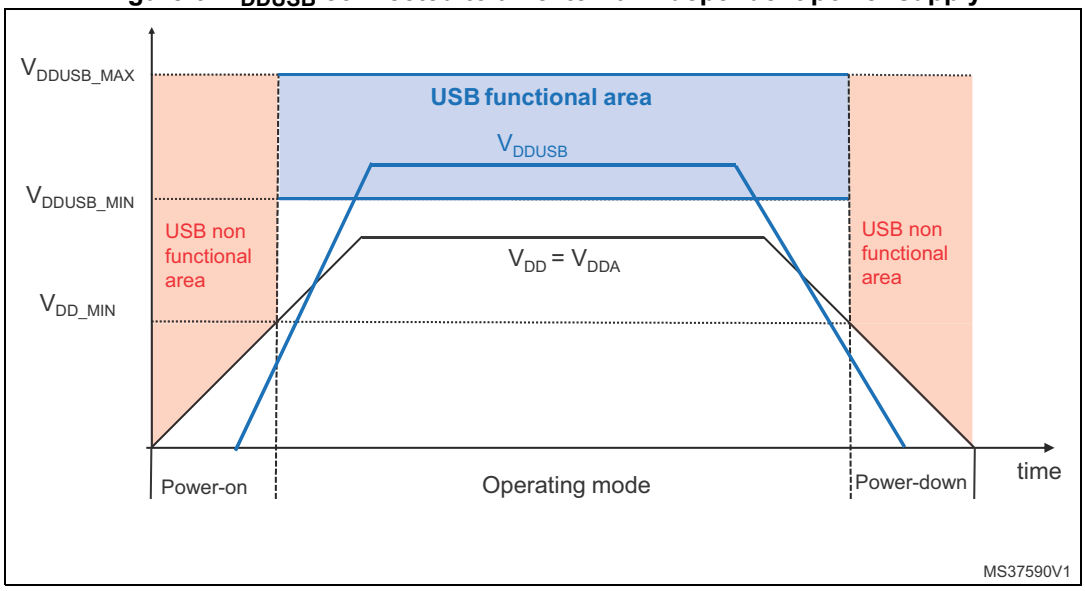
The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the $I^2S$ master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

it is independent from $V_{DD}$ or $V_{DDA}$ but it must be the last supply to be provided and the first to disappear.

The following conditions VDDUSB must be respected:

- During power-on phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDUSB}$ should be always lower than $V_{DD}$
- During power-down phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDUSB}$ should be always lower than $V_{DD}$
- $V_{DDUSB}$ rising and falling time rate specifications must be respected.
- In operating mode phase, $V_{DDUSB}$ could be lower or higher than VDD:
  - If USB is used, the associated GPIOs powered by $V_{DDUSB}$ are operating between $V_{DDUSB\_MIN}$ and $V_{DDUSB\_MAX}$.
  - If USB is not used, the associated GPIOs powered by $V_{DDUSB}$ are operating between $V_{DD\_MIN}$ and $V_{DD\_MAX}$.

**Figure 6. $V_{DDUSB}$ connected to an external independent power supply**



## 3.23 Timers and watchdogs

The devices embed two advanced-control timer, ten general-purpose timers, two basic timers, two watchdog timers and one SysTick timer.

All timer counters can be frozen in debug mode.

*Table 5* compares the features of the advanced-control and general-purpose timers.

## 3.33 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

## 3.34 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

## 3.35 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

## 3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

## 3.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

**Table 15. General operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $P_D$ | Power dissipation at TA = 85°C for range 6 or TA = 105°C for range 7(8) | UFQFPN48 | - | - | 625 | mW |
| | | WLCSP64 | - | - | 392 | |
| | | LQFP64 | - | - | 425 | |
| | | LQFP100 | - | - | 465 | |
| | | LQFP144 | | | 571 | |
| | | UFBGA100 | - | - | 351 | |
| | | UFBGA144 | - | - | 416 | |
| $T_A$ | Ambient temperature for range 6 | Maximum power dissipation | –40 | - | 85 | °C |
| | | Low power dissipation(9) | –40 | - | 105 | |
| | Ambient temperature for range 7 | Maximum power dissipation | –40 | - | 105 | |
| | | Low power dissipation(9) | –40 | - | 125 | |
| $T_J$ | Junction temperature range | Range 6 | –40 | - | 105 | |
| | | Range 7 | –40 | - | 125 | |

1. $V_{DD}/V_{DDA}$ minimum value of 1.7 V with the use of an external power supply supervisor (refer to *Section 3.18.2: Internal reset OFF*).
2. When the ADC is used, refer to *Table 71: ADC characteristics*.
3. If $V_{REF+}$ pin is present, it must respect the following condition: $V_{DDA}$-$V_{REF}$+ < 1.2 V.
4. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and power-down operation.
5. Only the DM ($P_{A11}$) and DP ($P_{A12}$) pads are supplied through $V_{DDUSB}$. For application where the $V_{BUS}$ ($P_{A9}$) is directly connected to the chip, a minimum $V_{DD}$ supply of 2.7V is required.

   (some application examples are shown in appendix B)
6. Guaranteed by test in production
7. To sustain a voltage higher than $V_{DD}$+0.3, the internal Pull-up and Pull-Down resistors must be disabled
8. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$.
9. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_{Jmax}$.

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both $f_{HCLK}$ frequency and VDD ranges (refer to *Table 16: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to $f_{HCLK}$ frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 64$ MHz
  - Scale 2 for 64 MHz < $f_{HCLK} \leq 84$ MHz
  - Scale 1 for 84 MHz < $f_{HCLK} \leq 100$ MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for $V_{DD}$ = 3.6 V and a maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

**Table 21. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD}$ = 1.7 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$= 25 °C | $T_A$= 25 °C | $T_A$=85 °C | $T_A$=105 °C | |
| $I_{DD}$ | Supply current in **Run mode** | External clock, PLL ON, all peripherals enabled(2)(3) | 100 | 28.1 | 30.24 | 31.27 | 32.21 | mA |
| | | | 84 | 22.7 | 24.05 | 24.54 | 25.11 | |
| | | | 64 | 15.7 | 16.99 | 17.47 | 18.03 | |
| | | | 50 | 12.3 | 13.36 | 13.82 | 14.36 | |
| | | | 25 | 6.5 | 7.44 | 7.82 | 8.30 | |
| | | | 20 | 5.6 | 6.16 | 6.66 | 7.20 | |
| | | HSI, PLL off, all peripherals enabled(2)(3) | 16 | 3.9 | 4.70 | 5.31 | 6.08 | |
| | | | 1 | 0.6 | 0.78 | 1.33 | 1.98 | |
| | | External clock, PLL ON, all peripherals disabled(3) | 100 | 14.0 | 15.48 | 16.08 | 16.83 | |
| | | | 84 | 11.3 | 12.23 | 12.75 | 13.41 | |
| | | | 64 | 7.9 | 8.84 | 9.31 | 10.01 | |
| | | | 50 | 6.2 | 7.06 | 7.53 | 8.19 | |
| | | | 25 | 3.4 | 4.18 | 4.61 | 5.13 | |
| | | | 20 | 2.9 | 3.44 | 3.98 | 4.65 | |
| | | HSI, PLL off, all peripherals disabled(3) | 16 | 2.0 | 2.51 | 3.13 | 3.89 | |
| | | | 1 | 0.5 | 0.64 | 1.21 | 1.90 | |

1. Based on characterization, not tested in production unless otherwise specified
2. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. Tested in production.

**Table 29. Typical and maximum current consumption in Sleep mode - $V_{DD}$ = 1.7 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in **Sleep mode** | External clock, PLL ON, Flash deep power down, all peripherals enabled(2) | 100 | 17.3 | 18.62 | 19.90 | 21.40 | mA |
| | | | 84 | 14.0 | 15.08 | 16.04 | 17.16 | |
| | | | 64 | 9.7 | 10.41 | 11.02 | 11.80 | |
| | | | 50 | 7.6 | 8.27 | 8.89 | 9.62 | |
| | | | 25 | 4.2 | 4.79 | 5.35 | 6.00 | |
| | | | 20 | 3.7 | 4.11 | 4.67 | 5.31 | |
| | | HSI, PLL OFF(2), Flash deep power down, all peripherals enabled | 16 | 2.4 | 2.81 | 3.45 | 4.20 | |
| | | | 1 | 0.5 | 0.67 | 1.27 | 1.91 | |
| | | External clock, PLL ON(2) all peripherals enabled, Flash ON | 100 | 17.8 | 19.08 | 20.35 | 21.90 | |
| | | | 84 | 14.4 | 15.49 | 16.42 | 17.59 | |
| | | | 64 | 10.0 | 10.76 | 11.43 | 12.18 | |
| | | | 50 | 7.9 | 8.58 | 9.19 | 9.94 | |
| | | | 25 | 4.4 | 4.99 | 5.54 | 6.21 | |
| | | | 20 | 4.0 | 4.42 | 4.95 | 5.64 | |
| | | HSI, PLL OFF(2), all peripherals enabled, Flash ON | 16 | 2.7 | 3.09 | 3.75 | 4.49 | |
| | | | 1 | 0.8 | 0.93 | 1.52 | 2.18 | |

**Table 36. Peripheral current consumption (continued)**

| Peripheral | | $I_{DD}$ (Typ) | | | Unit |
|---|---|---|---|---|---|
| | | Scale 1 | Scale 2 | Scale 3 | |
| APB2 | AHB-APB2 bridge | 0.09 | 0.07 | 0.08 | µA/MHz |
| | TIM1 | 6.83 | 6.46 | 5.81 | |
| | TIM8 | 6.63 | 6.29 | 5.63 | |
| | USART1 | 3.31 | 3.11 | 2.80 | |
| | USART6 | 3.21 | 3.02 | 2.73 | |
| | ADC1 | 3.51 | 3.31 | 2.98 | |
| | SDIO | 3.74 | 3.51 | 3.17 | |
| | SPI1 | 1.47 | 1.36 | 1.23 | |
| | SPI4 | 1.56 | 1.45 | 1.31 | |
| | SYSCFG | 0.54 | 0.49 | 0.45 | |
| | TIM9 | 3.09 | 2.92 | 2.63 | |
| | TIM10 | 1.91 | 1.79 | 1.61 | |
| | TIM11 | 1.93 | 1.81 | 1.64 | |
| | SPI5 | 1.54 | 1.44 | 1.30 | |
| | DFSDM1 | 4.25 | 4.02 | 3.61 | |
| Bus Matrix | | 3.23 | 3.06 | 2.73 | |

1. N is the number of stream enable (1...8).

### 6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 37* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0/PC0/PC1) pins are used to wakeup from Standby, Stop and Sleep modes.

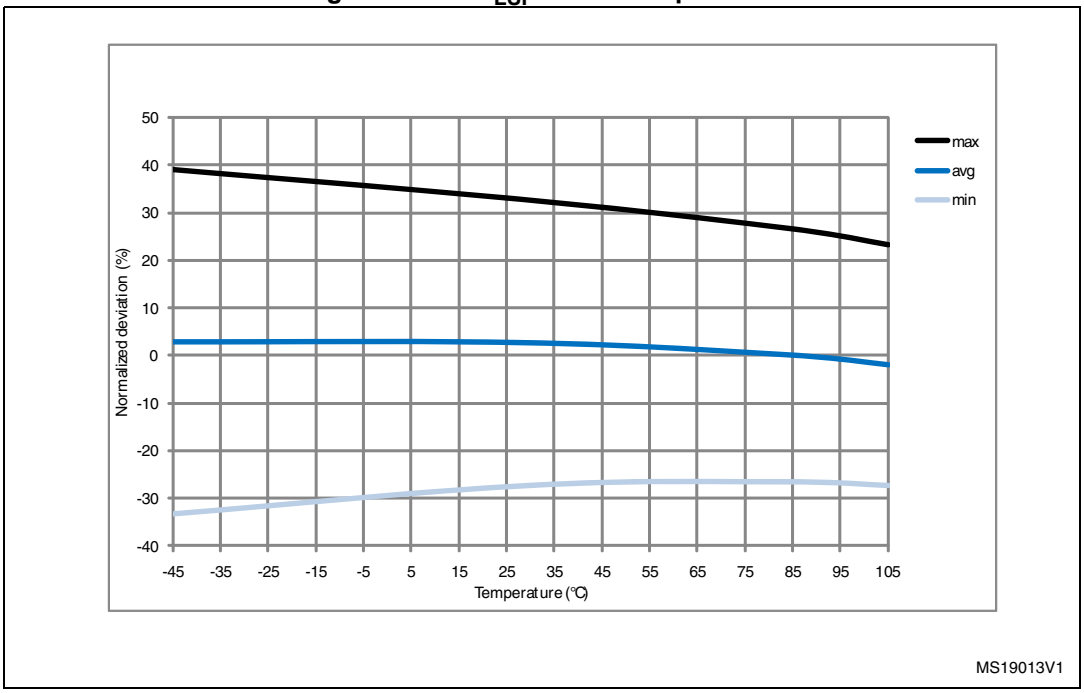
## Low-speed internal (LSI) RC oscillator

**Table 43. LSI oscillator characteristics (1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$ (2) | Frequency | 17 | 32 | 47 | kHz |
| $t_{su(LSI)}$ (3) | LSI oscillator startup time | - | 15 | 40 | µs |
| $I_{DD(LSI)}$ (3) | LSI oscillator power consumption | - | 0.4 | 0.6 | µA |

1. $V_{DD}$ = 3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design, not tested in production.

**Figure 32. $ACC_{LSI}$ versus temperature**



### QSPI interface characteristics

Unless otherwise specified, the parameters given in the following tables for QSPI are derived from tests performed under the ambient temperature, $f_{AHB}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C=20pF
- Measurement points are done at CMOS levels: 0.5VDD

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics.

**Table 66. QSPI dynamic characteristics in SDR mode(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | QSPI clock frequency | Write mode<br>1.71 V≤$V_{DD}$≤3.6 V<br>$C_{load}$ = 15 pF | - | - | 80 | MHz |
| | | Read mode<br>2.7 V<$V_{DD}$<3.6 V<br>$C_{load}$ = 15 pF | - | - | 100 | |
| | | 1.71 V≤$V_{DD}$≤3.6 V | - | - | 50 | |
| $t_{w(CKH)}$ | QSPI clock high and low | - | ($T_{(CK)}$ / 2)-1 | - | $T_{(CK)}$ / 2 | ns |
| $t_{w(CKL)}$ | | | $T_{(CK)}$ / 2) | - | ($T_{(CK)}$ / 2)+1 | |
| $t_{s(IN)}$ | Data input setup time | - | 0.5 | - | - | |
| $t_{h(IN)}$ | Data input hold time | - | 3.5 | - | - | |
| $t_{v(OUT)}$ | Data output valid time | - | - | 1 | 1.5 | |
| $t_{h(OUT)}$ | Data output hold time | - | 0.5 | - | - | |

1. Guaranteed by characterization results, not tested in production.

**Table 67. QSPI dynamic characteristics in DDR mode(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | QSPI clock frequency | Write mode<br>1.71 V≤$V_{DD}$≤3.6 V<br>$C_{load}$ = 15 pF | - | - | 80 | MHz |
| | | Read mode<br>2.7 V<$V_{DD}$<3.6 V<br>$C_{load}$ = 15 pF | - | - | 80 | |
| | | 1.71 V≤$V_{DD}$≤3.6 V | - | - | 50 | |

**Table 71. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_S$(2) | Sampling rate ($f_{ADC}$ = 30 MHz, and $t_S$ = 3 ADC cycles) | 12-bit resolution Single ADC | - | - | 2 | Msps |
| | | 12-bit resolution Interleave Dual ADC mode | - | - | 3.75 | Msps |
| | | 12-bit resolution Interleave Triple ADC mode | - | - | 6 | Msps |
| $I_{VREF+}$(2) | ADC $V_{REF}$ DC current consumption in conversion mode | - | - | 300 | 500 | µA |
| $I_{VDDA}$(2) | ADC $V_{DDA}$ DC current consumption in conversion mode | - | - | 1.6 | 1.8 | mA |

1. $V_{DDA}$ minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.18.2: Internal reset OFF*).
2. Guaranteed by characterization, not tested in production.
3. $V_{REF+}$ is internally connected to $V_{DDA}$ and $V_{REF-}$ is internally connected to $V_{SSA}$.
4. $R_{ADC}$ maximum value is given for $V_{DD}$=1.7 V, and minimum value for $V_{DD}$=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 71*.

**Equation 1: $R_{AIN}$ max formula**

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

**Table 72. ADC accuracy at $f_{ADC}$ = 18 MHz(1)**

| Symbol | Parameter | Test conditions | Typ | Max(2) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ =18 MHz<br>$V_{DDA}$ = 1.7 to 3.6 V<br>$V_{REF}$ = 1.7 to 3.6 V<br>$V_{DDA} - V_{REF}$ < 1.2 V | ±3 | ±4 | LSB |
| EO | Offset error | | ±2 | ±3 | |
| EG | Gain error | | ±1 | ±3 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±2 | ±3 | |

1. Better performance could be achieved in restricted $V_{DD}$, frequency and temperature ranges.
2. Guaranteed by characterization, not tested in production.

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics.

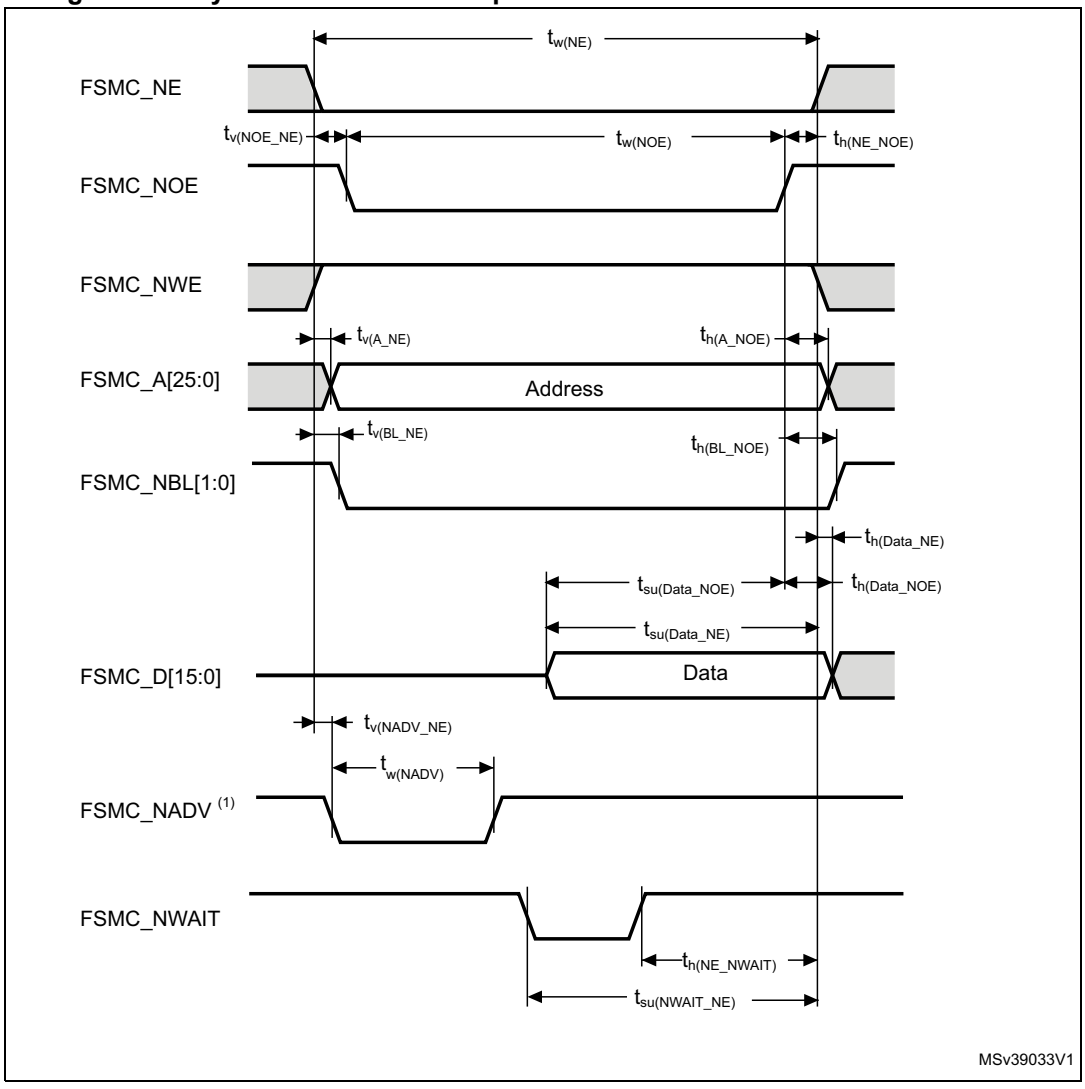
### Asynchronous waveforms and timings

*Figure 50* through *Figure 53* represent asynchronous waveforms and *Table 83* through *Table 90* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

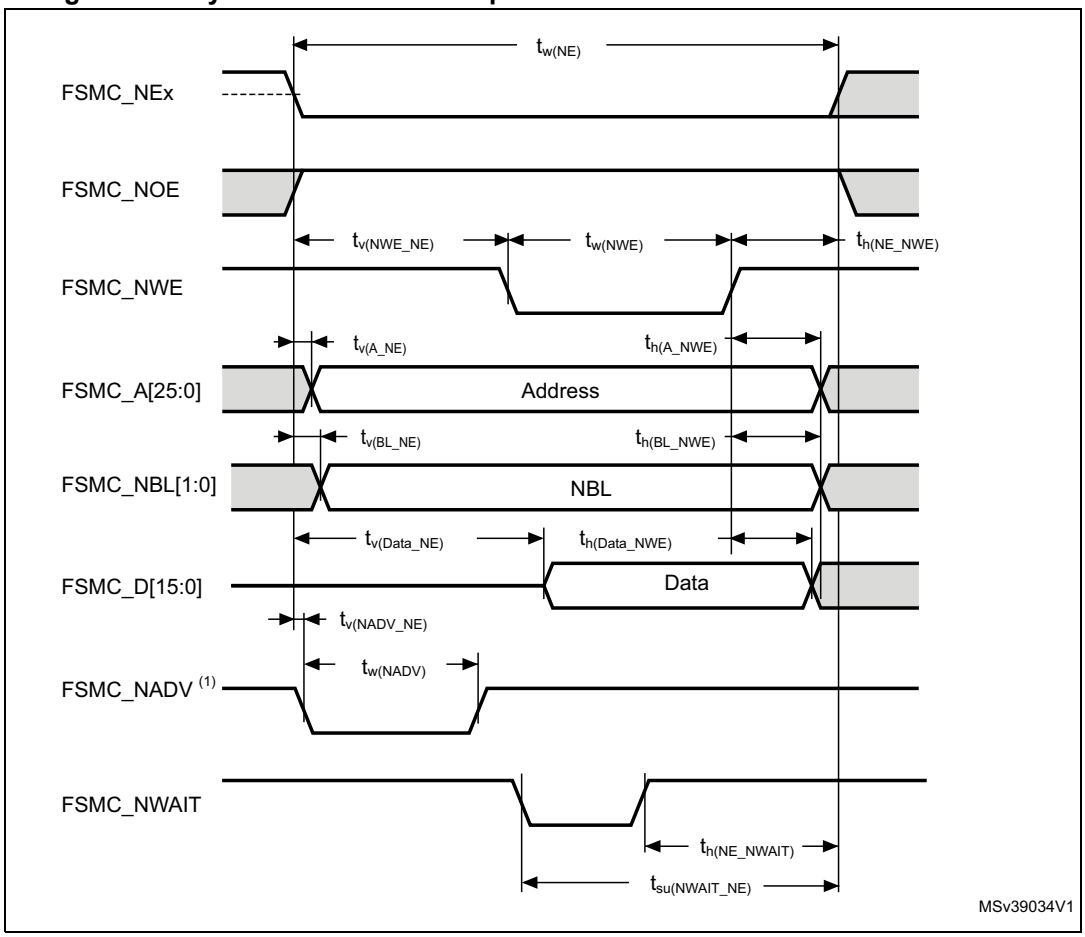
In all timing tables, the $T_{HCLK}$ is the HCLK clock period.

**Figure 50. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms**




1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

**Figure 51. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms**



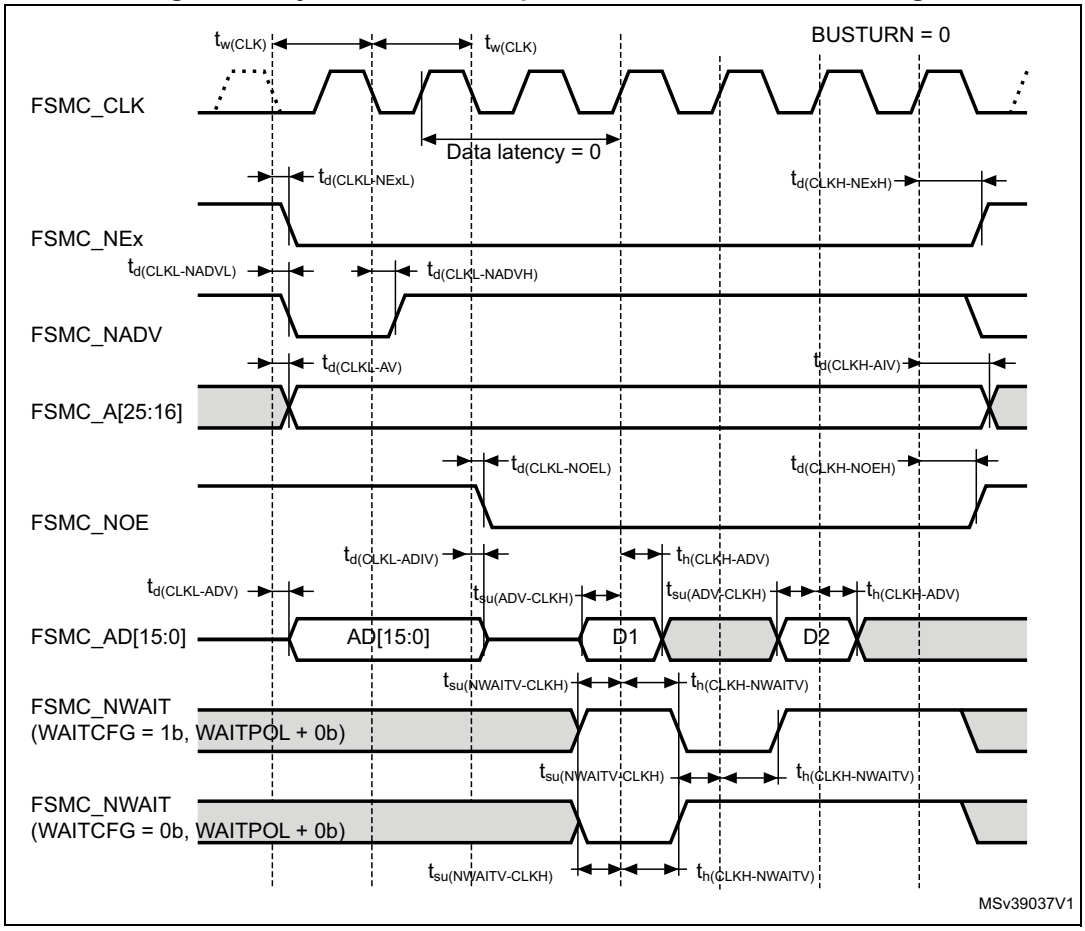

1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

**Table 85. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | 3 $T_{HCLK}$ - 1 | 3 $T_{HCLK}$ +0.5 | ns |
| $t_{v(NWE\_NE)}$ | FSMC_NEx low to FSMC_NWE low | $T_{HCLK}$ + 0.5 | $T_{HCLK}$ + 0.5 | |
| $t_{w(NWE)}$ | FSMC_NWE low time | $T_{HCLK}$ – 1.5 | $T_{HCLK}$+ 1 | |
| $t_{h(NE\_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | $T_{HCLK}$ - 1 | - | |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0.5 | |
| $t_{h(A\_NWE)}$ | Address hold time after FSMC_NWE high | $T_{HCLK}$ - 0.5 | - | |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 1 | |
| $t_{h(BL\_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | $T_{HCLK}$ - 1 | - | |
| $t_{v(Data\_NE)}$ | Data to FSMC_NEx low to Data valid | - | $T_{HCLK}$ + 2 | |
| $t_{h(Data\_NWE)}$ | Data hold time after FSMC_NWE high | $T_{HCLK}$ + 0.5 | - | |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | - | 1 | |
| $t_{w(NADV)}$ | FSMC_NADV low time | - | $T_{HCLK}$+ 0.5 | |

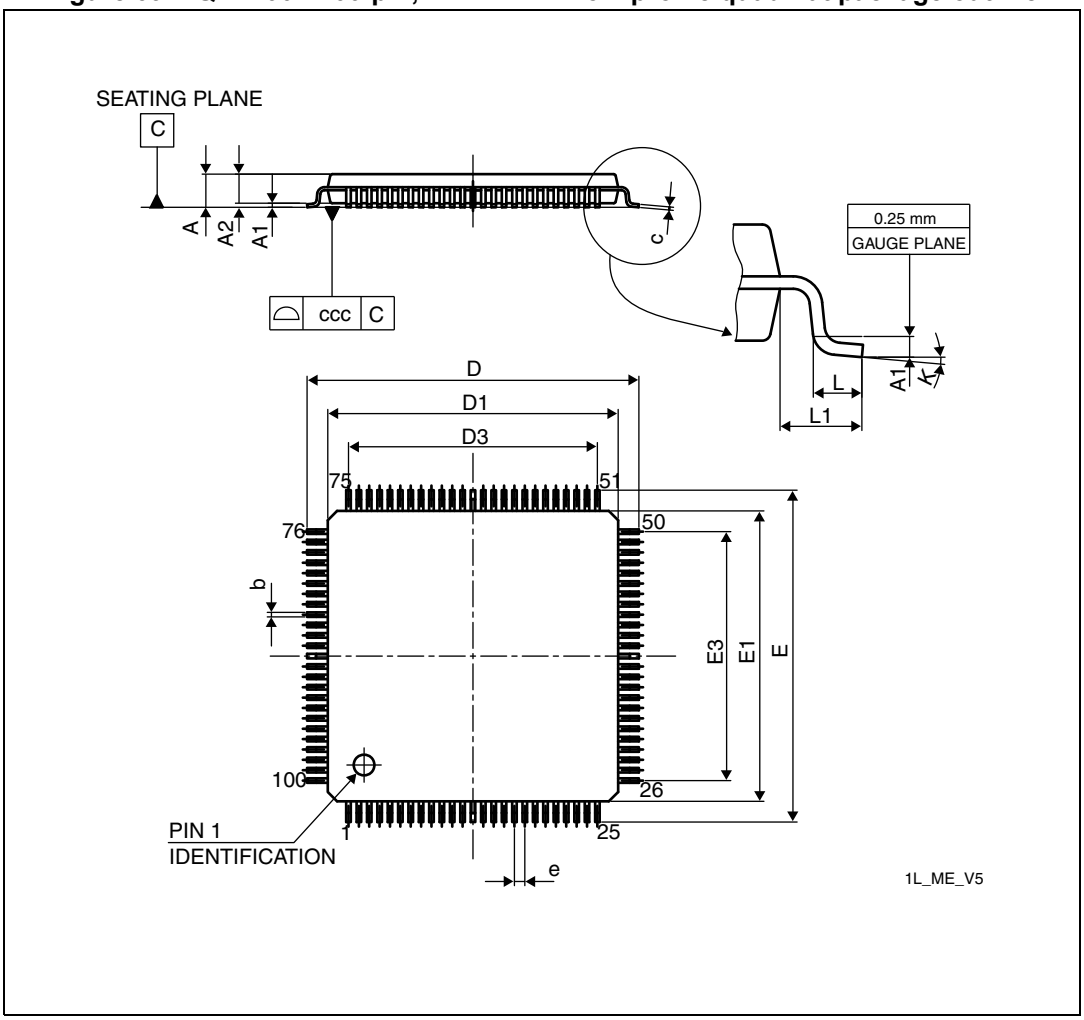
In all timing tables, the $T_{HCLK}$ is the HCLK clock period (with maximum FSMC_CLK = 90 MHz).

**Figure 54. Synchronous multiplexed NOR/PSRAM read timings**



## 7.4 LQFP100 package information

**Figure 69. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline**




1. Drawing is not to scale. Dimensions are in millimeters.

**Table 102. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |

**Table 103. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| D1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| D3 | - | 17.500 | - | - | 0.6890 | - |
| E | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| E1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| E3 | - | 17.500 | - | - | 0.6890 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Table 104. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| ddd | - | - | 0.100 | - | - | 0.0039 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 76. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint**

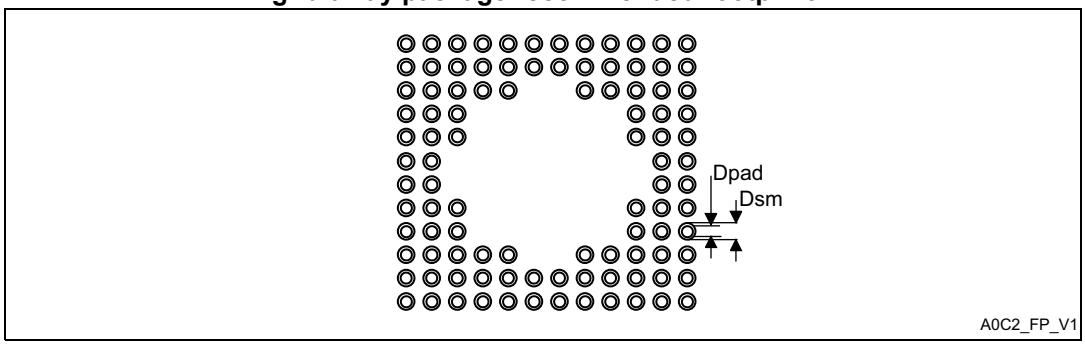
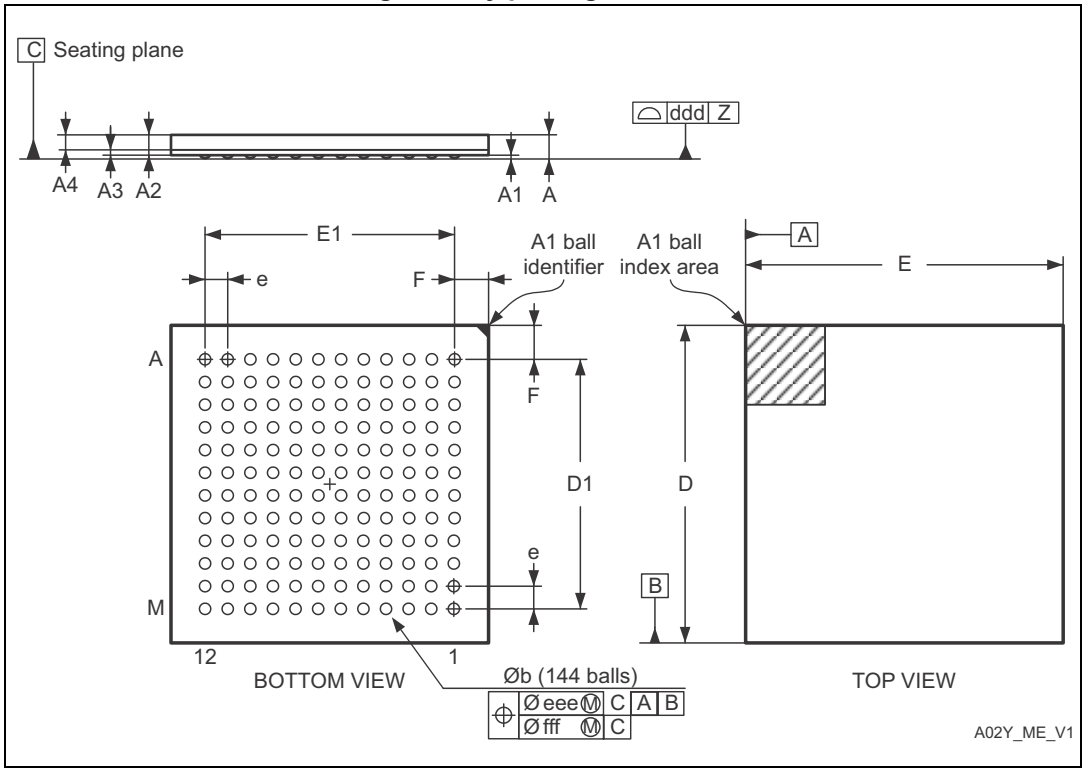



**Table 105. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.5 |
| Dpad | 0.280 mm |
| Dsm | 0.370 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.280 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |

## 7.7 UFBGA144 package information

**Figure 78. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package outline**




1. Drawing is not to scale.

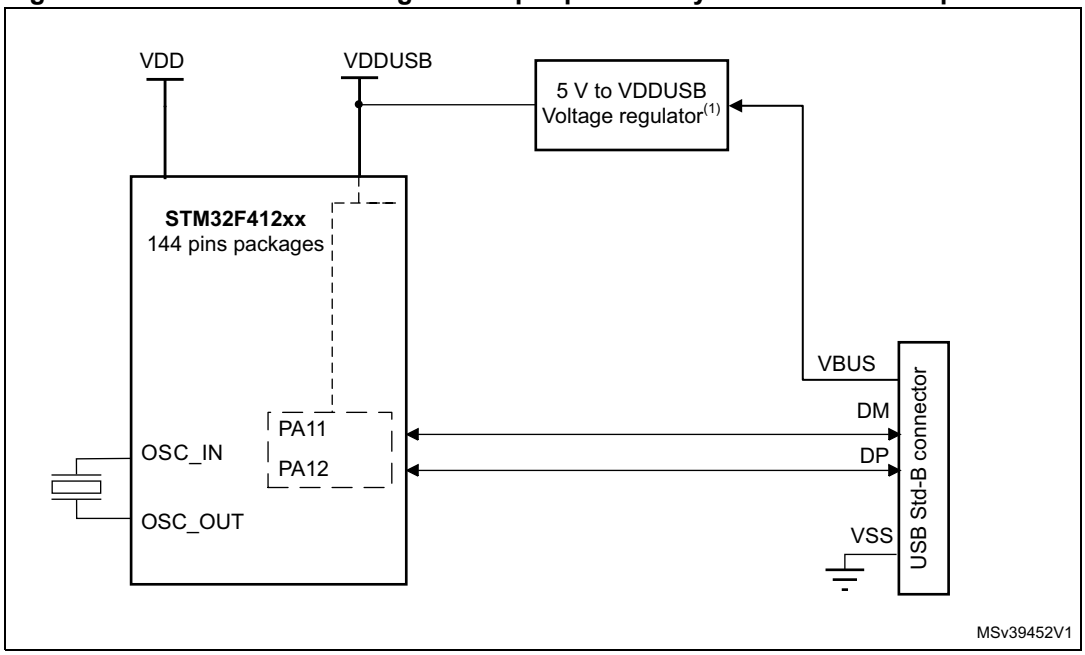
**Table 106. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.0020 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A3 | 0.050 | 0.080 | 0.110 | - | 0.0051 | - |
| A4 | 0.270 | 0.320 | 0.370 | 0.0106 | 0.0126 | 0.0146 |
| b | 0.360 | 0.400 | 0.440 | 0.0091 | 0.0110 | 0.0130 |
| D | 9.950 | 10.000 | 10.050 | 0.2736 | 0.2756 | 0.2776 |
| D1 | 8.750 | 8.800 | 8.850 | 0.2343 | 0.2362 | 0.2382 |
| E | 9.950 | 10.000 | 10.050 | 0.2736 | 0.2756 | 0.2776 |
| E1 | 8.750 | 8.800 | 8.850 | 0.2343 | 0.2362 | 0.2382 |
| e | 0.750 | 0.800 | 0.850 | - | 0.0197 | - |

# Appendix B Application block diagrams

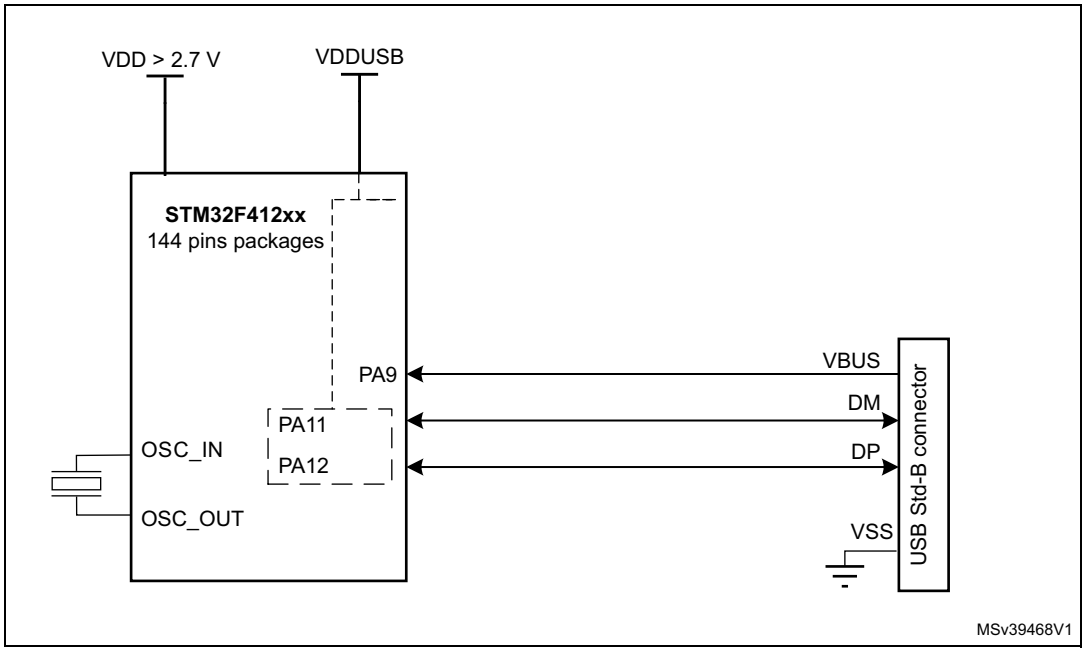
## B.1 USB OTG full speed (FS) interface solutions

**Figure 81. USB controller configured as peripheral-only and used in Full speed mode**




1. External voltage regulator only needed when building a $V_{BUS}$ powered device.

**Figure 82. USB peripheral-only Full speed mode with direct connection for VBUS sense**




1. External voltage regulator only needed when building a $V_{BUS}$ powered device.