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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412vet3

3 Functional overview

3.1 ARM[®] Cortex[®]-M4 with FPU core with embedded Flash and SRAM

The ARM[®] Cortex[®]-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM[®] Cortex[®]-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F412xE/G devices are compatible with all ARM tools and software.

Figure 4 shows the general block diagram of the STM32F412xE/G.

Note: Cortex[®]-M4 with FPU is binary compatible with Cortex[®]-M3.

3.2 Adaptive real-time memory accelerator (ART Accelerator[™])

The ART Accelerator[™] is a memory accelerator which is optimized for STM32 industry-standard ARM[®] Cortex[®]-M4 with FPU processors. It balances the inherent performance advantage of the ARM[®] Cortex[®]-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 125 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 100 MHz.

3.3 Batch Acquisition mode (BAM)

The Batch acquisition mode allows enhanced power efficiency during data batching. It enables data acquisition through any communication peripherals directly to memory using the DMA in reduced power consumption as well as data processing while the rest of the system is in low-power mode (including the flash and ART). For example in an audio system, a smart combination of PDM audio sample acquisition and processing from the DFSDM directly to RAM (flash and ART[™] stopped) with the DMA using BAM followed by some very short processing from flash allows to drastically reduce the power consumption of the application. A dedicated application note (AN4515) describes how to implement the STM32F412xE/G BAM to allow the best power efficiency.

3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 byte and the whole 4 Gbyte of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.5 Embedded Flash memory

The devices embed up to 1 Mbyte of Flash memory available for storing programs and data.

The Flash user area can be protected against reading by an entrusted code (Read Protection, RDP) with different protection levels.

The flash user sectors can also be individually protected against write operation.

Furthermore the proprietary readout protection (PCROP) can also individually protect the flash user sectors against D-bus read accesses.

(Additional information can be found in the product reference manual).

To optimize the power consumption the Flash memory can also be switched off in Run or in Sleep mode (see [Section 3.21: Low-power modes](#)).

Two modes are available: Flash in Stop mode or in DeepSleep mode (trade off between power saving and startup time).

Before disabling the Flash, the code must be executed from the internal RAM.

3.6 One-time programmable bytes

A one-time programmable area is available with 16 OTP blocks of 32 bytes. Each block can be individually locked

(Additional information can be found in the product reference manual)

3.7 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run mode)
In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.
- LPR is used in the Stop mode
The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.
The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Depending on the package, one or two external ceramic capacitors should be connected on the VCAP_1 and VCAP_2 pins. The VCAP_2 pin is only available for the 100 pins and 144 pins packages.

All packages have the regulator ON feature.

3.19.2 Regulator OFF

This feature is available only on UFBGA100 and UFBGA144 packages, which feature the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through VCAP_1 and VCAP_2 pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.

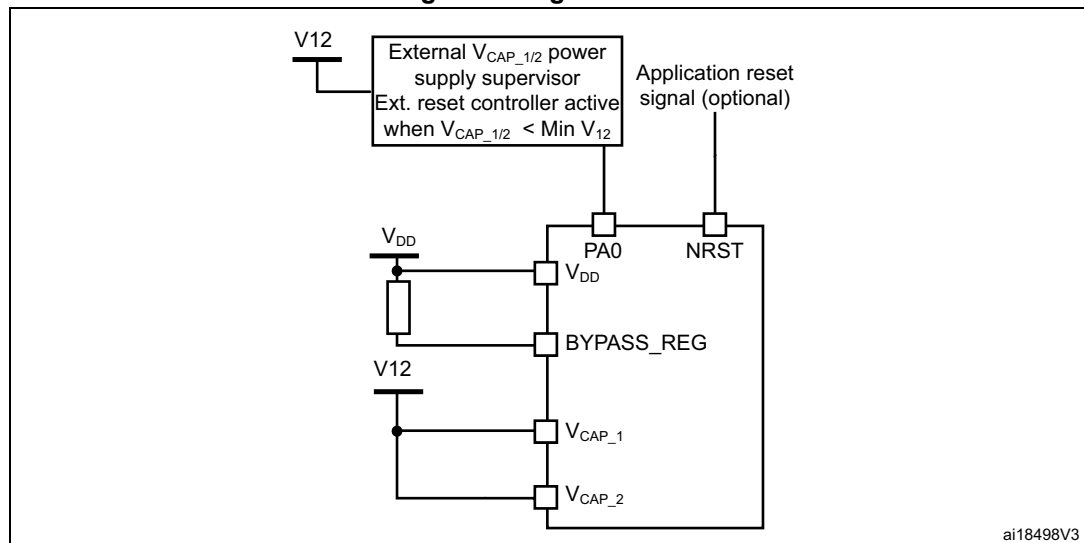
The two 2.2 μ F ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12} . An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.

Figure 8. Regulator OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V₁₂ minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V₁₂ minimum value and until V_{DD} reaches 1.7 V (see [Figure 9](#)).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V₁₂ minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 10](#)).
- If V_{CAP_1} and V_{CAP_2} go below V₁₂ minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V₁₂ depends on the maximum frequency targeted in the application.

Table 9. STM32F412xE/G pin definition

Pin Number							Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WL CSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	1	B2	A3	1	PE2	I/O	FT	-	TRACECLK, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, QUADSPI_BK1_IO2, FSMC_A23, EVENTOUT	-
-	-	-	2	A1	A2	2	PE3	I/O	FT	-	TRACED0, FSMC_A19, EVENTOUT	-
-	-	-	3	B1	B2	3	PE4	I/O	FT	-	TRACED1, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, DFSDM1_DATIN3, FSMC_A20, EVENTOUT	-
-	-	-	4	C2	B3	4	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SPI5_MISO, DFSDM1_CKIN3, FSMC_A21, EVENTOUT	-
-	-	-	5	D2	B4	5	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, FSMC_A22, EVENTOUT	-
1	1	B7	6	E2	C2	6	VBAT	S	-	-	-	VBAT
2	2	B8	7	C1	A1	7	PC13	I/O	FT	(2)(3)	EVENTOUT	TAMP_1
3	3	C8	8	D1	B1	8	PC14- OSC32_IN	I/O	FT	(2)(3) (4)	EVENTOUT	OSC32_IN
4	4	C7	9	E1	C1	9	PC15- OSC32_ OUT	I/O	FT	(2)(4)	EVENTOUT	OSC32_ OUT
-	-	-	-	-	C3	10	PF0	I/O	FT	-	I2C2_SDA, FSMC_A0, EVENTOUT	-
-	-	-	-	-	C4	11	PF1	I/O	FT	-	I2C2_SCL, FSMC_A1, EVENTOUT	-
-	-	-	-	-	D4	12	PF2	I/O	FT	-	I2C2_SMBA, FSMC_A2, EVENTOUT	-
-	-	-	-	-	E2	13	PF3	I/O	FT	-	TIM5_CH1, FSMC_A3, EVENTOUT	-
-	-	-	-	-	E3	14	PF4	I/O	FT	-	TIM5_CH2, FSMC_A4, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WL CSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	K1	K1	-	VREF-	S	-	-	-	-
9	13	F7	-	-	-	-	VDDA/ VREF+	S	-	-	-	-
-	-	-	21	L1	L1	32	VREF+	S	-	-	-	-
-	-	-	22	M1	M1	33	VDDA	S	-	-	-	-
10	14	E6	23	L2	J2	34	PA0	I/O	FT	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, EVENTOUT	ADC1_0, WKUP1
11	15	G7	24	M2	K2	35	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, SPI4_MOSI/I2S4_SD, USART2_RTS, QUADSPI_BK1_IO3, EVENTOUT	ADC1_1
12	16	H8	25	K3	L2	36	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, I2S2_CKIN, USART2_TX, FSMC_D4, EVENTOUT	ADC1_2
13	17	F6	26	L3	M2	37	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, I2S2_MCK, USART2_RX, FSMC_D5, EVENTOUT	ADC1_3
-	18	-	27	-	G4	38	VSS	S	-	-	-	-
-	-	-	-	E3	H5	-	BYPASS_ REG	I	FT	-	-	-
-	19	H7	28	-	F4	39	VDD	S	-	-	-	-
14	20	G6	29	M3	J3	40	PA4	I/O	FT	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, DFSDM1_DATIN1, FSMC_D6, EVENTOUT	ADC1_4
15	21	F5	30	K4	K3	41	PA5	I/O	FT	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, DFSDM1_CKIN1, FSMC_D7, EVENTOUT	ADC1_5

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
27	35	G1	53	K11	L11	75	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, I2CFMP1_SDA, SPI2_MISO, I2S2ext_SD, USART3_RTS, DFSDM1_DATIN2, TIM12_CH1, FSMC_D0, SDIO_D6, EVENTOUT	-
28	36	F2	54	K10	L12	76	PB15	I/O	FT	-	RTC_50Hz, TIM1_CH3N, TIM8_CH3N, I2CFMP1_SCL, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, TIM12_CH2, SDIO_CK, EVENTOUT	-
-	-	-	55	-	L9	77	PD8	I/O	FT	-	USART3_TX, FSMC_D13/ FSMC_DA13, EVENTOUT	-
-	-	-	56	K8	K9	78	PD9	I/O	FT	-	USART3_RX, FSMC_D14/FSMC_DA14, EVENTOUT	-
-	-	-	57	J12	J9	79	PD10	I/O	FT	-	USART3_CK, FSMC_D15/FSMC_DA15, EVENTOUT	-
-	-	-	58	J11	H9	80	PD11	I/O	FT	-	I2CFMP1_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FSMC_A16, EVENTOUT	-
-	-	-	59	J10	L10	81	PD12	I/O	FT	-	TIM4_CH1, I2CFMP1_SCL, USART3_RTS, QUADSPI_BK1_IO1, FSMC_A17, EVENTOUT	-
-	-	-	60	H12	K10	82	PD13	I/O	FT	-	TIM4_CH2, I2CFMP1_SDA, QUADSPI_BK1_IO3, FSMC_A18, EVENTOUT	-
-	-	-	-	-	G8	83	VSS	S	-	-	-	-
-	-	-	-	-	F8	84	VDD	S	-	-	-	-

Table 20. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PDRhyst}^{(2)}$	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	
		Rising edge	2.53	2.59	2.63	
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	
		Rising edge	2.85	2.92	2.97	
$V_{BORhyst}^{(2)}$	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}^{(2)(3)}$	POR reset timing	-	0.5	1.5	3.0	ms
$I_{RUSH}^{(2)}$	In-Rush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
$E_{RUSH}^{(2)}$	In-Rush energy on voltage regulator power-on (POR or wakeup from Standby)	$V_{DD} = 1.7\text{ V}$, $T_A = 105\text{ }^{\circ}\text{C}$, $I_{RUSH} = 171\text{ mA}$ for $31\text{ }\mu\text{s}$	-	-	5.4	μC

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.
3. The reset timing is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is fetched by the user application code.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 22: Current consumption measurement scheme](#).

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 40. HSE 4-26 MHz oscillator characteristics⁽¹⁾

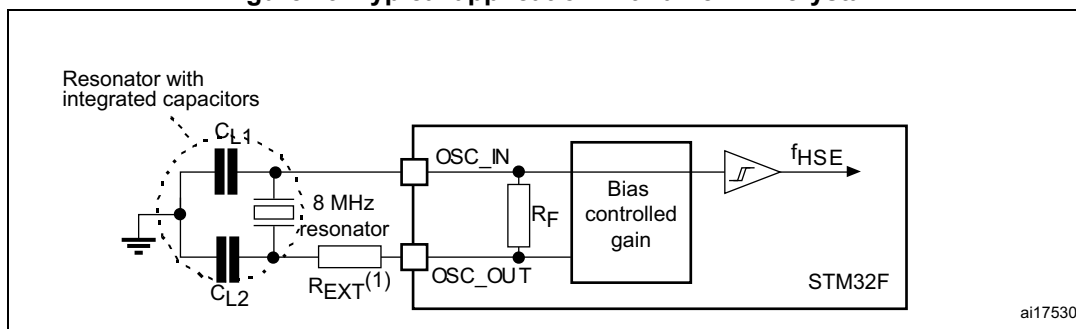
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	-	26	MHz
R_F	Feedback resistor		-	200	-	k Ω
I_{DD}	HSE current consumption	$V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=5\text{ pF @25 MHz}$	-	450	-	μA
		$V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=10\text{ pF @25 MHz}$	-	530	-	
$ACC_{HSE}^{(2)}$	HSE accuracy	-	-500	-	500	ppm
$G_{m_crit_max}$	Maximum critical crystal g_m	Startup	-	-	1	mA/V
$t_{SU(HSE)}^{(3)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design, not tested in production.
2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 29](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 29. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 41](#). In the application, the resonator and the load capacitors have to be placed as close as

The test results are given in [Table 52](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 51. EMS characteristics for LQFP144 package

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, LQFP144 $T_A = +25\text{ }^{\circ}\text{C}$, $f_{HCLK} = 100\text{ MHz}$, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, LQFP144 $T_A = +25\text{ }^{\circ}\text{C}$, $f_{HCLK} = 100\text{ MHz}$, conforms to IEC 61000-4-4	4B

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP144 packages and PDR_ON on WLCSP49.

As a consequence, it is recommended to add a serial resistor (1 k Ω maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

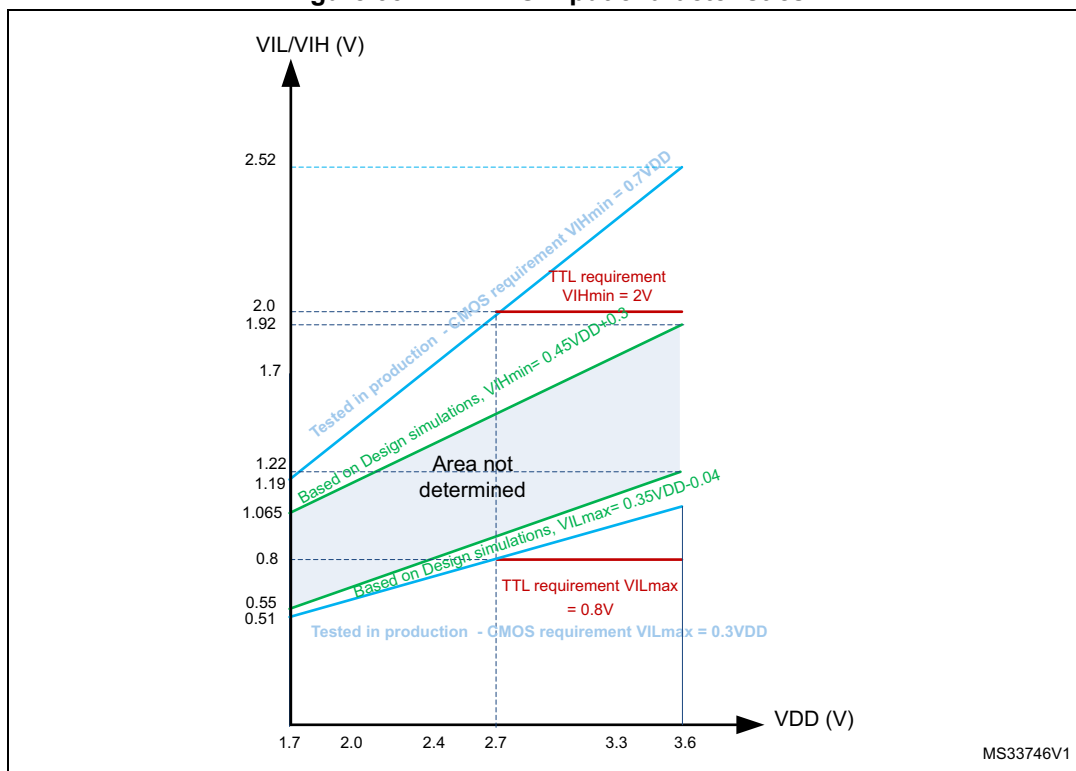
- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Figure 35. FT/TC I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ± 3 mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#). In particular:

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 13](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 13](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 57](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 15](#). All I/Os are CMOS and TTL compliant.

Table 57. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$1.3^{(4)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-1.3^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +6 \text{ mA}$ $1.8 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$0.4^{(4)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +4 \text{ mA}$ $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$0.4^{(5)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4^{(5)}$	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 13](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 13](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
4. Guaranteed by characterization results, not tested in production.
5. Guaranteed by design, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 36](#) and [Table 58](#), respectively.

Unless otherwise specified, the parameters given in [Table 58](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 15](#).

Table 58. I/O AC characteristics⁽¹⁾⁽²⁾

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{\max(I/O)out}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{DD} \geq 2.70 \text{ V}$	-	-	4	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} \geq 1.7 \text{ V}$	-	-	2	
			$C_L = 10 \text{ pF}$, $V_{DD} \geq 2.70 \text{ V}$	-	-	8	
			$C_L = 10 \text{ pF}$, $V_{DD} \geq 1.7 \text{ V}$	-	-	4	
	$t_{f(I/O)out}/$ $t_{r(I/O)out}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}$, $V_{DD} = 1.7 \text{ V}$ to 3.6 V	-	-	100	ns

2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 μ A current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Figure 45. USB OTG FS timings: definition of data signal rise and fall time

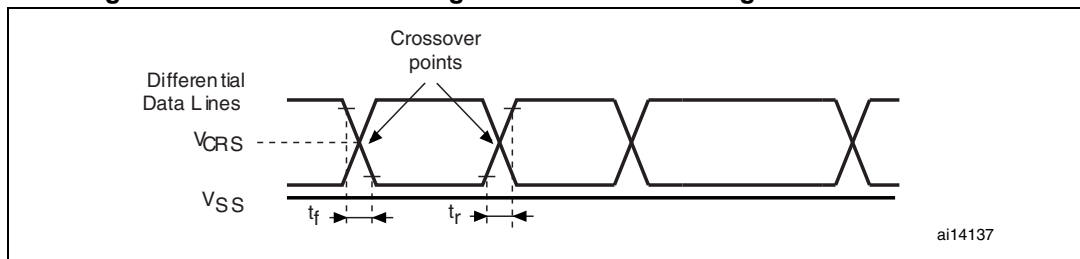


Table 70. USB OTG FS electrical characteristics⁽¹⁾

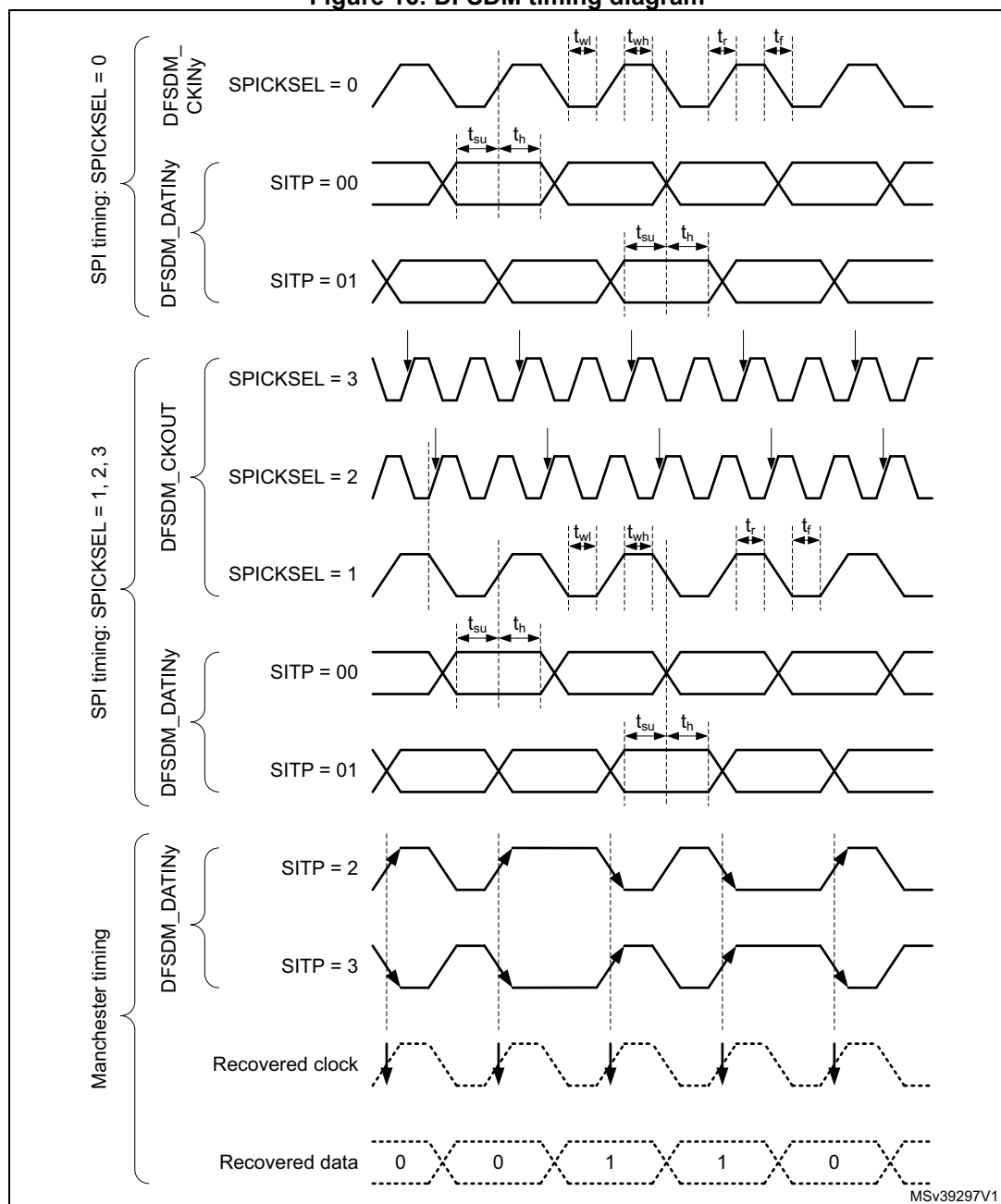
Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time ⁽²⁾	$C_L = 50$ pF	4	20	ns
t_f	Fall time ⁽²⁾	$C_L = 50$ pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

CAN (controller area network) interface

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

Figure 16: DFSDM timing diagram



6.3.25 FSMC characteristics

Unless otherwise specified, the parameters given in [Table 83](#) to [Table 90](#) for the FSMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in [Table 14](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitance load $C = 30$ pF
- Measurement points are done at CMOS levels: $0.5 \cdot V_{DD}$

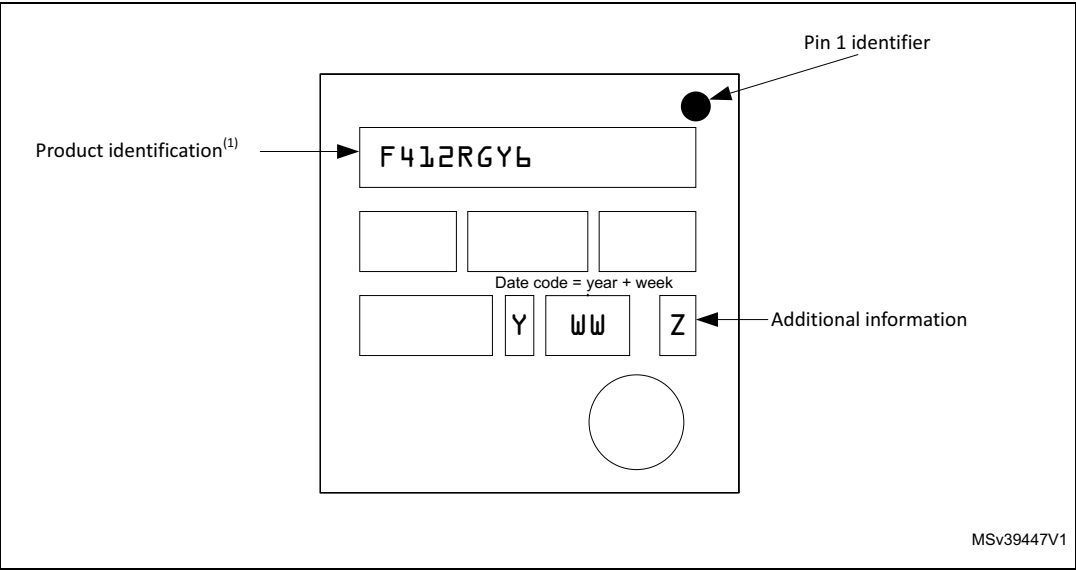
Table 99. WLCSP64 recommended PCB design rules (0.4 mm pitch) (continued)

Dimension	Recommended values
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking for WLCSP64

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 62. WLCSP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

1. Dimensions are in millimeters.

The following figure gives an example of topside marking and pin 1 position identifier location.

Diagram illustrating the package top view of the STM32F412RGTL6, showing the following markings:

- Product identification⁽¹⁾**: Points to the markings **STM32F412** and **RGTL6**.
- Revision code**: Points to the marking **R**.
- Date code**: Points to the markings **Y** and **WW**.
- Pin 1 identifier**: Points to the black circle marking.

The diagram also shows the **ST** logo and a circular marking.

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1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 104. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 76. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

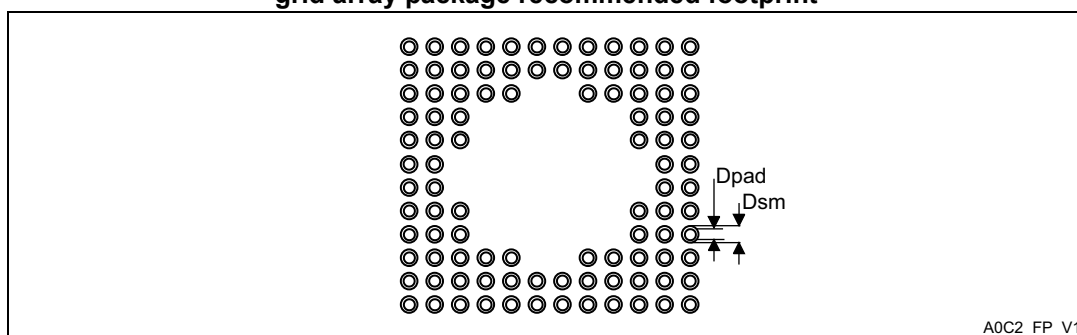


Table 105. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

8 Part numbering

Table 109. Ordering information scheme

Example:	STM32	F	412	C	E	T	6	TR
Device family								
STM32 = ARM®-based 32-bit microcontroller								
Product type								
F = General-purpose								
Device subfamily								
412 = 412 line								
Pin count								
C = 48 pins								
R = 64 pins								
V = 100 pins								
Z = 144 pins								
Flash memory size								
E = 512 Kbytes of Flash memory								
G = 1024 Kbytes of Flash memory								
Package								
H = UFBGA 7 x 7 mm								
J = UFBGA 10 x 10 mm								
T = LQFP								
U = UFQFPN								
Y = WLCSP								
Temperature range								
6 = Industrial temperature range, –40 to 85 °C								
Packing								
TR = tape and reel								
No character = tray or tube								

Appendix A Recommendations when using the internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on-reset (POR)/power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled. By default BOR is OFF.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD} .