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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412vet3tr

2.1 Compatibility with STM32F4 series

The STM32F412xE/G are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F412xE/G can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

Figure 1. Compatible board design for LQFP100 package
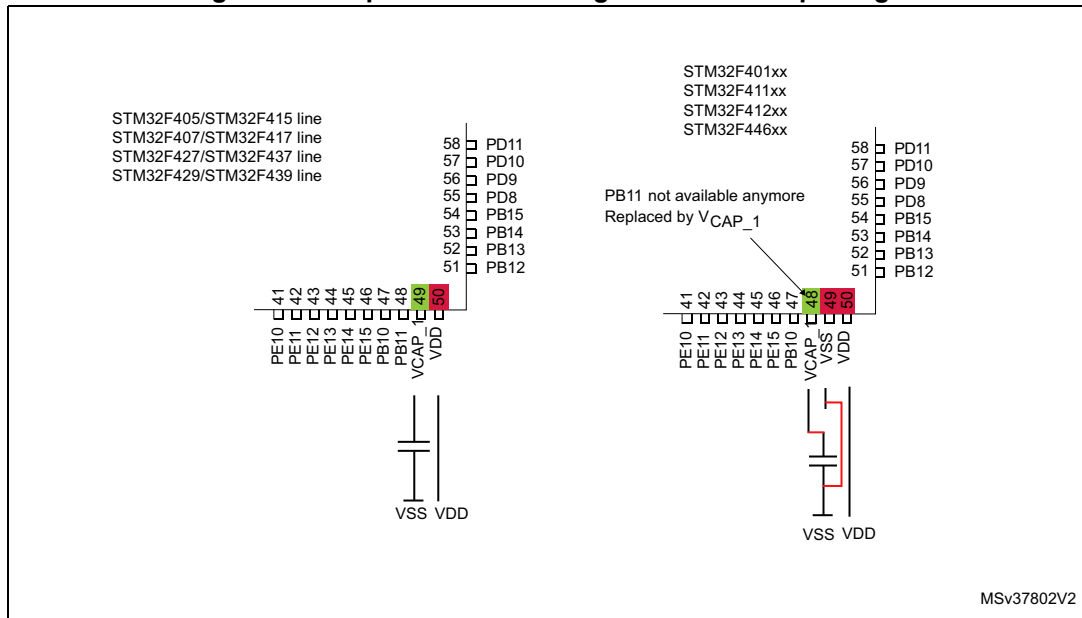
3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 byte and the whole 4 Gbyte of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.5 Embedded Flash memory

The devices embed up to 1 Mbyte of Flash memory available for storing programs and data.

The Flash user area can be protected against reading by an entrusted code (Read Protection, RDP) with different protection levels.

The flash user sectors can also be individually protected against write operation.

Furthermore the proprietary readout protection (PCROP) can also individually protect the flash user sectors against D-bus read accesses.

(Additional information can be found in the product reference manual).

To optimize the power consumption the Flash memory can also be switched off in Run or in Sleep mode (see *Section 3.21: Low-power modes*).

Two modes are available: Flash in Stop mode or in DeepSleep mode (trade off between power saving and startup time.

Before disabling the Flash, the code must be executed from the internal RAM.

3.6 One-time programmable bytes

A one-time programmable area is available with16 OTP blocks of 32 bytes. Each block can be individually locked

(Additional information can be found in the product reference manual)

3.7 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

The DMA can be used with the main peripherals:

- SPI and I^{2}S
- I^{2}C and I^{2}CFMP
- USART
- General-purpose, basic and advanced-control timers TIMx
- SD/SDIO/MMC/eMMC host interface
- Quad-SPI
- ADC
- Digital Filter for sigma-delta modulator (DFSDM) with a separate stream for each filter.

3.11 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes a NOR/PSRAM memory controller. It features four Chip Select outputs supporting the following modes: SRAM, PSRAM and NOR Flash memory.

The main functions are:

- 8-,16-bit data bus width
- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 90 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.12 Quad-SPI memory interface (QUAD-SPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting single, dual or quad-SPI Flash memories. It can work in direct mode through registers, external Flash status register polling mode and memory mapped mode. Up to 256 Mbyte of external Flash memory are mapped. They can be accessed in 8, 16 or 32-bit mode. Code execution is also supported. The opcode and the frame format are fully programmable. Communication can be performed either in single data rate or dual data rate.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run mode)

  In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.

- LPR is used in the Stop mode

  The LP regulator mode is configured by software when entering Stop mode.

- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Depending on the package, one or two external ceramic capacitors should be connected on the V_{CAP_1} and V_{CAP_2} pins. The V_{CAP_2} pin is only available for the 100 pins and 144 pins packages.

All packages have the regulator ON feature.

3.19.2 Regulator OFF

This feature is available only on UFBGA100 and UFBGA144 packages, which feature the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.

- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.

The DFSDM peripheral supports:

- 4 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0...20 MHz
- alternative inputs from 4 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: device memory data streams (DMA)
- 2 digital filter modules with adjustable digital signal processing:
  - Sinc^x filter: filter order/type (1...5), oversampling ratio (up to 1...1024)
  - integrator: oversampling ratio (1...256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM1FLT0)
- analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable Sinc^x digital filter (order = 1...3, oversampling ratio = 1...32
  - input from digital output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion
- short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1...256 consecutive 0's or 1's on serial data stream
  - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit input serial channel clock absence
- "regulator" or injected" conversions:
  - "regular" conversions can be requested at any time or even in continuous mode without having any impact on the timing of "injected" conversions
  - "injected" conversions for precise timing and with high conversion priority.

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)[(1)]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	88	A5	A9	123	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, FSMC_NE1, EVENTOUT	-
-	-	-	-	-	E8	124	PG9	I/O	FT	-	USART6_RX, QUADSPI_BK2_IO2, FSMC_NE2, EVENTOUT	-
-	-	-	-	-	D8	125	PG10	I/O	FT	-	FSMC_NE3, EVENTOUT	-
-	-	-	-	-	C8	126	PG11	I/O	FT	-	CAN2_RX, EVENTOUT	-
-	-	-	-	-	B8	127	PG12	I/O	FT	-	USART6_RTS, CAN2_TX, FSMC_NE4, EVENTOUT	-
-	-	-	-	-	D7	128	PG13	I/O	FT	-	TRACED2, USART6_CTS, FSMC_A24, EVENTOUT	-
-	-	-	-	-	C7	129	PG14	I/O	FT	-	TRACED3, USART6_TX, QUADSPI_BK2_IO3, FSMC_A25, EVENTOUT	-
-	-	-	-	-	-	130	VSS	S	-	-	-	-
-	-	-	-	-	F6	131	VDD	S	-	-	-	-
-	-	-	-	-	B7	132	PG15	I/O	FT	-	USART6_CTS, EVENTOUT	-
39	55	A5	89	A8	A7	133	PB3	I/O	FT	-	JTDO-SWO, TIM2_CH2, I2CFMP1_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, I2C2_SDA, EVENTOUT	-
40	56	B4	90	A7	A6	134	PB4	I/O	FT	-	JTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, I2C3_SDA, SDIO_D0, EVENTOUT	-
41	57	C4	91	C5	B6	135	PB5	I/O	FT	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, CAN2_RX, SDIO_D3, EVENTOUT	-

Table 10. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	FSMC_A0	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	FSMC_A1	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	FSMC_A2	EVENTOUT
	PF3	-	-	TIM5_CH1	-	-	-	-	-	-	-	-	FSMC_A3	EVENTOUT
	PF4	-	-	TIM5_CH2	-	-	-	-	-	-	-	-	FSMC_A4	EVENTOUT
	PF5	-	-	TIM5_CH3	-	-	-	-	-	-	-	-	FSMC_A5	EVENTOUT
	PF6	TRACED0	-	-	TIM10_CH1	-	-	-	-	-	QUADSPI_ BK1_IO3	-	-	EVENTOUT
	PF7	TRACED1	-	-	TIM11_CH1	-	-	-	-	-	QUADSPI_ BK1_IO2	-	-	EVENTOUT
	PF8	-	-	-	-	-	-	-	-	-	TIM13_CH1	QUADSPI_ BK1_IO0	-	EVENTOUT
	PF9	-	-	-	-	-	-	-	-	-	TIM14_CH1	QUADSPI_ BK1_IO1	-	EVENTOUT
	PF10	-	TIM1_ETR	TIM5_CH4	-	-	-	-	-	-	-	-	-	EVENTOUT
	PF11	-	-	-	TIM8_ETR	-	-	-	-	-	-	-	-	EVENTOUT
	PF12	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	FSMC_A6	EVENTOUT
	PF13	-	-	-	-	I2CFMP1_ SMBA	-	-	-	-	-	-	FSMC_A7	EVENTOUT
	PF14	-	-	-	-	I2CFMP1_ SCL	-	-	-	-	-	-	FSMC_A8	EVENTOUT
	PF15	-	-	-	-	I2CFMP1_ SDA	-	-	-	-	-	-	FSMC_A9	EVENTOUT

Table 15. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_D	Power dissipation at TA = 85°C for range 6 or TA = 105°C for range 7[8]	UFQFPN48	-	-	625	mW
		WLCSP64	-	-	392	
		LQFP64	-	-	425	
		LQFP100	-	-	465	
		LQFP144			571	
		UFBGA100	-	-	351	
		UFBGA144	-	-	416	
T_A	Ambient temperature for range 6	Maximum power dissipation	–40	-	85	°C
		Low power dissipation[9]	–40	-	105	
	Ambient temperature for range 7	Maximum power dissipation	–40	-	105	
		Low power dissipation[9]	–40	-	125	
T_J	Junction temperature range	Range 6	–40	-	105	
		Range 7	–40	-	125	

1. V_{DD}/V_{DDA} minimum value of 1.7 V with the use of an external power supply supervisor (refer to *Section 3.18.2: Internal reset OFF*).

2. When the ADC is used, refer to *Table 71: ADC characteristics*.

3. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF}+ < 1.2 V.

4. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.

5. Only the DM (P_{A11}) and DP (P_{A12}) pads are supplied through V_{DDUSB}. For application where the V_{BUS} (P_{A9}) is directly connected to the chip, a minimum V_{DD} supply of 2.7V is required.

    (some application examples are shown in appendix B)

6. Guaranteed by test in production

7. To sustain a voltage higher than V_{DD}+0.3, the internal Pull-up and Pull-Down resistors must be disabled

8. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.

9. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 24. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - V_DD = 3.6 V

Symbol	Parameter	Conditions	f_HCLK (MHz)	Typ	Max[1]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_DD	Supply current in **Run mode**	External clock, PLL ON[2], all peripherals enabled[3]	100	27.2	28.70[4]	30.14	31.98	mA
			84	21.9	23.60	24.31	25.37	
			64	15.2	16.45	17.03	17.87	
			50	12.1	13.12	13.67	14.46	
			25	6.6	7.59	8.12	8.77	
			20	5.7	6.51	7.07	7.77	
		HSI, PLL OFF, all peripherals enabled[3]	16	4.0	4.32	4.88	5.69	
			1	0.8	1.14	1.67	2.38	
		External clock, PLL ON[2] all peripherals disabled[3]	100	13.0	14.06[4]	15.34	17.27	
			84	10.5	11.21	12.16	13.47	
			64	7.5	8.29	9.01	9.88	
			50	6.0	6.73	7.32	8.27	
			25	3.5	4.18	4.73	5.57	
			20	3.1	3.72	4.25	5.10	
		HSI, PLL OFF, all peripherals disabled[3]	16	2.1	2.41	2.94	3.75	
			1	0.7	0.99	1.51	2.30	

1. Based on characterization, not tested in production unless otherwise specified.

2. Refer to *Table 44* and RM0383 for the possible PLL VCO setting

3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

4. Tested in production.

pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics [1]

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}[2]	Frequency	17	32	47	kHz
$t_{su(LSI)}$[3]	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$[3]	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.

2. Guaranteed by characterization, not tested in production.

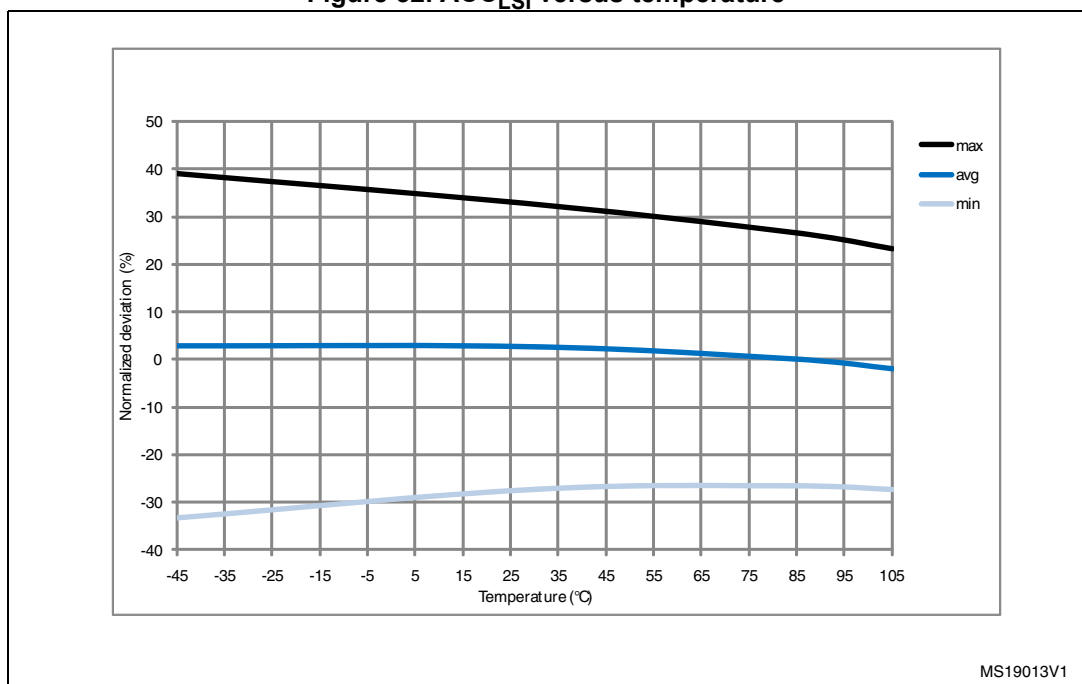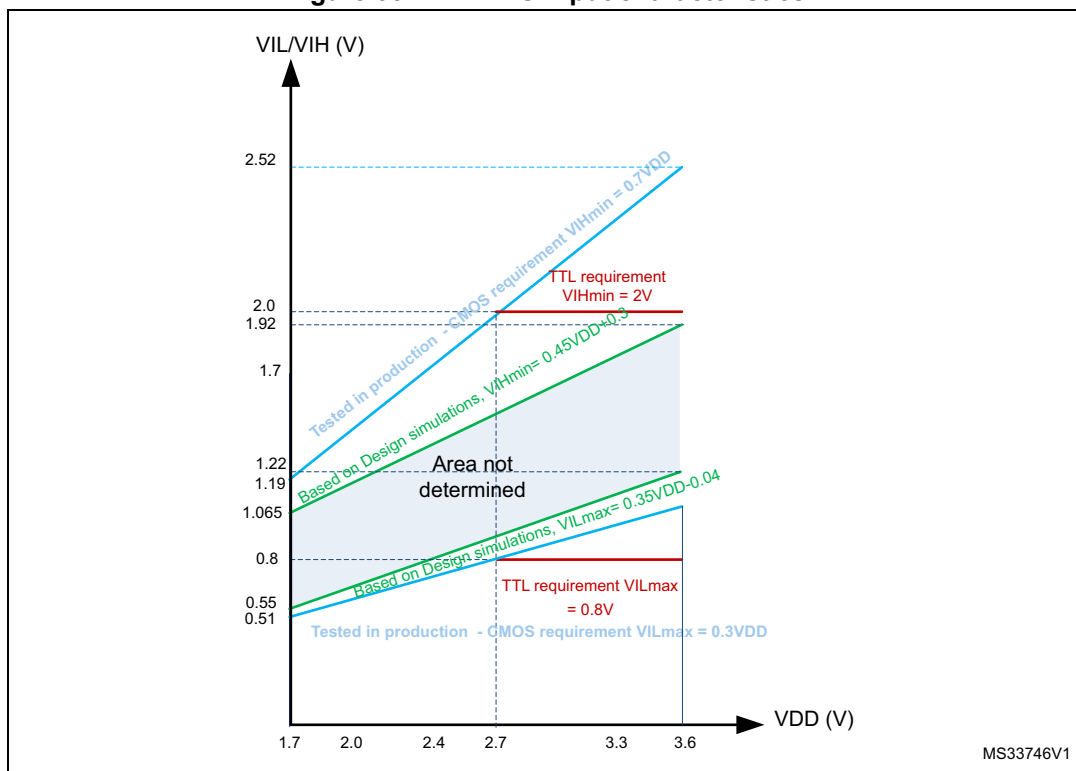3. Guaranteed by design, not tested in production.

Figure 32. ACC$_{LSI}$ versus temperature

Figure 35. FT/TC I/O input characteristics

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 13*).

- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 13*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*. All I/Os are CMOS and TTL compliant.

Table 73. ADC accuracy at f_{ADC} = 30 MHz[1]

Symbol	Parameter	Test conditions	Typ	Max[2]	Unit
ET	Total unadjusted error	f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V, $V_{DDA} - V_{REF}$ < 1.2 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±4	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.

2. Guaranteed by characterization, not tested in production.

Table 74. ADC accuracy at f_{ADC} = 36 MHz[1]

Symbol	Parameter	Test conditions	Typ	Max[2]	Unit
ET	Total unadjusted error	f_{ADC} = 36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.

2. Guaranteed by characterization, not tested in production.

Table 75. ADC dynamic accuracy at f_{ADC} = 18 MHz - limited test conditions[1]

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =18 MHz V_{DDA} = V_{REF+}= 1.7 V Input Frequency = 20 kHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		-	-72	-67	

1. Guaranteed by characterization, not tested in production.

Table 76. ADC dynamic accuracy at f_{ADC} = 36 MHz - limited test conditions[1]

| Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 36 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 20 kHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		-	-72	-70	

1. Guaranteed by characterization, not tested in production.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 48* or *Figure 49*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 48. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})
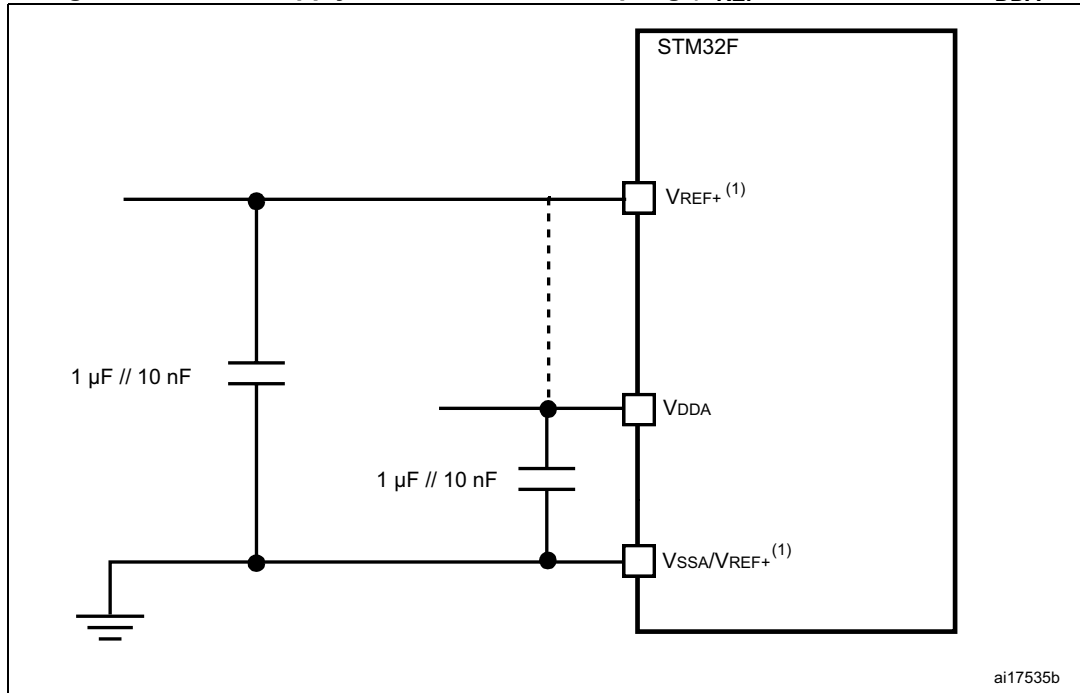
1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.24 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 82* for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in *Table 15: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 $_x$ VDD

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM_CKINy, DFSDM_DATINy, DFSDM_CKOUT for DFSDM).

Table 82. DFSDM characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	-	-	-	f_{SYSCLK}	MHz
f_{CKIN} $(1/T_{CKIN})$	Input clock frequency	SPI mode (SITP[1:0] = 01)	-	-	20 $(f_{DFSDMCLK}/4)$	MHz
f_{CKOUT}	Output clock frequency	-	-	-	20	MHz
$DuCy_{CKOUT}$	Output clock frequency duty cycle	-	30	50	75	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0)	$T_{CKIN}/2$-0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	1	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	1	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0)	(CKOUT DIV+1) $_x$ $T_{DFSDMCLK}$	-	(2 $_x$ CKOUTDIV) $_x$ $T_{DFSDMCLK}$	

1. Data based on characterization results, not tested in production.
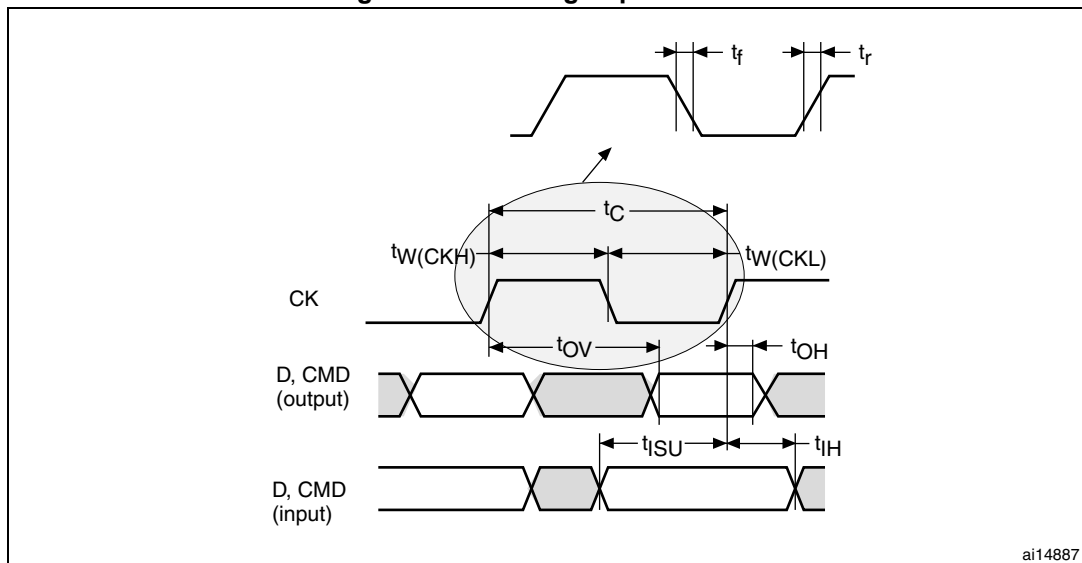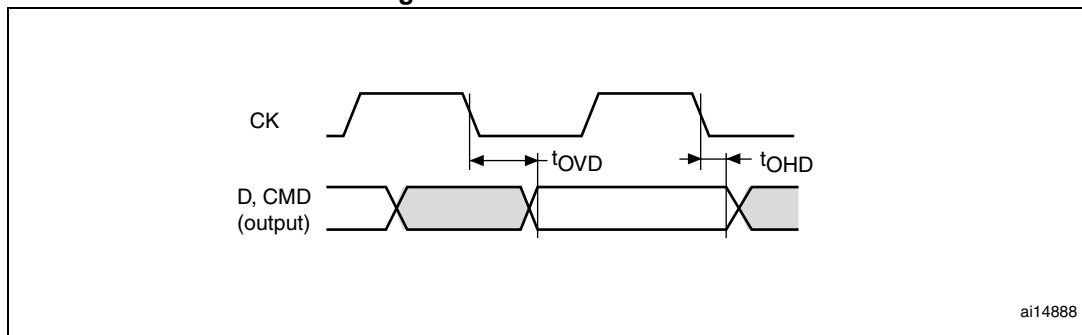
Figure 58. SDIO high-speed mode


Figure 59. SD default mode

Table 95. Dynamic characteristics: SD / MMC characteristics[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50MHz	4	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	13	13.5	ns
t_{OH}	Output hold time HS	fpp =50MHz	11	-	-	

Device marking for UFQFPN48

The following figure gives an example of topside marking and pin 1 position identifier location.

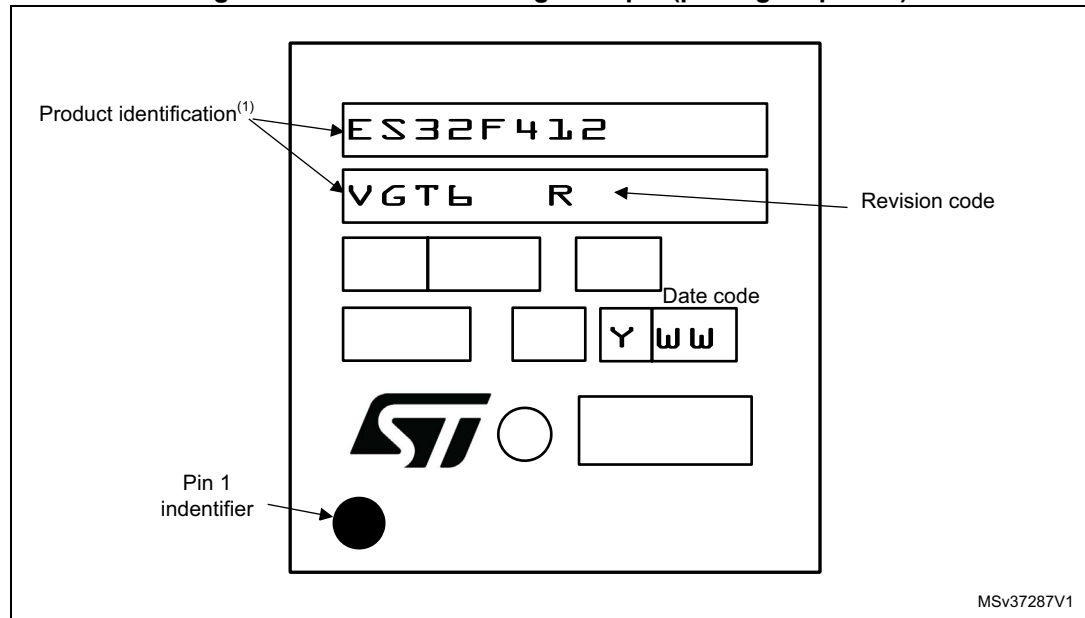**Figure 65. UFQFPN48 marking example (package top view)**
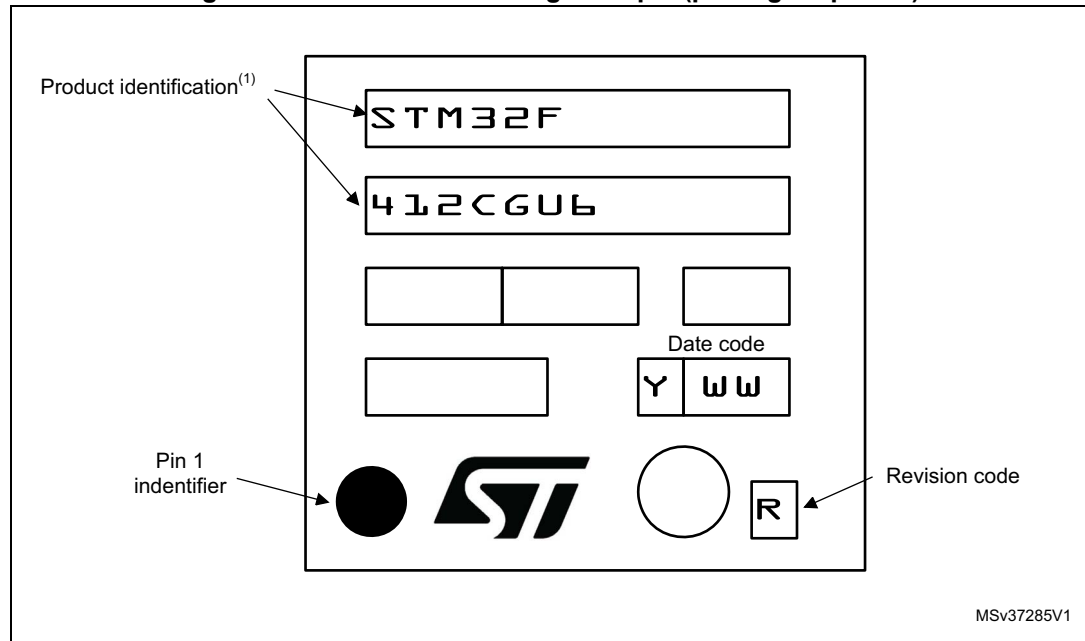
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking for LQFP100

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 71. LQFP100 marking example (package top view)

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.