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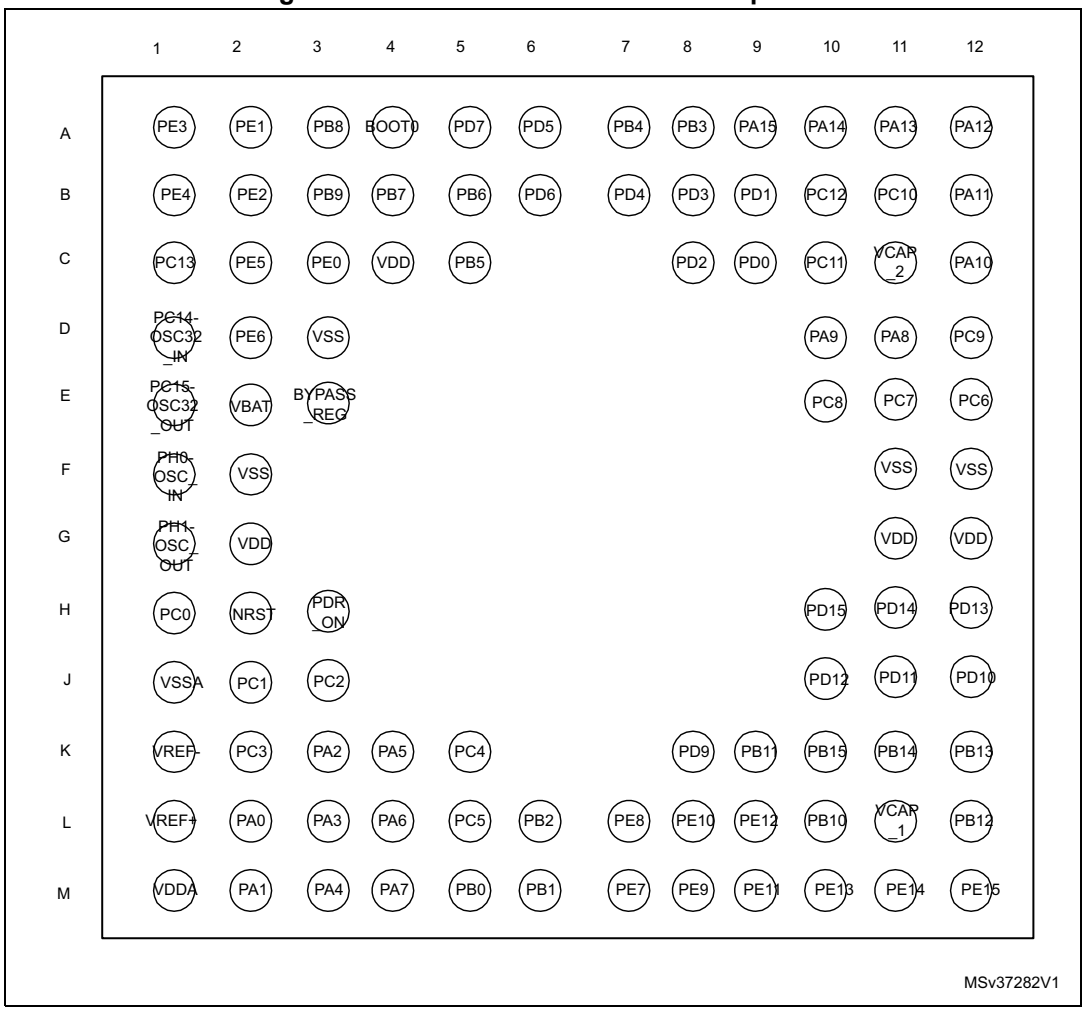
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412vet6

Figure 16. STM32F412xE/G UFBGA100 pinout



1. The above figure shows the package top view.

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	K1	K1	-	VREF-	S	-	-	-	-
9	13	F7	-	-	-	-	VDDA/ VREF+	S	-	-	-	-
-	-	-	21	L1	L1	32	VREF+	S	-	-	-	-
-	-	-	22	M1	M1	33	VDDA	S	-	-	-	-
10	14	E6	23	L2	J2	34	PA0	I/O	FT	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, EVENTOUT	ADC1_0, WKUP1
11	15	G7	24	M2	K2	35	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, SPI4_MOSI/I2S4_SD, USART2_RTS, QUADSPI_BK1_IO3, EVENTOUT	ADC1_1
12	16	H8	25	K3	L2	36	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, I2S2_CKIN, USART2_TX, FSMC_D4, EVENTOUT	ADC1_2
13	17	F6	26	L3	M2	37	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, I2S2_MCK, USART2_RX, FSMC_D5, EVENTOUT	ADC1_3
-	18	-	27	-	G4	38	VSS	S	-	-	-	-
-	-	-	-	E3	H5	-	BYPASS_ REG	I	FT	-	-	-
-	19	H7	28	-	F4	39	VDD	S	-	-	-	-
14	20	G6	29	M3	J3	40	PA4	I/O	FT	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, DFSDM1_DATIN1, FSMC_D6, EVENTOUT	ADC1_4
15	21	F5	30	K4	K3	41	PA5	I/O	FT	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, DFSDM1_CKIN1, FSMC_D7, EVENTOUT	ADC1_5

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
16	22	H6	31	L4	L3	42	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, I2S2_MCK, TIM13_CH1, QUADSPI_BK2_IO0, SDIO_CMD, EVENTOUT	ADC1_6
17	23	E5	32	M4	M3	43	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, QUADSPI_BK2_IO1, EVENTOUT	ADC1_7
-	24	E4	33	K5	J4	44	PC4	I/O	FT	-	I2S1_MCK, QUADSPI_BK2_IO2, FSMC_NE4, EVENTOUT	ADC1_14
-	25	G5	34	L5	K4	45	PC5	I/O	FT	-	I2CFMP1_SMBA, USART3_RX, QUADSPI_BK2_IO3, FSMC_NOE, EVENTOUT	ADC1_15
18	26	H5	35	M5	L4	46	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI5_SCK/I2S5_CK, EVENTOUT	ADC1_8
19	27	F4	36	M6	M4	47	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, SPI5_NSS/I2S5_WS, DFSDM1_DATIN0, QUADSPI_CLK, EVENTOUT	ADC1_9
20	28	G4	37	L6	J5	48	PB2	I/O	FT	-	DFSDM1_CKIN0, QUADSPI_CLK, EVENTOUT	BOOT1
-	-	-	-	-	M5	49	PF11	I/O	FT	-	TIM8_ETR, EVENTOUT	-
-	-	-	-	-	L5	50	PF12	I/O	FT	-	TIM8_BKIN, FSMC_A6, EVENTOUT	-
-	-	-	-	-	-	51	VSS	S	-	-	-	-
-	-	-	-	-	G5	52	VDD	S	-	-	-	-
-	-	-	-	-	K5	53	PF13	I/O	FT	-	I2CFMP1_SMBA, FSMC_A7, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	-	M6	54	PF14	I/O	FT	-	I2CFMP1_SCL, FSMC_A8, EVENTOUT	-
-	-	-	-	-	L6	55	PF15	I/O	FT	-	I2CFMP1_SDA, FSMC_A9, EVENTOUT	-
-	-	-	-	-	K6	56	PG0	I/O	FT	-	CAN1_RX, FSMC_A10, EVENTOUT	-
-	-	-	-	-	J6	57	PG1	I/O	FT	-	CAN1_TX, FSMC_A11, EVENTOUT	-
-	-	-	38	M7	M7	58	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, QUADSPI_BK2_IO0, FSMC_D4/FSMC_DA4, EVENTOUT	-
-	-	-	39	L7	L7	59	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, QUADSPI_BK2_IO1, FSMC_D5/FSMC_DA5, EVENTOUT	-
-	-	-	40	M8	K7	60	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, QUADSPI_BK2_IO2, FSMC_D6/FSMC_DA6, EVENTOUT	-
-	-	-	-	-	-	61	VSS	S	-	-	-	-
-	-	-	-	-	G6	62	VDD	S	-	-	-	-
-	-	-	41	L8	J7	63	PE10	I/O	FT	-	TIM1_CH2N, QUADSPI_BK2_IO3, FSMC_D7/FSMC_DA7, EVENTOUT	-
-	-	-	42	M9	H8	64	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, FSMC_D8/FSMC_DA8, EVENTOUT	-
-	-	-	43	L9	J8	65	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, FSMC_D9/FSMC_DA9, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	61	H11	K11	85	PD14	I/O	FT	-	TIM4_CH3, I2CFMP1_SCL, FSMC_D0/FSMC_DA0, EVENTOUT	-
-	-	-	62	H10	K12	86	PD15	I/O	FT	-	TIM4_CH4, I2CFMP1_SDA, FSMC_D1/FSMC_DA1, EVENTOUT	-
-	-	-	-	-	J12	87	PG2	I/O	FT	-	FSMC_A12, EVENTOUT	-
-	-	-	-	-	J11	88	PG3	I/O	FT	-	FSMC_A13, EVENTOUT	-
-	-	-	-	-	J10	89	PG4	I/O	FT	-	FSMC_A14, EVENTOUT	-
-	-	-	-	-	H12	90	PG5	I/O	FT	-	FSMC_A15, EVENTOUT	-
-	-	-	-	-	H11	91	PG6	I/O	FT	-	QUADSPI_BK1_NCS, EVENTOUT	-
-	-	-	-	-	H10	92	PG7	I/O	FT	-	USART6_CK, EVENTOUT	-
-	-	-	-	-	G11	93	PG8	I/O	FT	-	USART6_RTS, EVENTOUT	-
-	-	-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	-	-	F10	-	VDD	S	-			
-	-	-	-	-	C11	95	VDDUSB	S	-	-	-	-
-	37	F1	63	E12	G12	96	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2CFMP1_SCL, I2S2_MCK, DFSDM1_CKIN3, USART6_TX, FSMC_D1, SDIO_D6, EVENTOUT	-
-	38	E1	64	E11	F12	97	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2CFMP1_SDA, SPI2_SCK/I2S2_CK, I2S3_MCK, USART6_RX, DFSDM1_DATIN3, SDIO_D7, EVENTOUT	-
-	39	F3	65	E10	F11	98	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, USART6_CK, QUADSPI_BK1_IO2, SDIO_D0, EVENTOUT	-

Table 11. STM32F412xE/G register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB1	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	Reserved
	0x4000 6800- 0x4000 6BFF	CAN2
	0x4000 6400- 0x4000 67FF	CAN1
	0x4000 6000- 0x4000 63FF	I2CFMP1
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 4C00 - 0x4000 53FF	Reserved
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	Reserved
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

6.3 Operating conditions

6.3.1 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale3: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x01	0	-	64	MHz
		Power Scale2: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x10	0	-	84	
		Power Scale1: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x11	0	-	100	
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	50	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	-	100	MHz
V_{DD}	Standard operating voltage	-	1.7(1)	-	3.6	V
V_{DDA}(2)(3)	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}(4)	1.7(1)	-	2.4	V
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11 and PA12 pins)	USB not used	1.7	3.3	3.6	V
		USB used(5)	3.0	-	3.6	
V_{BAT}	Backup operating voltage	-	1.65	-	3.6	V
V_{12}	Regulator ON: 1.2 V internal voltage on VCAP_1/VCAP_2 pins	VOS[1:0] bits in PWR_CR register = 0x01 Max frequency 64 MHz	1.08(6)	1.14	1.20(6)	V
		VOS[1:0] bits in PWR_CR register = 0x10 Max frequency 84 MHz	1.20(6)	1.26	1.32(6)	
		VOS[1:0] bits in PWR_CR register = 0x11 Max frequency 100 MHz	1.26	1.32	1.38	
V_{12}	Regulator OFF: 1.2 V external voltage must be supplied on VCAP_1/VCAP_2 pins	Max frequency 64 MHz	1.10	1.14	1.20	V
		Max frequency 84 MHz	1.20	1.26	1.32	
		Max frequency 100 MHz	1.26	1.32	1.38	
V_{IN}	Input voltage on RST, FT and TC pins(7)	$2\ V \le V_{DD} \le 3.6\ V$	–0.3	-	5.5	V
		$V_{DD} \le 2\ V$	–0.3	-	5.2	
	Input voltage on BOOT0 pin	-	0	-	9	

Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)	100	36.3	38.95	41.19	42.95	mA
			84	31.1	33.22	34.81	36.10	
			64	22.3	23.97	25.10	26.23	
			50	18.3	19.77	20.65	21.73	
			25	10.1	11.39	12.16	13.11	
			20	8.6	9.60	10.25	11.06	
		HSI, PLL OFF, all peripherals enabled(3)	16	6.3	6.85	7.51	8.38	
			1	1.1	1.39	1.82	2.61	
		External clock, PLL ON(2) all peripherals disabled(3)	100	22.1	23.95	25.80	27.50	
			84	19.7	20.79	22.52	24.12	
			64	14.5	15.88	17.21	18.54	
			50	12.2	13.38	14.59	15.79	
			25	7.0	8.05	8.89	10.16	
			20	6.0	6.84	7.51	8.52	
		HSI, PLL OFF, all peripherals disabled(3)	16	4.4	4.91	5.56	6.54	
			1	0.9	1.25	1.79	2.59	

1. Based on characterization, not tested in production unless otherwise specified.
2. Refer to *Table 44* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 34. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions[1]	Typ				Max[2]		Unit
			T_A = 25 °C				T_A = 85 °C	T_A = 105 °C	
			V_{BAT} = 1.7 V	V_{BAT}= 2.4 V	V_{BAT} = 3.3 V	V_{BAT} = 3.6 V	V_{BAT} = 3.6 V		
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator (LSE in low-drive mode) and RTC ON	0.74	0.87	1.04	1.11	3.0	5.0	µA
		Low-speed oscillator (LSE in high-drive mode) and RTC ON	1.52	1.70	1.97	2.09	3.8	5.8	
		RTC and LSE OFF	0.04	0.04	0.05	0.05	2.0	4.0	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization, not tested in production.

Figure 24. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "low power" mode selection)

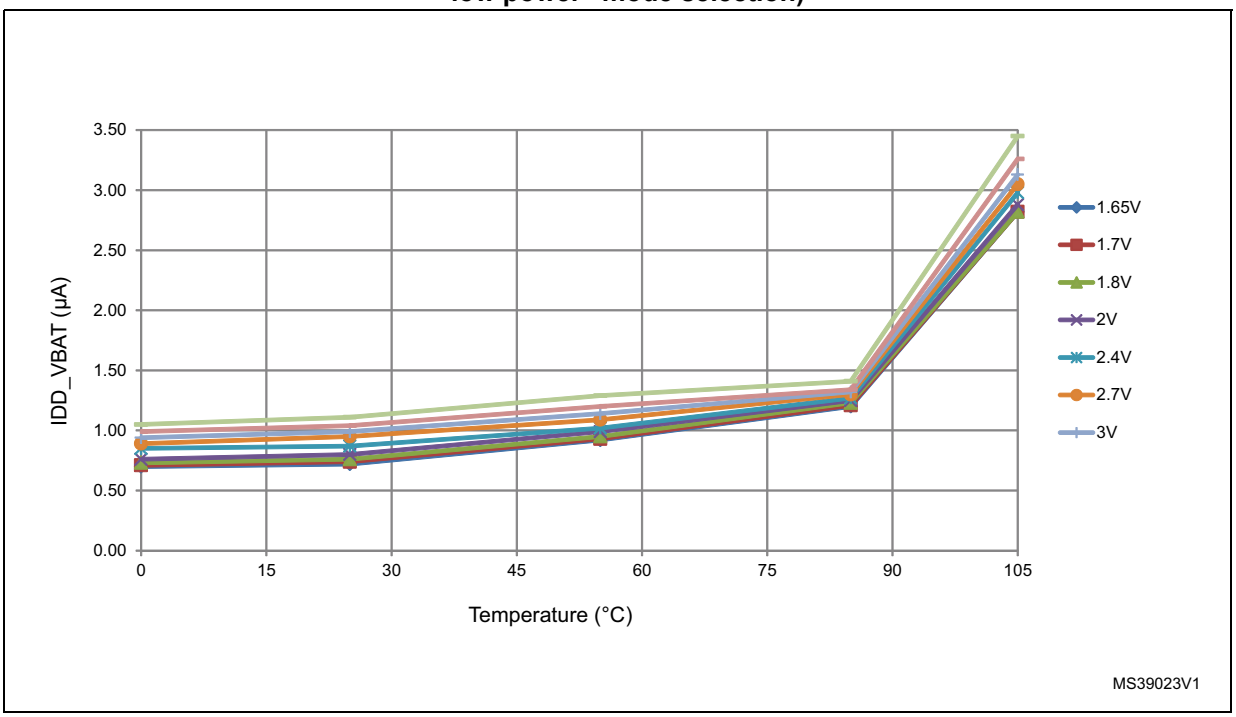


Table 35. Switching output I/O current consumption

Symbol	Parameter	Conditions(1)	I/O toggling frequency (f_{SW})	Typ	Unit
IDDIO	I/O switching current	V_{DD} = 3.3 V C = C_{INT}	2 MHz	0.05	mA
			8 MHz	0.15	
			25 MHz	0.45	
			50 MHz	0.85	
			60 MHz	1.00	
			84 MHz	1.40	
			90 MHz	1.67	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.10	
			8 MHz	0.35	
			25 MHz	1.05	
			50 MHz	2.20	
			60 MHz	2.40	
			84 MHz	3.55	
			90 MHz	4.23	
		V_{DD} = 3.3 V C_{EXT} =10 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.20	
			8 MHz	0.65	
			25 MHz	1.85	
			50 MHz	2.45	
			60 MHz	4.70	
			84 MHz	8.80	
			90 MHz	10.47	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.25	
			8 MHz	1.00	
			25 MHz	3.45	
			50 MHz	7.15	
			60 MHz	11.55	
		V_{DD} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.32	
			8 MHz	1.27	
			25 MHz	3.88	
			50 MHz	12.34	

1. CS is the PCB board capacitance including the pad pin. CS = 7 pF (estimated value).

6.3.9 Internal clock source characteristics

The parameters given in *Table 42* and *Table 43* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

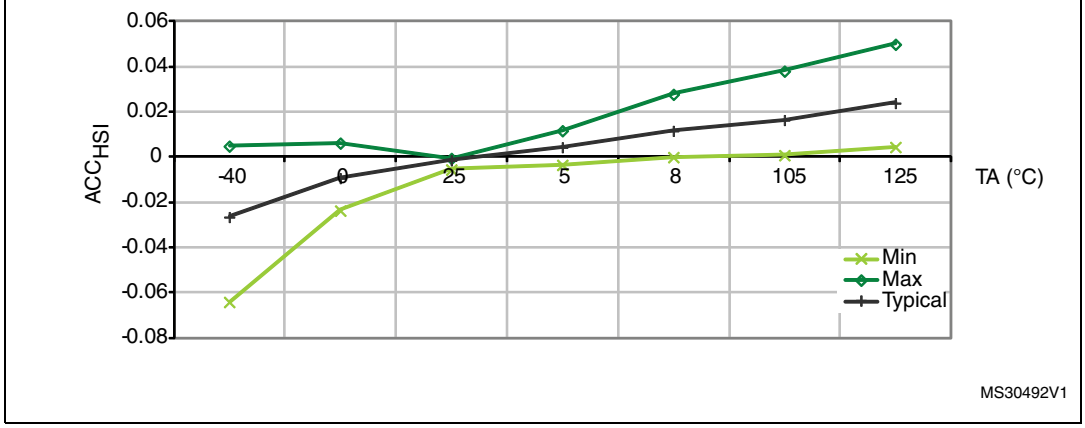
High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	–8	-	4.5	%
		T_A = –10 to 85 °C(3)	–4	-	4	%
		T_A = 25 °C(4)	–1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production
3. Based on characterization, not tested in production
4. Factory calibrated, parts not soldered.

Figure 31. ACC_{HSI} versus temperature



1. Guaranteed by characterization, not tested in production.

Table 49. Flash memory programming with V_{PP} voltage

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 50. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycle(2) at T_A = 55 °C	20	

1. Guaranteed by characterization, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

6.3.24 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 82* for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in *Table 15: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x VDD

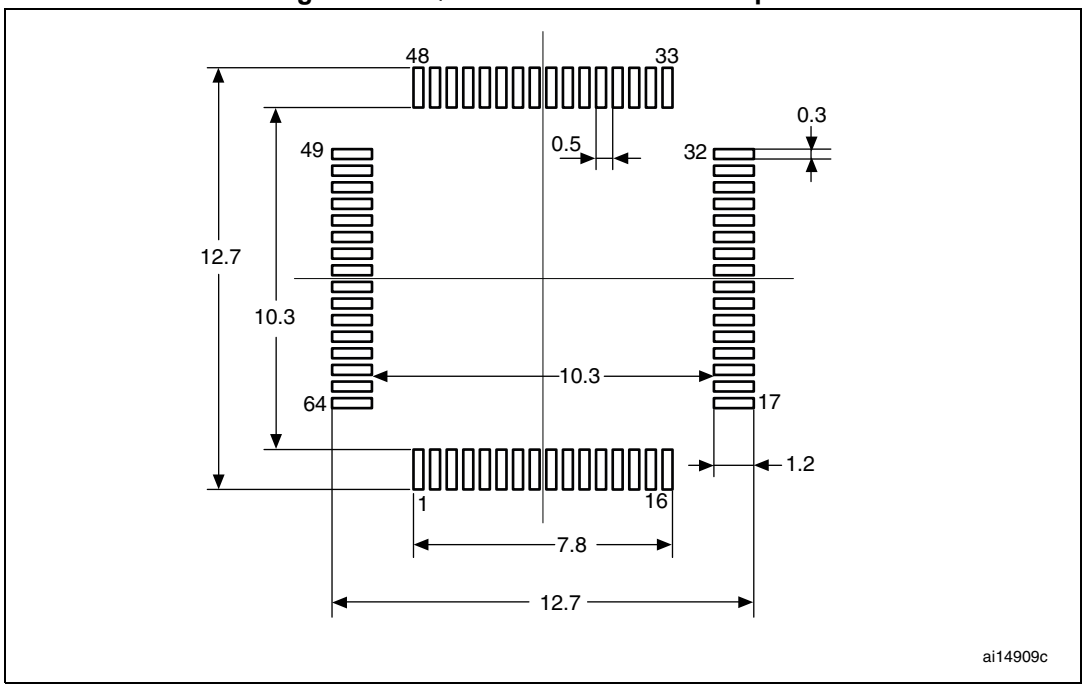
Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM_CKINy, DFSDM_DATINy, DFSDM_CKOUT for DFSDM).

Table 82. DFSDM characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	-	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0] = 01)	-	-	20 ($f_{DFSDMCLK}/4$)	
f_{CKOUT}	Output clock frequency	-	-	-	20	MHz
$DuCy_{CKOUT}$	Output clock frequency duty cycle	-	30	50	75	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0)	$T_{CKIN}/2-0.5$	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	1	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	1	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0)	(CKOUT DIV+1) x $T_{DFSDMCLK}$	-	(2 x CKOUTDIV) x $T_{DFSDMCLK}$	

1. Data based on characterization results, not tested in production.

Figure 67. LQFP64 recommended footprint

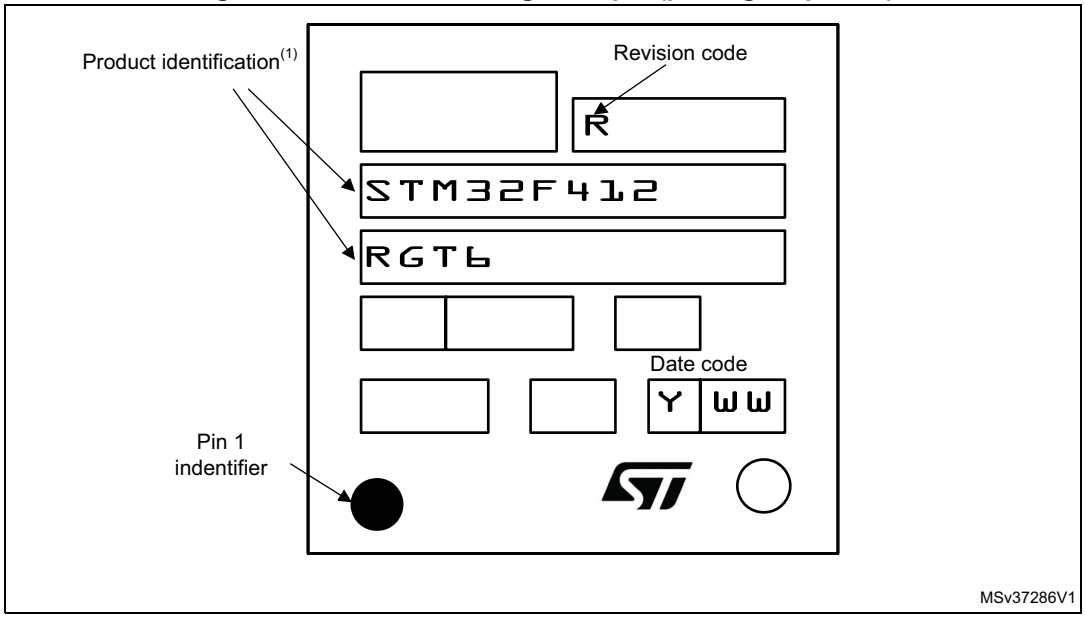


1. Dimensions are in millimeters.

Device marking for LQFP64

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 68. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 103. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

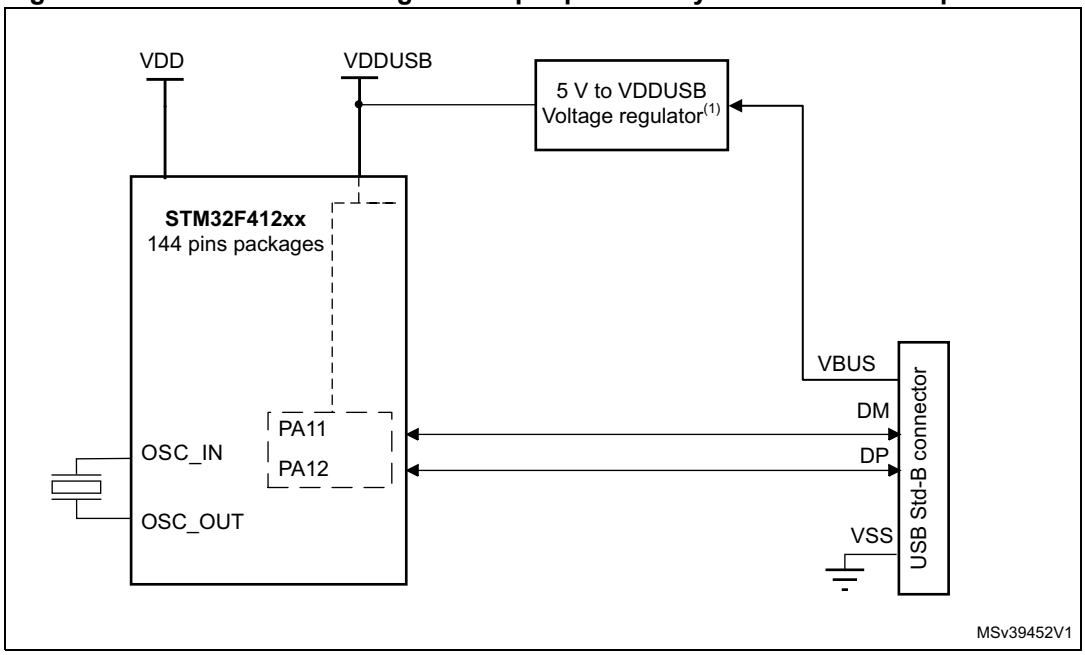
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Appendix B Application block diagrams

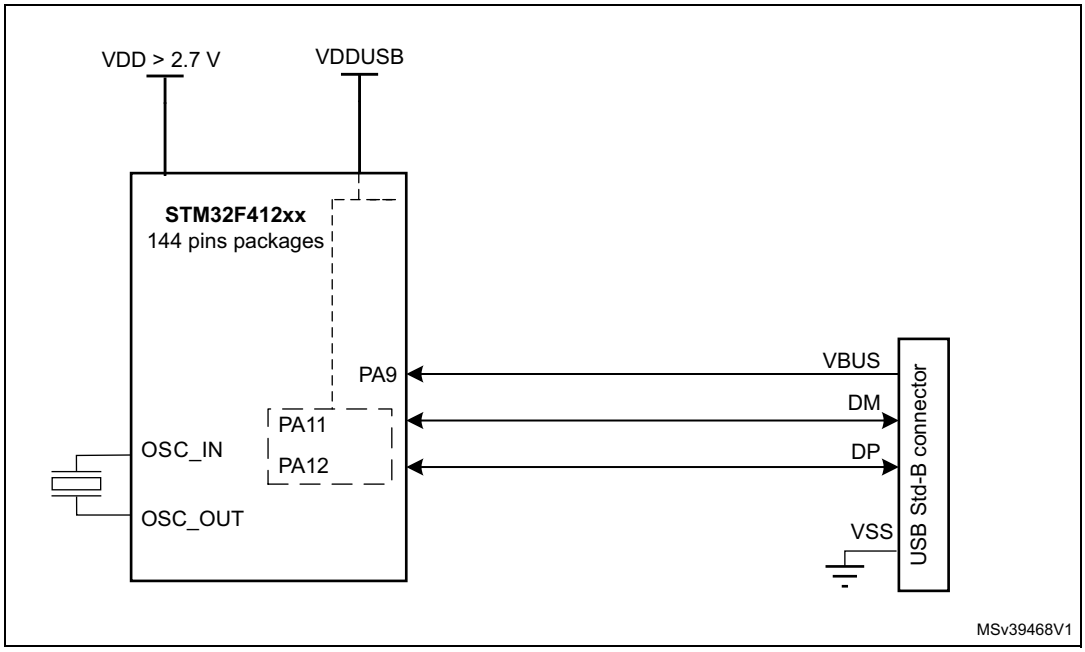
B.1 USB OTG full speed (FS) interface solutions

Figure 81. USB controller configured as peripheral-only and used in Full speed mode



1. External voltage regulator only needed when building a V_{BUS} powered device.

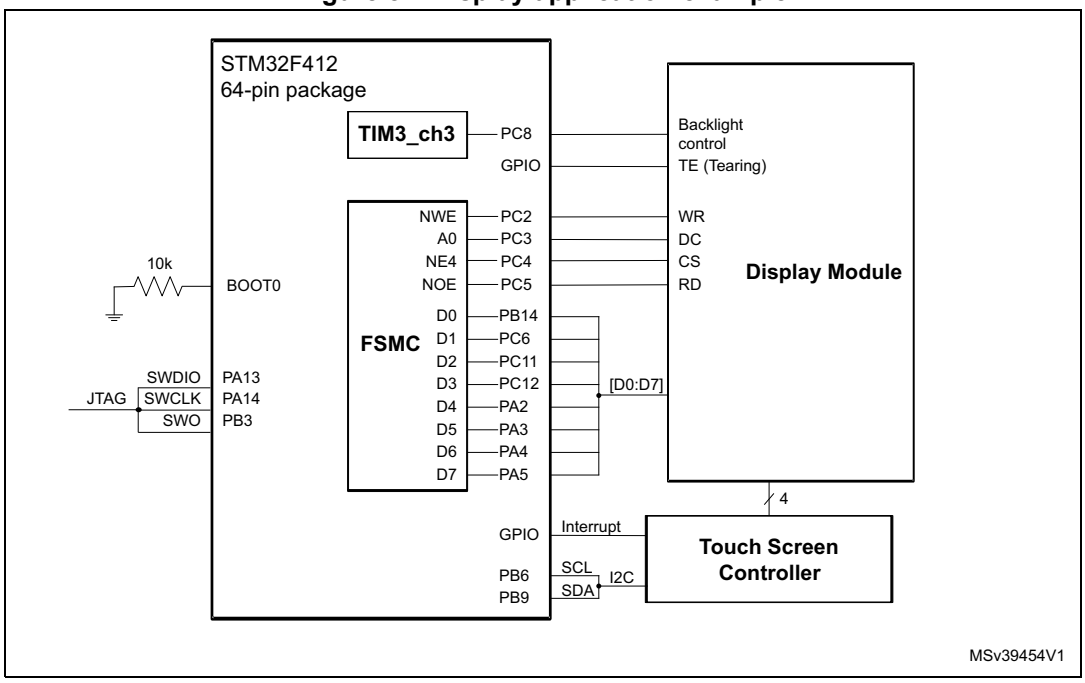
Figure 82. USB peripheral-only Full speed mode with direct connection for VBUS sense



1. External voltage regulator only needed when building a V_{BUS} powered device.

B.3 Display application example

Figure 87. Display application example



Note: 16 bit displays interfaces can be addressed with 100 and 144 pins packages.

Revision history

Table 110. Document revision history

Date	Revision	Changes
10-Nov-2015	1	Initial release.
01-Feb-2016	2	Added – *Table 3: Embedded bootloader interfaces* – *Figure 3: Compatible board design for LQFP144 package* – *Figure 62: WLCSP64 marking example (package top view)* – *Figure 77: UFBGA100 marking example (package top view)* Updated – *Section 3.17: Power supply schemes* – *Section 3.23: Timers and watchdogs* – *Section 3.32: Universal serial bus on-the-go full-speed (USB_OTG_FS)* – *Figure 1: Compatible board design for LQFP100 package* – *Figure 2: Compatible board design for LQFP64 package* – *Figure 14: STM32F412xE/G LQFP100 pinout* – *Figure 16: STM32F412xE/G UFBGA100 pinout* – *Figure 17: STM32F412xE/G UFBGA144 pinout* – *Figure 20: Input voltage measurement* – *Figure 80: UFBGA144 marking example (package top view)* – *Table 2: STM32F412xE/G features and peripheral counts* – *Table 9: STM32F412xE/G pin definition* – *Table 12: Voltage characteristics* – *Table 13: Current characteristics* – *Table 15: General operating conditions* – *Table 36: Peripheral current consumption* – *Table 51: EMS characteristics for LQFP144 package* – *Table 63: FMPI2C characteristics*