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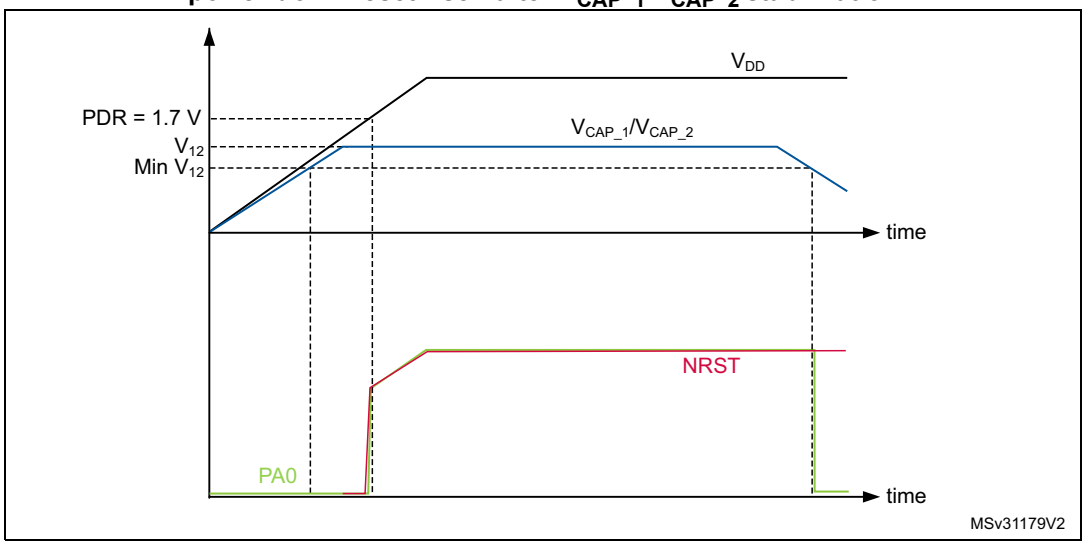
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

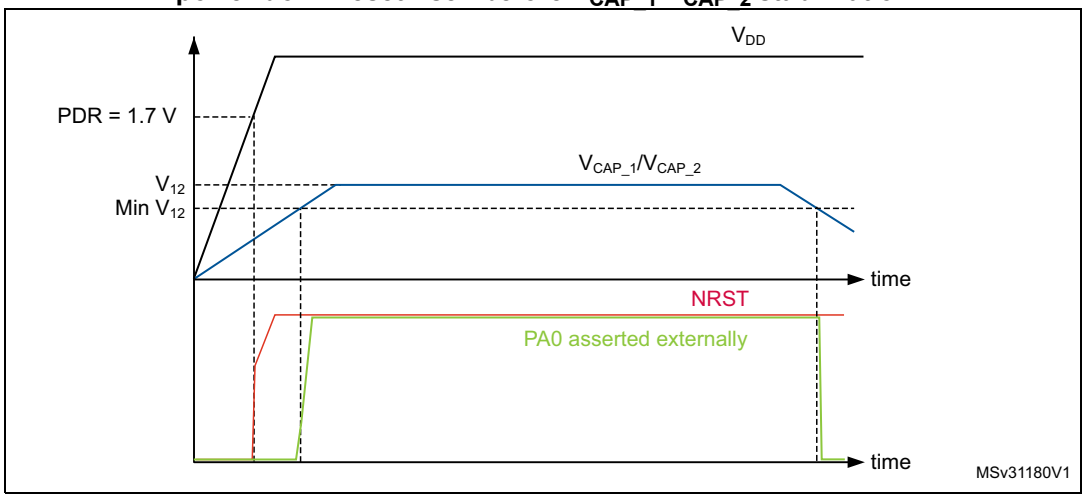
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412vet6tr

Figure 9. Startup in regulator OFF: slow V_{DD} slope power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 10. Startup in regulator OFF mode: fast V_{DD} slope power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

3.19.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal power supply supervisor availability

Package	Regulator ON	Regulator OFF	Power supply supervisor ON	Power supply supervisor OFF
UFQFPN48	Yes	No	Yes	No
WLCSP64	Yes	No	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP64	Yes	No	Yes	No
LQFP100	Yes	No	Yes	No
LQFP144	Yes	No	Yes PDR_ON set to VDD	Yes PDR_ON set to V_{SS}
UFBGA100	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD		
UFBGA144	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD		

3.20 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 byte of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.21: Low-power modes*).

3.33 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.34 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

3.35 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

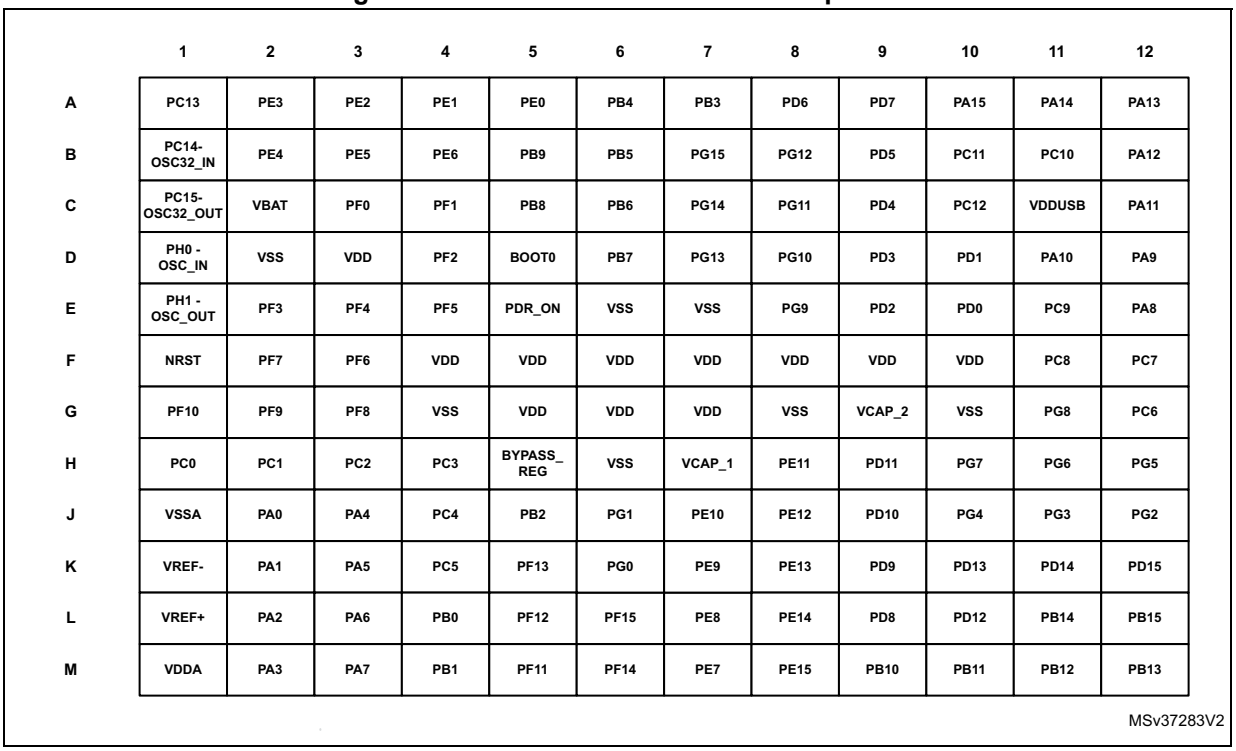
As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 17. STM32F412xE/G UFBGA144 pinout



	1	2	3	4	5	6	7	8	9	10	11	12
A	PC13	PE3	PE2	PE1	PE0	PB4	PB3	PD6	PD7	PA15	PA14	PA13
B	PC14-OSC32_IN	PE4	PE5	PE6	PB9	PB5	PG15	PG12	PD5	PC11	PC10	PA12
C	PC15-OSC32_OUT	VBAT	PF0	PF1	PB8	PB6	PG14	PG11	PD4	PC12	VDDUSB	PA11
D	PH0 - OSC_IN	VSS	VDD	PF2	BOOT0	PB7	PG13	PG10	PD3	PD1	PA10	PA9
E	PH1 - OSC_OUT	PF3	PF4	PF5	PDR_ON	VSS	VSS	PG9	PD2	PD0	PC9	PA8
F	NRST	PF7	PF6	VDD	VDD	VDD	VDD	VDD	VDD	VDD	PC8	PC7
G	PF10	PF9	PF8	VSS	VDD	VDD	VDD	VSS	VCAP_2	VSS	PG8	PC6
H	PC0	PC1	PC2	PC3	BYPASS_REG	VSS	VCAP_1	PE11	PD11	PG7	PG6	PG5
J	VSSA	PA0	PA4	PC4	PB2	PG1	PE10	PE12	PD10	PG4	PG3	PG2
K	VREF-	PA1	PA5	PC5	PF13	PG0	PE9	PE13	PD9	PD13	PD14	PD15
L	VREF+	PA2	PA6	PB0	PF12	PF15	PE8	PE14	PD8	PD12	PB14	PB15
M	VDDA	PA3	PA7	PB1	PF11	PF14	PE7	PE15	PB10	PB11	PB12	PB13

MSv37283V2

1. The above figure shows the package top view.

Table 8. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/ output pin
I/O structure	FT	5 V tolerant I/O
	TC	Standard 3.3 V I/O
	B	Dedicated BOOT0 pin
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)	100	36.3	38.95	41.19	42.95	mA
			84	31.1	33.22	34.81	36.10	
			64	22.3	23.97	25.10	26.23	
			50	18.3	19.77	20.65	21.73	
			25	10.1	11.39	12.16	13.11	
			20	8.6	9.60	10.25	11.06	
		HSI, PLL OFF, all peripherals enabled(3)	16	6.3	6.85	7.51	8.38	
			1	1.1	1.39	1.82	2.61	
		External clock, PLL ON(2) all peripherals disabled(3)	100	22.1	23.95	25.80	27.50	
			84	19.7	20.79	22.52	24.12	
			64	14.5	15.88	17.21	18.54	
			50	12.2	13.38	14.59	15.79	
			25	7.0	8.05	8.89	10.16	
			20	6.0	6.84	7.51	8.52	
		HSI, PLL OFF, all peripherals disabled(3)	16	4.4	4.91	5.56	6.54	
			1	0.9	1.25	1.79	2.59	

1. Based on characterization, not tested in production unless otherwise specified.
2. Refer to *Table 44* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. Tested in production.

Table 29. Typical and maximum current consumption in Sleep mode - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Sleep mode**	External clock, PLL ON, Flash deep power down, all peripherals enabled(2)	100	17.3	18.62	19.90	21.40	mA
			84	14.0	15.08	16.04	17.16	
			64	9.7	10.41	11.02	11.80	
			50	7.6	8.27	8.89	9.62	
			25	4.2	4.79	5.35	6.00	
			20	3.7	4.11	4.67	5.31	
		HSI, PLL OFF(2), Flash deep power down, all peripherals enabled	16	2.4	2.81	3.45	4.20	
			1	0.5	0.67	1.27	1.91	
		External clock, PLL ON(2) all peripherals enabled, Flash ON	100	17.8	19.08	20.35	21.90	
			84	14.4	15.49	16.42	17.59	
			64	10.0	10.76	11.43	12.18	
			50	7.9	8.58	9.19	9.94	
			25	4.4	4.99	5.54	6.21	
			20	4.0	4.42	4.95	5.64	
		HSI, PLL OFF(2), all peripherals enabled, Flash ON	16	2.7	3.09	3.75	4.49	
			1	0.8	0.93	1.52	2.18	

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off,
  - with only one peripheral clocked on,
  - scale 1 with f_{HCLK} = 100 MHz,
  - scale 2 with f_{HCLK} = 84 MHz,
  - scale 3 with f_{HCLK} = 64 MHz.
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 36. Peripheral current consumption

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
AHB1	GPIOA	1.84	1.75	1.55	µA/MHz
	GPIOB	1.90	1.80	1.61	
	GPIOC	1.77	1.67	1.50	
	GPIOD	1.67	1.58	1.42	
	GPIOE	1.75	1.67	1.48	
	GPIOF	1.65	1.56	1.39	
	GPIOG	1.65	1.56	1.39	
	GPIOH	0.62	0.57	0.53	
	CRC	0.26	0.25	0.22	
	DMA1(1)	1,71N+2,98	1,62N+2,87	1,45N+2,58	
	DMA2(1)	1,78N+2,62	1,70N+2.53	1,52N+2.26	
AHB2	RNG	0.77	0.74	0.66	
	USB_OTG_FS	19.68	18.73	16.78	
AHB3	FSMC	5.36	5.11	4.56	
	QSPI	9.99	9.51	8.53	

Table 37. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
t_{WUSTOP}	Wakeup from STOP mode Code execution on Flash	Main regulator	-	12.9	15.0	µs
		Main regulator, Flash memory in Deep power down mode	-	104.9	120.0	
		Wakeup from Stop mode, regulator in low power mode(2)	-	20.8	28.0	
		Regulator in low power mode, Flash memory in Deep power down mode(2)	-	112.9	130.0	
t_{WUSTOP}	Wakeup from STOP mode code execution on RAM(3)	Main regulator with Flash in Stop mode or Deep power down	-	4.9	7.0	
		Wakeup from Stop mode, regulator in low power mode and Flash in Stop mode or Deep power down(2)	-	12.8	20.0	
$t_{WUSTDBY}$	Wakeup from Standby mode	-	-	316.8	400.0	
$t_{WUFLASH}$	Wakeup of Flash	From Flash_Stop mode	-		11.0	
		From Flash Deep power down mode	-		50.0	

1. Guaranteed by characterization, not tested in production.
2. The specification is valid for wakeup from regulator in low power mode or low power low voltage mode, since the timing difference is negligible.
3. For the faster wakeup time for code execution on RAM, the Flash must be in STOP or DeepPower Down mode (see reference manual RM0402).

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 56*. However, the recommended clock input waveform is shown in *Figure 27*.

The characteristics given in *Table 38* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 15*.

6.3.9 Internal clock source characteristics

The parameters given in *Table 42* and *Table 43* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

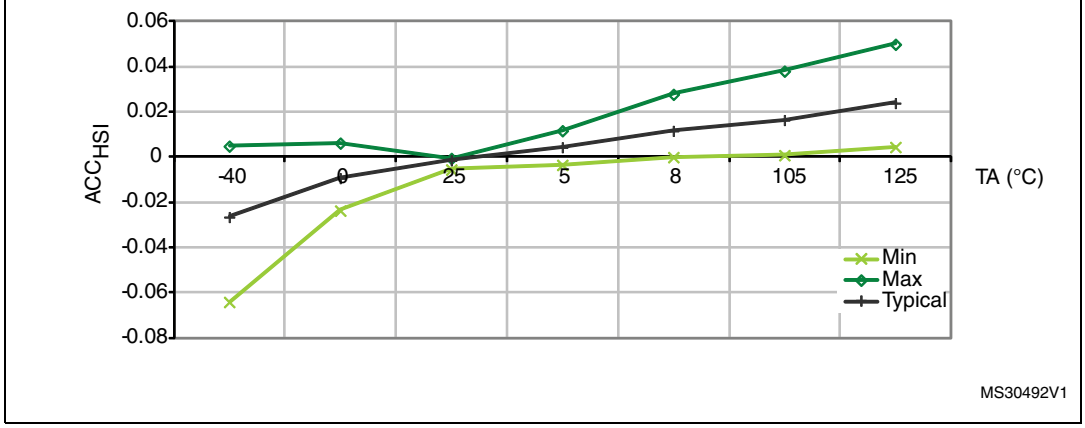
High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	–8	-	4.5	%
		T_A = –10 to 85 °C(3)	–4	-	4	%
		T_A = 25 °C(4)	–1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production
3. Based on characterization, not tested in production
4. Factory calibrated, parts not soldered.

Figure 31. ACC_{HSI} versus temperature



1. Guaranteed by characterization, not tested in production.

Table 49. Flash memory programming with V_{PP} voltage

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 50. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycle(2) at T_A = 55 °C	20	

1. Guaranteed by characterization, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 52. EMI characteristics for LQFP144

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/100 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP144 package, conforming to IEC 61967-2, EEMBC, ART ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	20	dBµV
			30 to 130 MHz	28	
			130 MHz to 1 GHz	21	
			EMI Level	3.5	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 53. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1, UFBGA144, UFBGA100, LQFP100, LQFP64, UFQFPN48	4	500	
		T_A = +25 °C conforming to ANSI/ESD STM5.3.1, WLCSP64	3	400	
		T_A = +25 °C conforming to ANSI/ESD STM5.3.1, LQFP144	3	250	

1. Guaranteed by characterization, not tested in production.

Table 64. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{a(SO)}$	Data output access time	Slave mode	7	-	21	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	5	-	12	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge), 2.7 V < V_{DD} < 3.6 V	-	7.5	9	ns
		Slave mode (after enable edge), 1.7 V < V_{DD} < 3.6 V	-	7.5	14	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge), 1.7 V < V_{DD} < 3.6 V	5.5	-	-	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	3	8	ns
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	2	-	-	ns

1. Guaranteed by characterization, not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

Figure 40. SPI timing diagram - slave mode and CPHA = 0

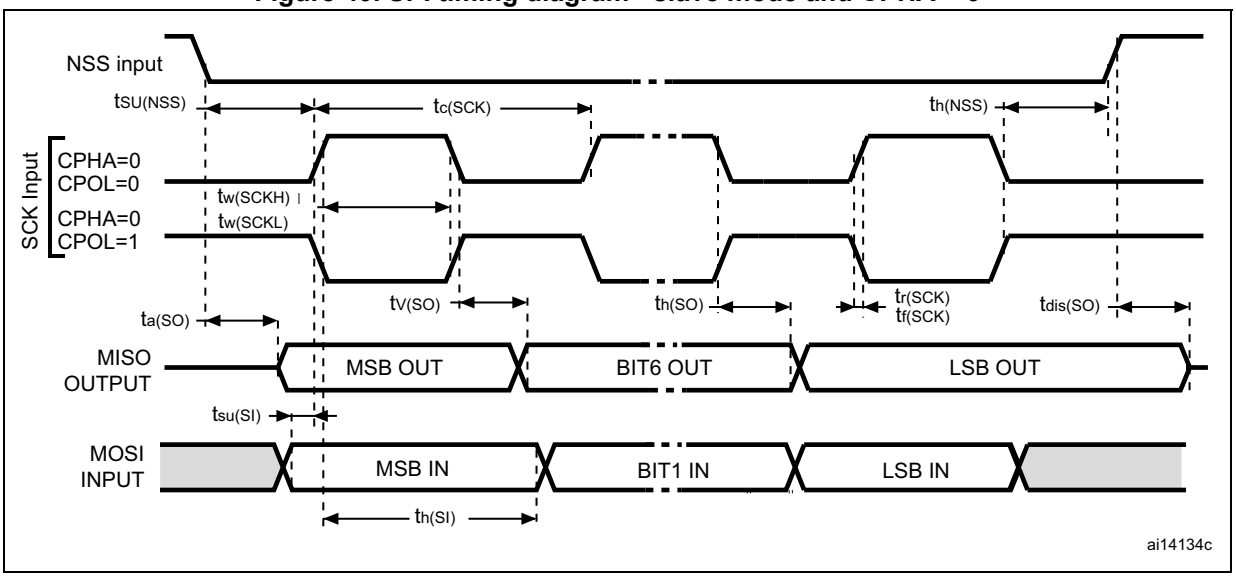


Table 89. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$4T_{HCLK}$ - 1	$4T_{HCLK}$+0.5	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	T_{HCLK}	T_{HCLK} + 1	
$t_{w(NWE)}$	FSMC_NWE low time	$2T_{HCLK}$ - 1	$2T_{HCLK}$ + 0.5	
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK} - 1.5	-	
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	2	
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	0	1	
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK} – 0.5	T_{HCLK}+ 0.5	
$t_{h(AD\_NADV)}$	FSMC_AD(adress) valid hold time after FSMC_NADV high)	T_{HCLK}	-	
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK}- 1.5	-	
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	T_{HCLK}	-	
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	T_{HCLK} + 2	
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK} + 0.5	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Table 90. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$9T_{HCLK}$ - 1	$9T_{HCLK}$ + 0.5	ns
$t_{w(NWE)}$	FSMC_NWE low time	$7T_{HCLK}$ - 1	$7T_{HCLK}$ + 0.5	
$t_{su(NWAIT\_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$6T_{HCLK}$ -1	-	
$t_{h(NE\_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4T_{HCLK}$ + 1	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Synchronous waveforms and timings

Figure 54 through *Figure 57* represent synchronous waveforms and *Table 91* through *Table 94* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F446 reference manual: RM0390)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Table 91. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH\_NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	T_{HCLK}	-	
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	1	-	
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	2	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Table 95. Dynamic characteristics: SD / MMC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	fpp =25MHz	2.5	-	-	ns
t_{IHD}	Input hold time SD	fpp =25MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	fpp =25 MHz	-	1.5	2	ns
t_{OHD}	Output hold default time SD	fpp =25 MHz	0.5	-	-	

1. Guaranteed by characterization results, not tested in production.
2. V_{DD} = 2.7 to 3.6 V.

Table 96. Dynamic characteristics: eMMC characteristics V_{DD} = 1.7 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	fpp =50MHz	3.5	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	4	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	13.5	15	ns
t_{OH}	Output hold time HS	fpp =50MHz	12	-	-	

1. Guaranteed by characterization results, not tested in production.
2. C_{LOAD} = 20 pF.

6.3.27 RTC characteristics

Table 97. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

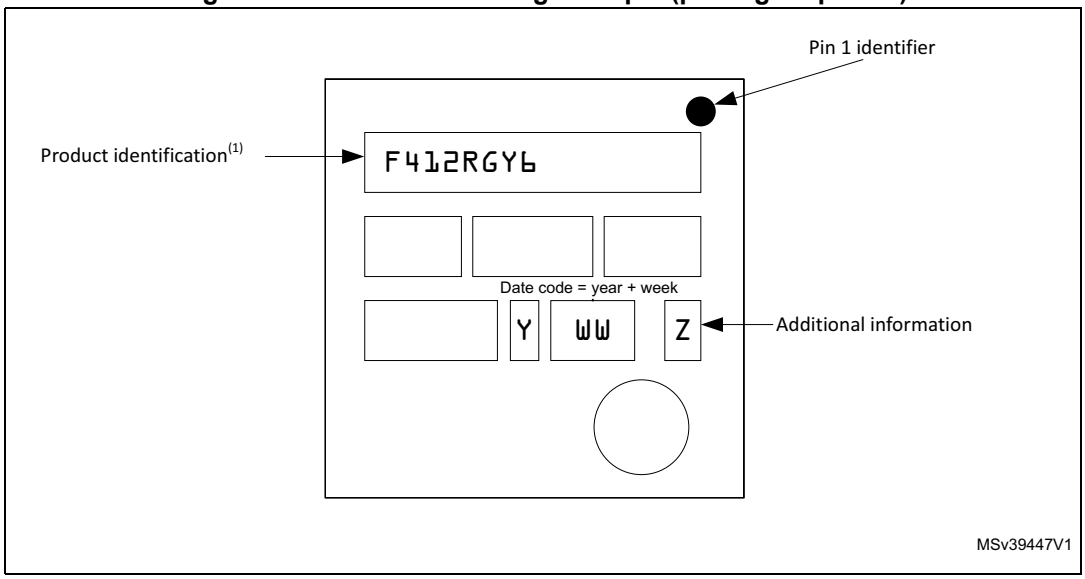
Table 99. WLCSP64 recommended PCB design rules (0.4 mm pitch) (continued)

Dimension	Recommended values
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking for WLCSP64

The following figure gives an example of topside marking and pin 1 position identifier location.

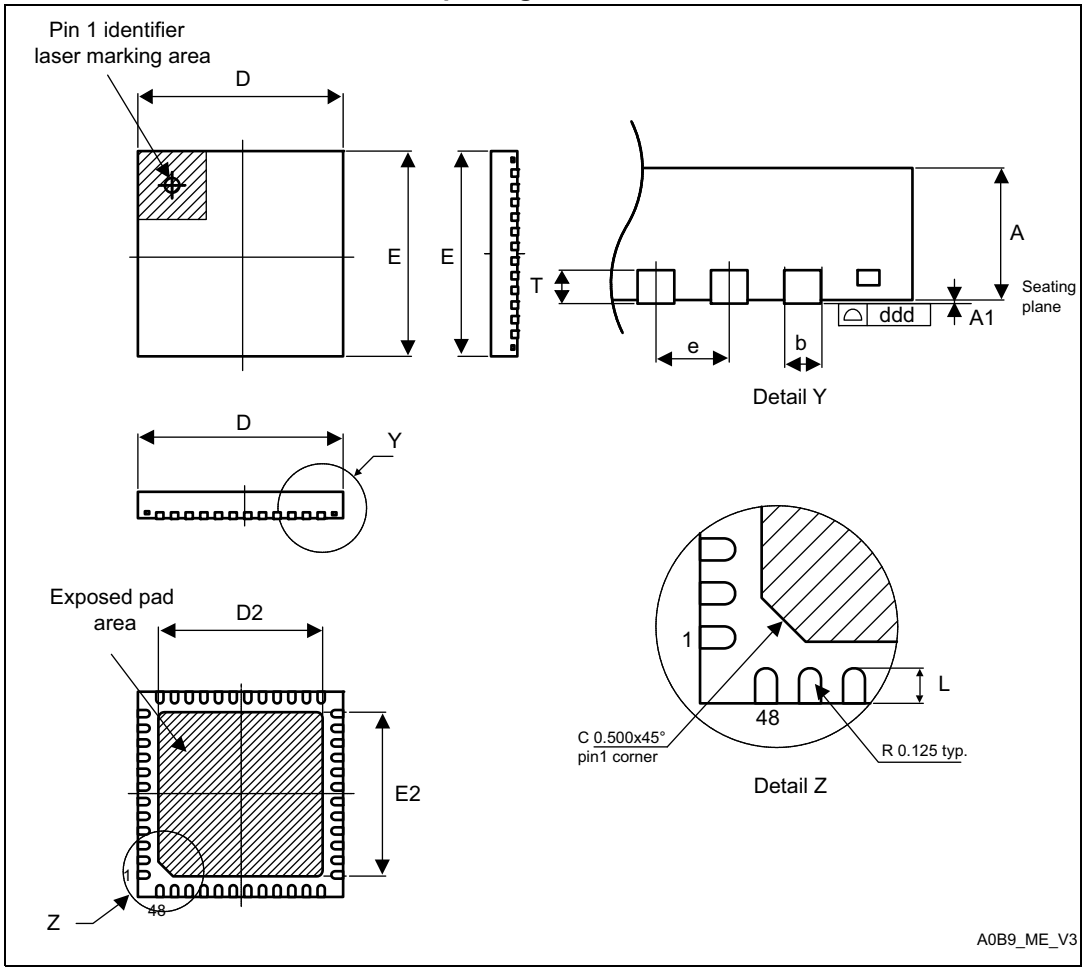
Figure 62. WLCSP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.2 UFQFPN48 package information

Figure 63. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 100. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244

8 Part numbering

Table 109. Ordering information scheme

Example: STM32 F 412 C E T 6 TR

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = General-purpose

Device subfamily

412 = 412 line

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Z = 144 pins

Flash memory size

E = 512 Kbytes of Flash memory

G = 1024 Kbytes of Flash memory

Package

H = UFBGA 7 x 7 mm

J = UFBGA 10 x 10 mm

T = LQFP

U = UFQFPN

Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C

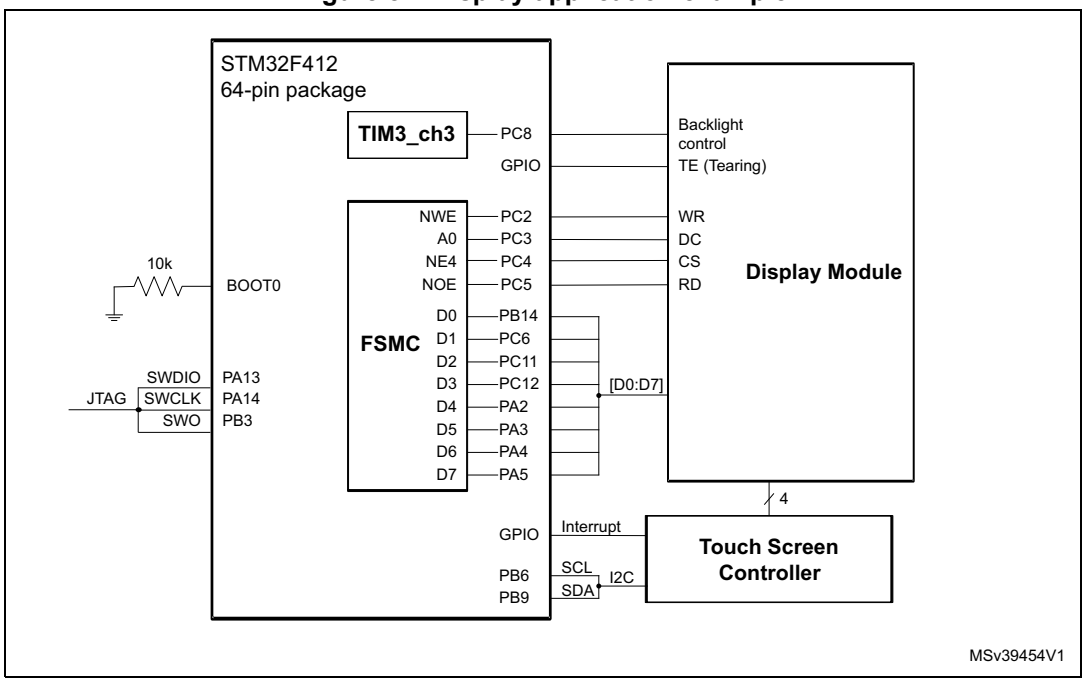
Packing

TR = tape and reel

No character = tray or tube

B.3 Display application example

Figure 87. Display application example



Note: 16 bit displays interfaces can be addressed with 100 and 144 pins packages.

Table 110. Document revision history

Date	Revision	Changes
25-Mar-2016	3	Added: – *Figure 82: USB peripheral-only Full speed mode with direct connection for VBUS sense* – *Figure 83: USB peripheral-only Full speed mode, VBUS detection using GPIO* Updated: – *Figure 15: STM32F412xE/G LQFP144 pinout* – *Section 6.3.6: Supply current characteristics* – *Table 9: STM32F412xE/G pin definition* – *Table 10: STM32F412xE/G alternate functions* – *Table 11: STM32F412xE/G register boundary addresses* – *Table 15: General operating conditions* – *Table 36: Peripheral current consumption* – *Table 96: Dynamic characteristics: eMMC characteristics VDD = 1.7 V to 1.9 V*
27-May-2016	4	Updated: – *Section 3.23.2: General-purpose timers (TIMx)* – *Table 21: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - VDD = 1.7 V* – *Table 22: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - VDD = 3.6 V* – *Table 23: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- VDD = 1.7 V* – *Table 24: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - VDD = 3.6 V* – *Table 25: Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - VDD = 3.6 V* – *Table 26: Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - VDD = 1.7 V* – *Table 27: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - VDD = 3.6 V* – *Table 28: Typical and maximum current consumption in Sleep mode - VDD = 3.6 V* – *Table 29: Typical and maximum current consumption in Sleep mode - VDD = 1.7 V* – *Table 37: Low-power mode wakeup timings(1)* – *Figure 38: I2C bus AC waveforms and measurement circuit* – *Figure 39: FMPI2C timing diagram and measurement circuit*