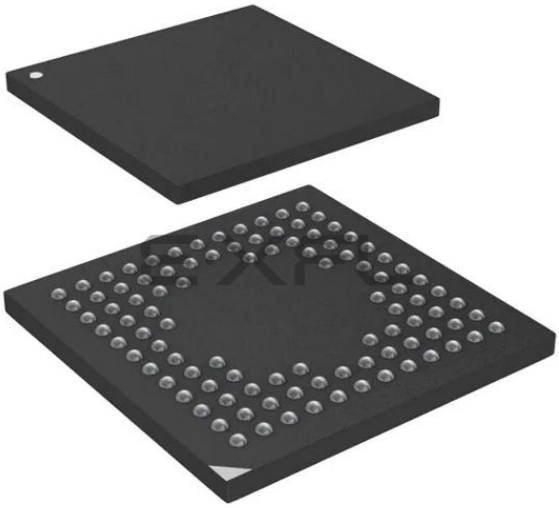


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412vgh6

These features make the STM32F412xE/G microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub
- Wearable devices
- Connected objects
- Wifi modules

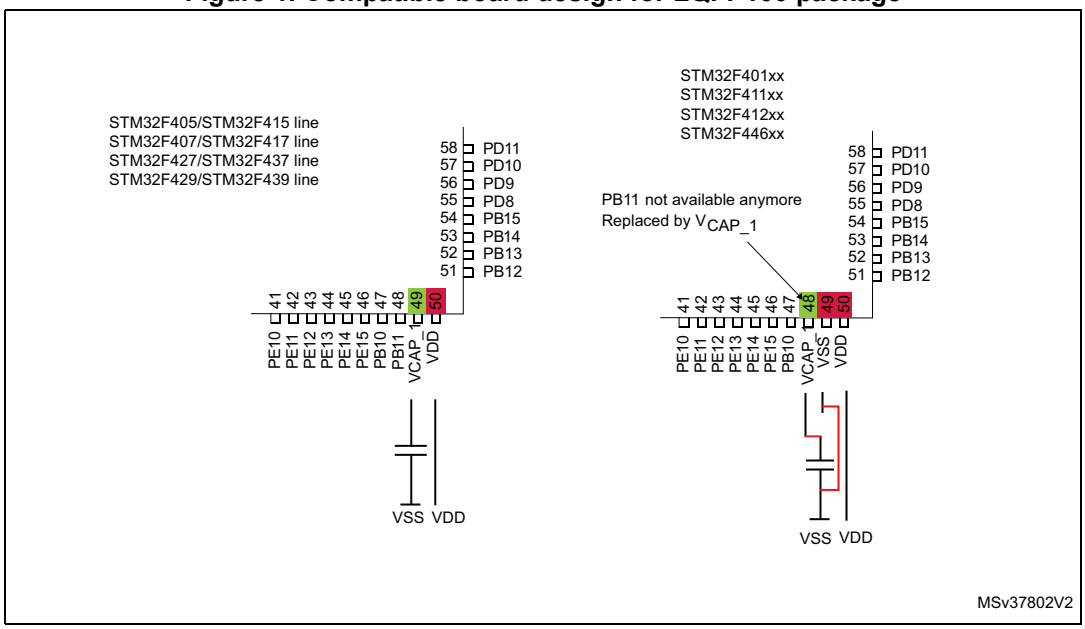
Figure 4 shows the general block diagram of the devices.

2.1 Compatibility with STM32F4 series

The STM32F412xE/G are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F412xE/G can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

Figure 1. Compatible board design for LQFP100 package



3.13 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 81 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.14 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 21 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

3.15 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 100 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses and high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

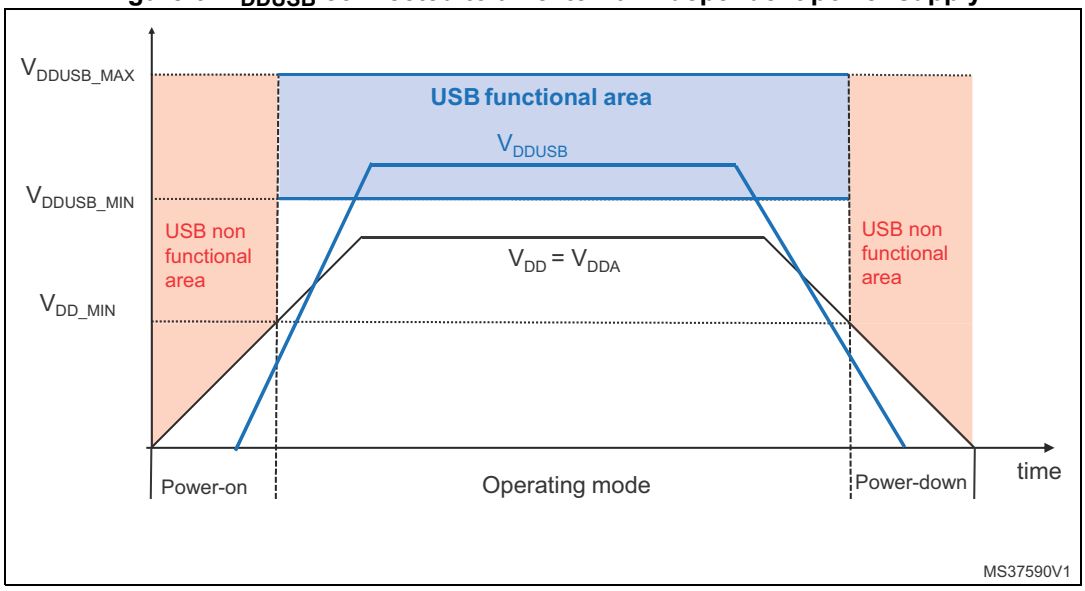
The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear.

The following conditions VDDUSB must be respected:

- During power-on phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- During power-down phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- V_{DDUSB} rising and falling time rate specifications must be respected.
- In operating mode phase, V_{DDUSB} could be lower or higher than VDD:
  - If USB is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX}.
  - If USB is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX}.

Figure 6. V_{DDUSB} connected to an external independent power supply



3.33 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.34 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

3.35 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

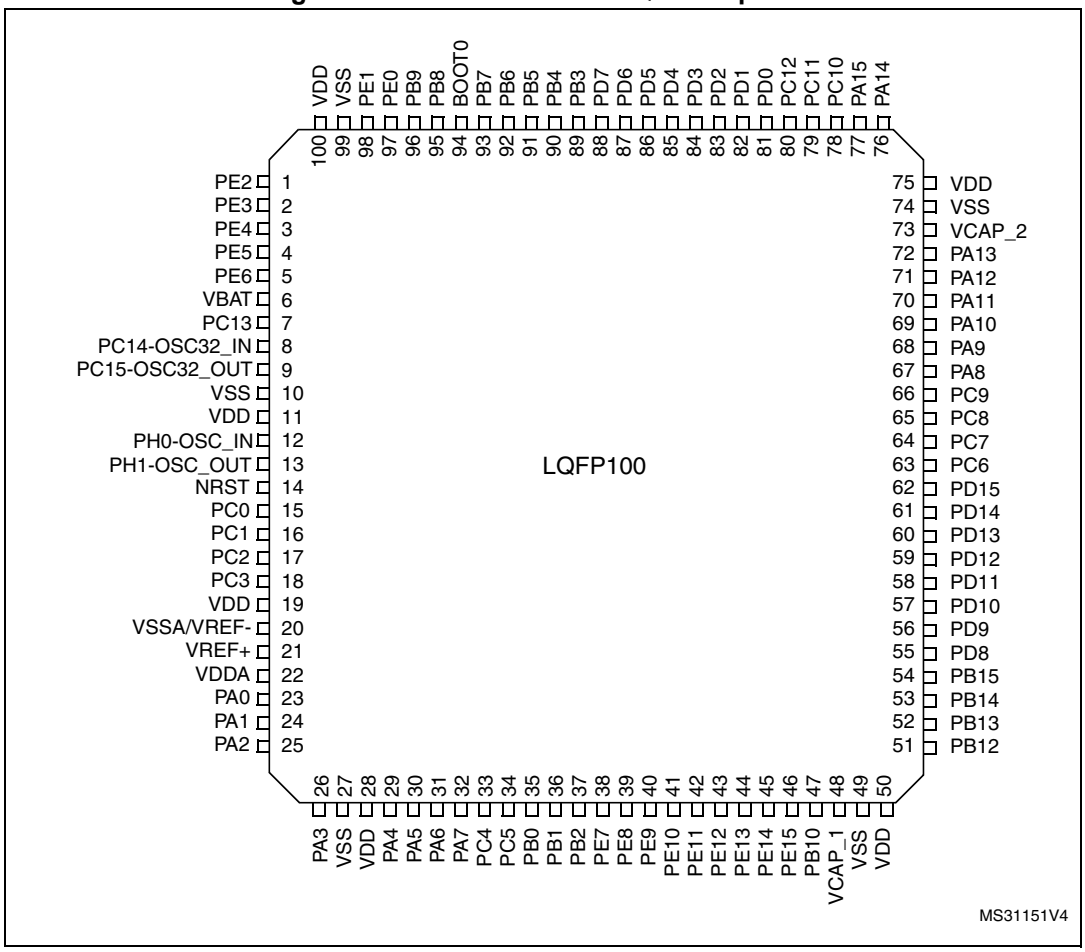
As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 14. STM32F412xE/G LQFP100 pinout



1. The above figure shows the package top view.

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
27	35	G1	53	K11	L11	75	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, I2CFMP1_SDA, SPI2_MISO, I2S2ext_SD, USART3_RTS, DFSDM1_DATIN2, TIM12_CH1, FSMC_D0, SDIO_D6, EVENTOUT	-
28	36	F2	54	K10	L12	76	PB15	I/O	FT	-	RTC_50Hz, TIM1_CH3N, TIM8_CH3N, I2CFMP1_SCL, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, TIM12_CH2, SDIO_CK, EVENTOUT	-
-	-	-	55	-	L9	77	PD8	I/O	FT	-	USART3_TX, FSMC_D13/ FSMC_DA13, EVENTOUT	-
-	-	-	56	K8	K9	78	PD9	I/O	FT	-	USART3_RX, FSMC_D14/FSMC_DA14, EVENTOUT	-
-	-	-	57	J12	J9	79	PD10	I/O	FT	-	USART3_CK, FSMC_D15/FSMC_DA15, EVENTOUT	-
-	-	-	58	J11	H9	80	PD11	I/O	FT	-	I2CFMP1_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FSMC_A16, EVENTOUT	-
-	-	-	59	J10	L10	81	PD12	I/O	FT	-	TIM4_CH1, I2CFMP1_SCL, USART3_RTS, QUADSPI_BK1_IO1, FSMC_A17, EVENTOUT	-
-	-	-	60	H12	K10	82	PD13	I/O	FT	-	TIM4_CH2, I2CFMP1_SDA, QUADSPI_BK1_IO3, FSMC_A18, EVENTOUT	-
-	-	-	-	-	G8	83	VSS	S	-	-	-	-
-	-	-	-	-	F8	84	VDD	S	-	-	-	-

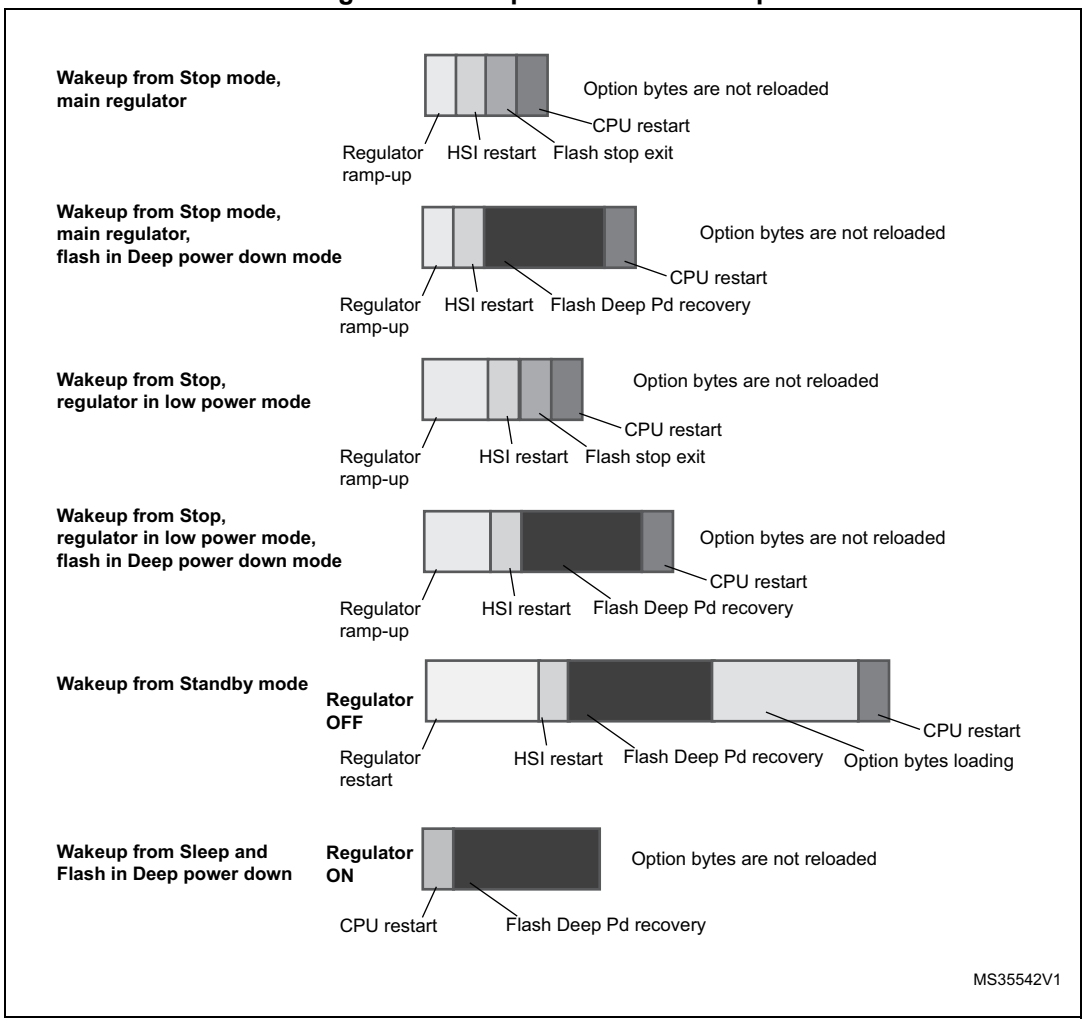
Table 10. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port C	PC0	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	I2S2ext_SD	-	DFSDM1_ CKOUT	-	-	FSMC_NWE	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI/I 2S2_SD	-	-	-	-	-	FSMC_A0	EVENTOUT
	PC4	-	-	-	-	-	I2S1_MCK	-	-	-	-	QUADSPI_ BK2_IO2	FSMC_NE4	EVENTOUT
	PC5	-	-	-	-	I2CFMP1_ SMBA	-	-	USART3_RX	-	-	QUADSPI_ BK2_IO3	FSMC_NOE	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	I2CFMP1_ SCL	I2S2_MCK	DFSDM1_ CKIN3	-	USART6_ TX	-	FSMC_D1	SDIO_D6	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	I2CFMP1_ SDA	SPI2_SCK/ I2S2_CK	I2S3_MCK	-	USART6_ RX	-	DFSDM1_ DATIN3	SDIO_D7	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_ CK	QUADSPI_ BK1_IO2	-	SDIO_D0	EVENTOUT
	PC9	MCO_2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	-	-	-	QUADSPI_ BK1_IO0	-	SDIO_D1	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK/ I2S3_CK	USART3_TX	-	QUADSPI_ BK1_IO1	-	SDIO_D2	EVENTOUT
	PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO	USART3_RX	-	QUADSPI_ BK2_NCS	FSMC_D2	SDIO_D3	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/ I2S3_SD	USART3_CK	-	-	FSMC_D3	SDIO_CK	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 10. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port G	PG0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	FSMC_A10	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	FSMC_A11	EVENTOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	FSMC_A12	EVENTOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	FSMC_A13	EVENTOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	FSMC_A14	EVENTOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	FSMC_A15	EVENTOUT
	PG6	-	-	-	-	-	-	-	-	-	-	QUADSPI_ BK1_NCS	-	EVENTOUT
	PG7	-	-	-	-	-	-	-	-	USART6_ CK	-	-	-	EVENTOUT
	PG8	-	-	-	-	-	-	-	-	USART6_ RTS	-	-	-	EVENTOUT
	PG9	-	-	-	-	-	-	-	-	USART6_ RX	QUADSPI_ BK2_IO2	-	FSMC_NE2	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	-	-	FSMC_NE3	EVENTOUT
	PG11	-	-	-	-	-	-	-	-	-	CAN2_RX	-	-	EVENTOUT
	PG12	-	-	-	-	-	-	-	-	USART6_ RTS	CAN2_TX	-	FSMC_NE4	EVENTOUT
	PG13	TRACED2	-	-	-	-	-	-	-	USART6_ CTS	-	-	FSMC_A24	EVENTOUT
	PG14	TRACED3	-	-	-	-	-	-	-	USART6_ TX	QUADSPI_ BK2_IO3	-	FSMC_A25	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_ CTS	-	-	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Figure 26. Low-power mode wakeup



All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 37. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	-	4	6	clk cycles
$t_{WUSLEEPFDSM}$		Flash memory in Deep power down mode	-	-	50.0	µs

possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

The LSE high-power mode allows to cover a wider range of possible crystals but with a cost of higher power consumption.

Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	MΩ
I_{DD}	LSE current consumption	Low-power mode (default)	-	-	1	µA
		High-drive mode	-	-	3	
ACC_{LSE} (2)	LSE accuracy	-	-500	-	500	ppm
G_m_crit_max	Maximum critical crystal g_m	Startup, low-power mode	-	-	0.56	µA/V
		Startup, high-drive mode	-	-	1.50	
$t_{SU(LSE)}$ (3)	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.
2. This parameter depends on the crystal used in the application. Refer to the application note AN2867.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is guaranteed by characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

For information about the LSE high-power mode, refer to the reference manual RM0383.

Figure 30. Typical application with a 32.768 kHz crystal

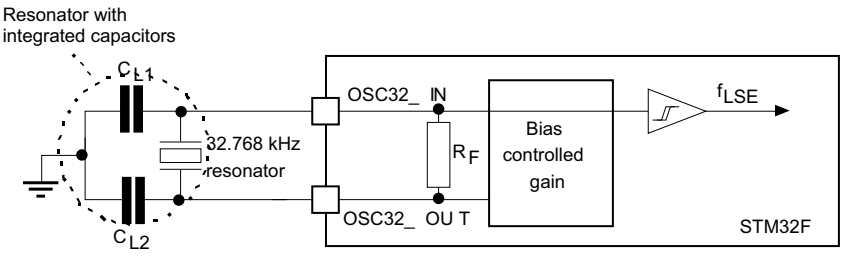


Figure 33 and *Figure 34* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 33. PLL output clock waveforms in center spread mode

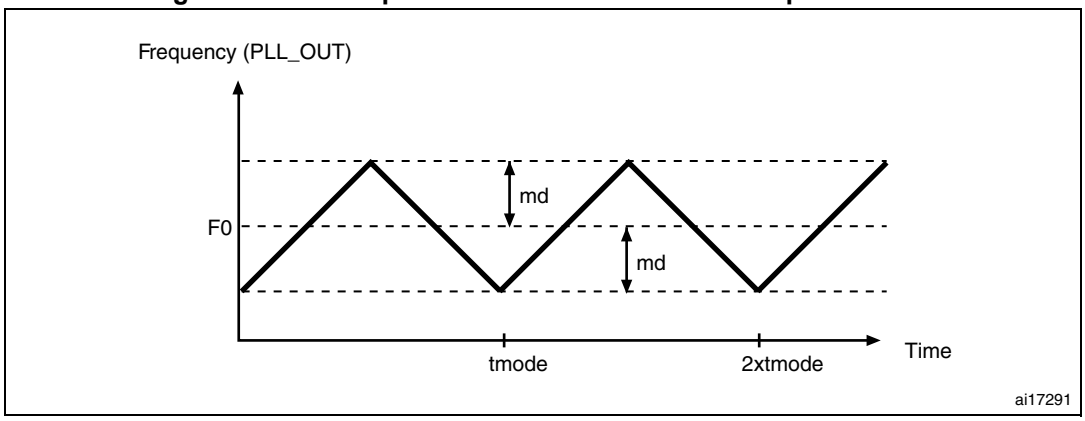
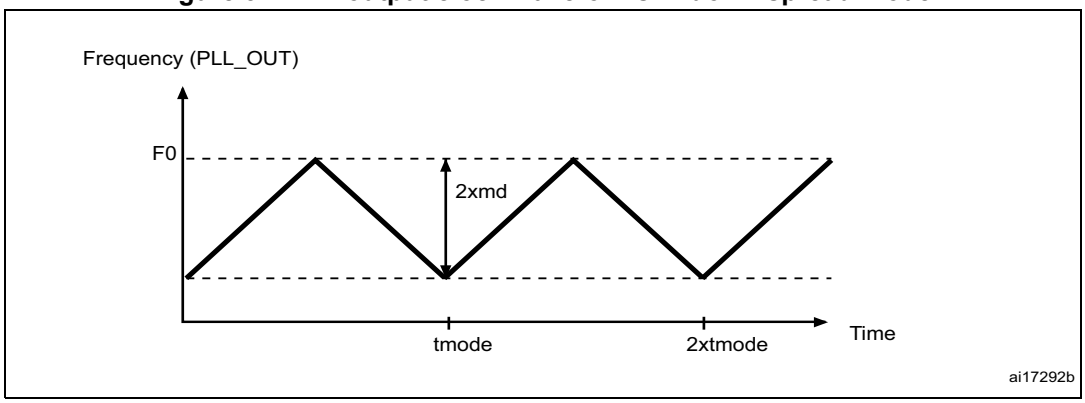


Figure 34. PLL output clock waveforms in down spread mode



6.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 47. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.7 V	-	5	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	12	-	

The test results are given in *Table 52*. They are based on the EMS levels and classes defined in application note AN1709.

Table 51. EMS characteristics for LQFP144 package

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-4	4B

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP144 packages and PDR_ON on WLCSP49.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 56. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{HYS}	FT, TC and NRST I/O input hysteresis		1.7 V≤V_{DD}≤3.6 V	10% V_{DD} (2)(3)	-	-	V
	BOOT0 I/O input hysteresis		1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤105 °C	0.1	-	-	
			1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
I_{lkg}	I/O input leakage current (4)		V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT/TC input leakage current (5)		V_{IN} = 5 V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10 (OTG_FS_ID)	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10 (OTG_FS_ID)	-	7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10 (OTG_FS_ID)	V_{IN} = V_{DD}	30	40	50	
		PA10 (OTG_FS_ID)	-	7	10	14	
C_{IO} (8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by test in production.
2. Guaranteed by design, not tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 55: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 55: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT and TC I/Os is shown in *Figure 35*.

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 65* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 65. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	2	-	
$t_{h(WS)}$	WS hold time	Slave mode	0.5	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	0	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	15	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	2.5	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	6	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization, not tested in production.
2. The maximum value of 256xFs is 50 MHz (APB1 maximum frequency).

Note: Refer to the I2S section of RM0383 reference manual for more details on the sampling frequency (F_S).

*f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Figure 45. USB OTG FS timings: definition of data signal rise and fall time

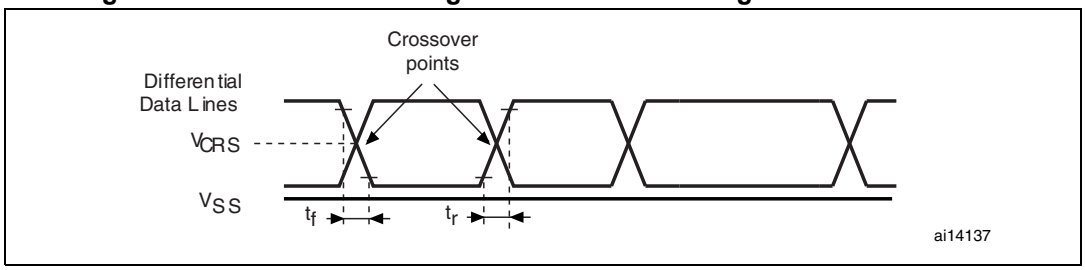


Table 70. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

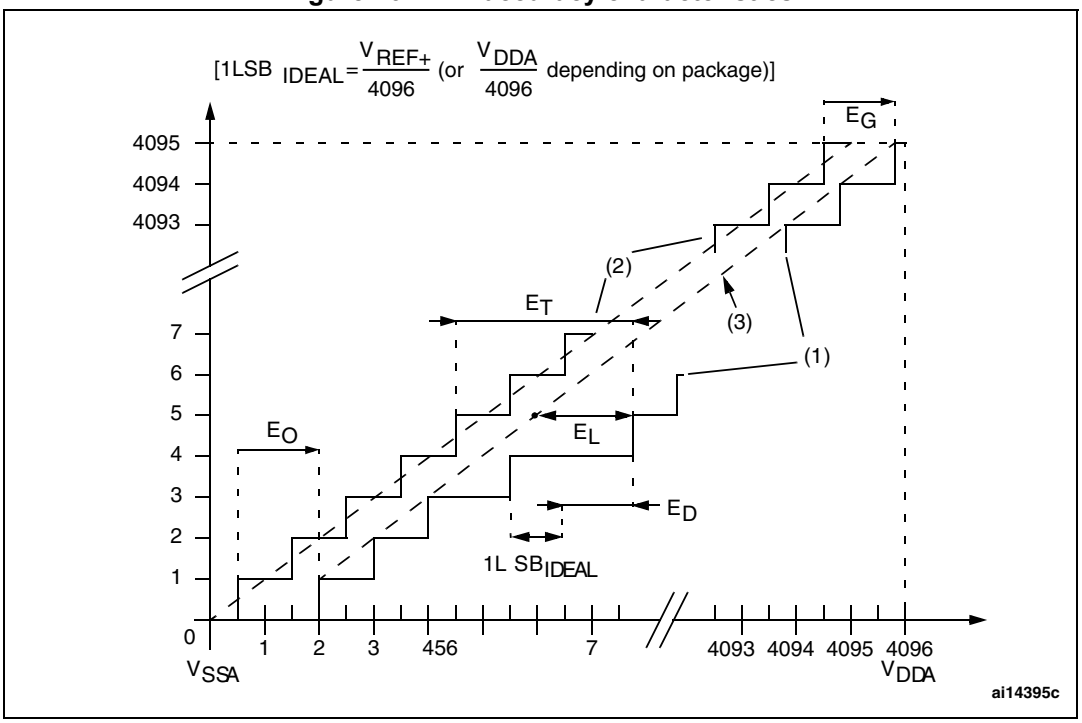
CAN (controller area network) interface

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.16* does not affect the ADC accuracy.

Figure 46. ADC accuracy characteristics



1. See also *Table 73*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 55. Synchronous multiplexed PSRAM write timings

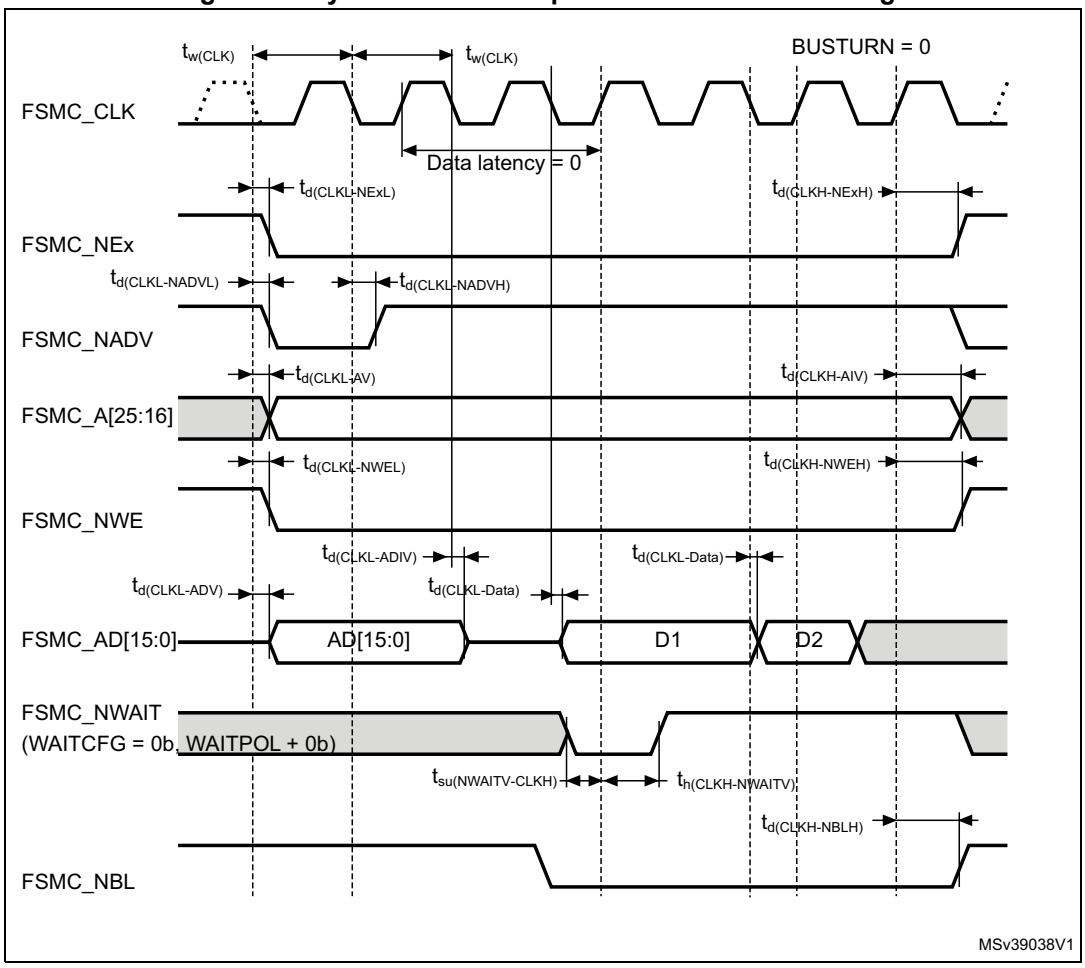


Figure 58. SDIO high-speed mode

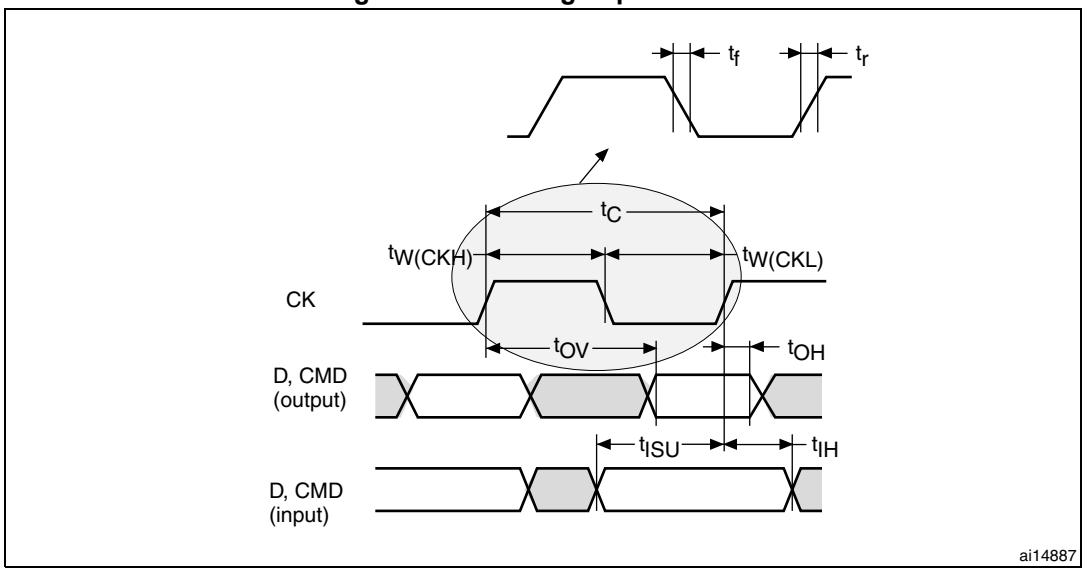


Figure 59. SD default mode

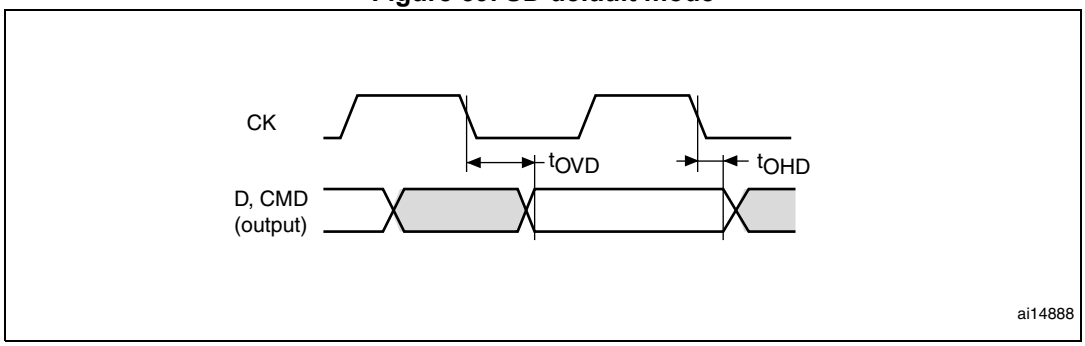


Table 95. Dynamic characteristics: SD / MMC characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50MHz	4	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	13	13.5	ns
t_{OH}	Output hold time HS	fpp =50MHz	11	-	-	