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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412vgt6

Figure 2. Compatible board design for LQFP64 package

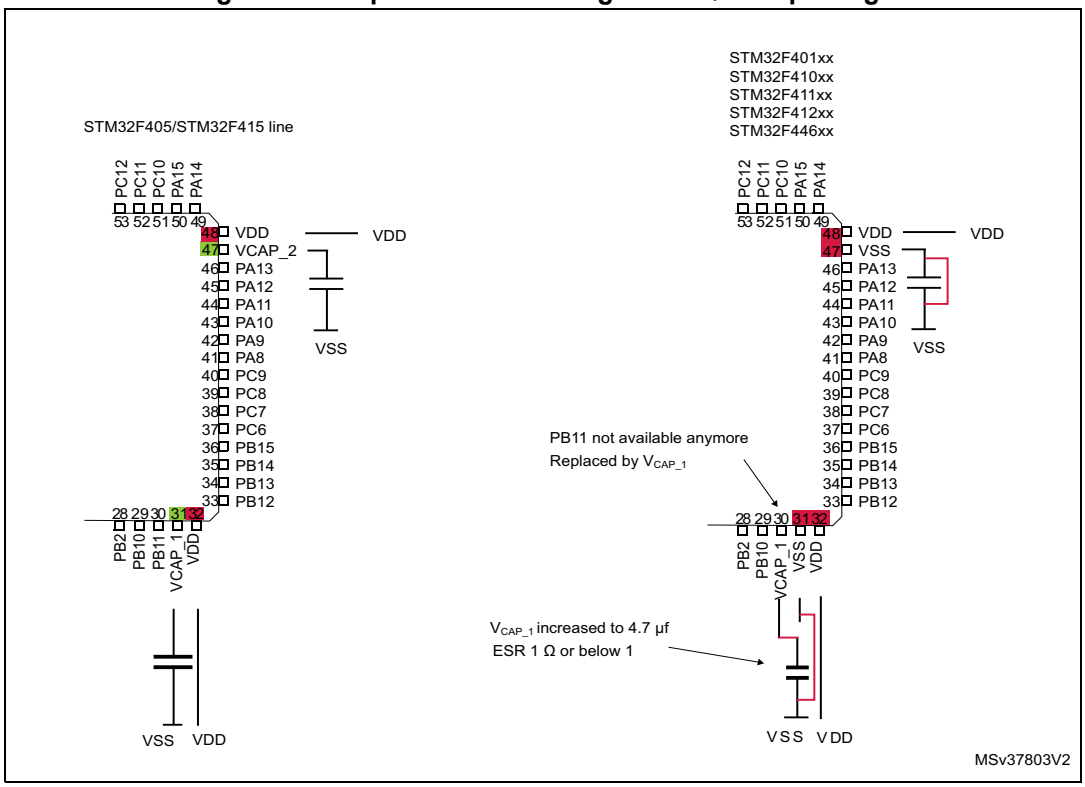
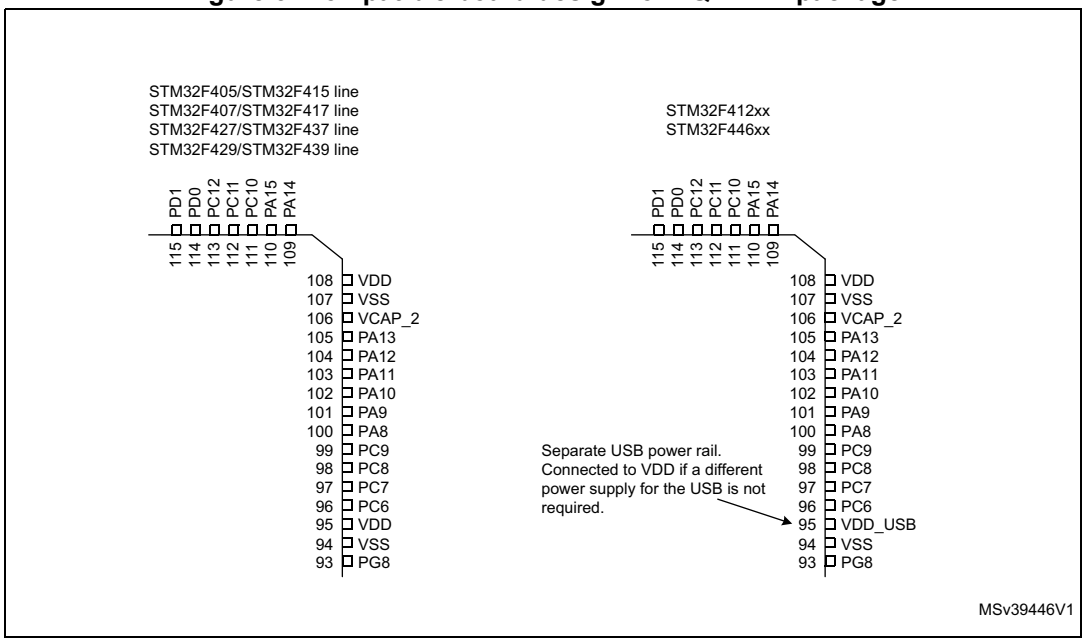


Figure 3. Compatible board design for LQFP144 package



3.33 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.34 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

3.35 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

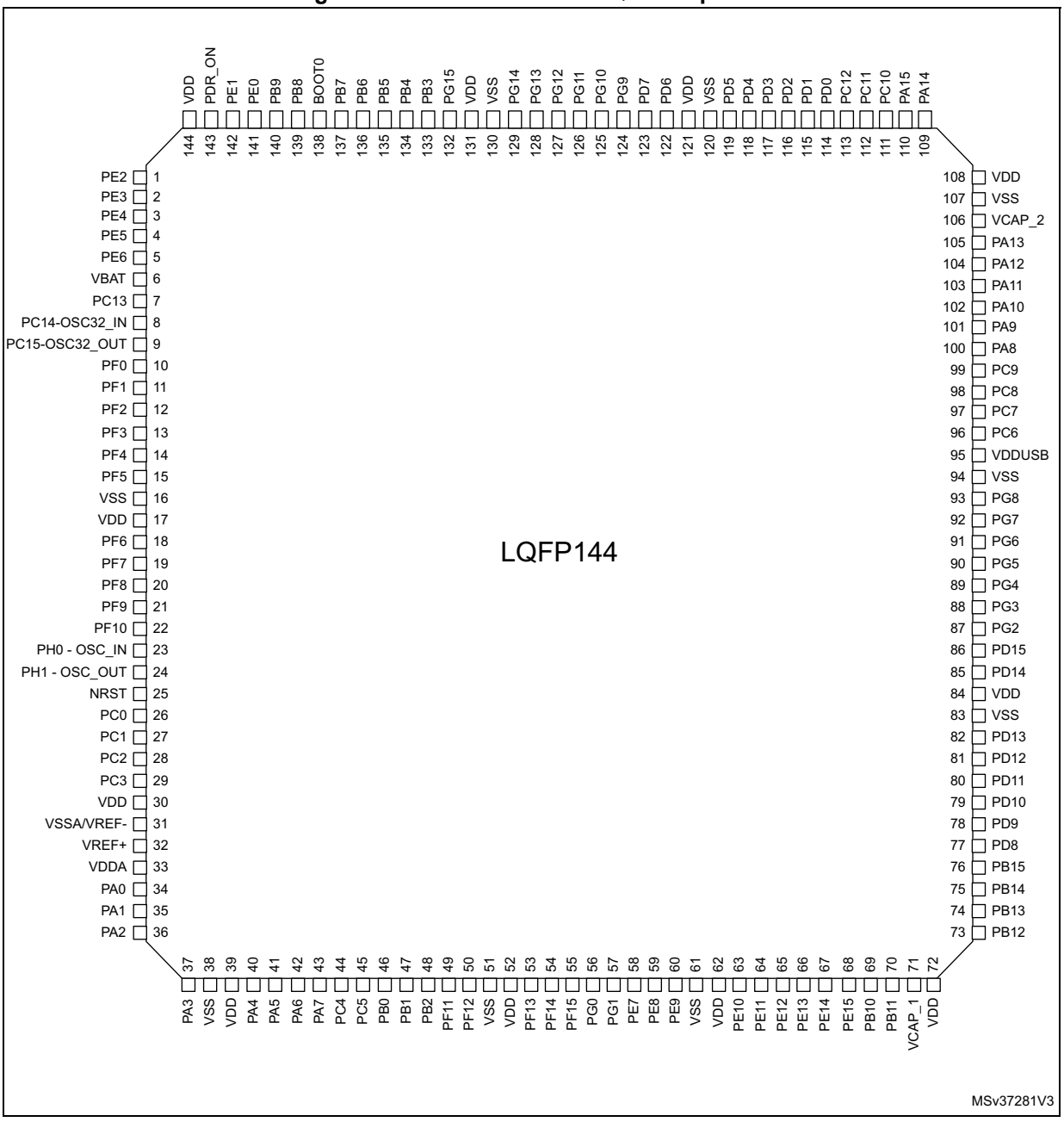
As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 15. STM32F412xE/G LQFP144 pinout



1. The above figure shows the package top view.

Table 10. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-	-	-	-	FSMC_NBL0	EVENTOUT
	PE1	-	-	-	-	-	-	-	-	-	-	-	FSMC_NBL1	EVENTOUT
	PE2	TRACECLK	-	-	-	-	SPI4_SCK/ I2S4_CK	SPI5_SCK/ I2S5_CK	-	-	QUADSPI_ BK1_IO2	-	FSMC_A23	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	-	-	-	-	-	FSMC_A19	EVENTOUT
	PE4	TRACED1	-	-	-	-	SPI4_NSS/ I2S4_WS	SPI5_NSS/ I2S5_WS	-	DFSDM1_ DATIN3	-	-	FSMC_A20	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	SPI4_MISO	SPI5_MISO	-	DFSDM1_ CKIN3	-	-	FSMC_A21	EVENTOUT
	PE6	TRACED3	-	-	TIM9_CH2	-	SPI4_MOSI/I 2S4_SD	SPI5_MOSI/ I2S5_SD	-	-	-	-	FSMC_A22	EVENTOUT
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_ DATIN2	-	-	-	QUADSPI_ BK2_IO0	FSMC_D4/ FSMC_DA4	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_ CKIN2	-	-	-	QUADSPI_ BK2_IO1	FSMC_D5/ FSMC_DA5	EVENTOUT
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_ CKOUT	-	-	-	QUADSPI_ BK2_IO2	FSMC_D6/ FSMC_DA6	EVENTOUT
	PE10	-	TIM1_CH2N	-	-	-	-	-	-	-	-	QUADSPI_ BK2_IO3	FSMC_D7/ FSMC_DA7	EVENTOUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS/ I2S4_WS	SPI5_NSS/ I2S5_WS	-	-	-		FSMC_D8/ FSMC_DA8	EVENTOUT
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK/ I2S4_CK	SPI5_SCK/ I2S5_CK	-	-	-	-	FSMC_D9/ FSMC_DA9	EVENTOUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	SPI5_MISO	-	-	-	-	FSMC_D10/ FSMC_DA10	EVENTOUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI/I 2S4_SD	SPI5_MOSI/ I2S5_SD	-	-	-	-	FSMC_D11/ FSMC_DA11	EVENTOUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	FSMC_D12/ FSMC_DA12	EVENTOUT

Table 10. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	FSMC_A0	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	FSMC_A1	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	FSMC_A2	EVENTOUT
	PF3	-	-	TIM5_CH1	-	-	-	-	-	-	-	-	FSMC_A3	EVENTOUT
	PF4	-	-	TIM5_CH2	-	-	-	-	-	-	-	-	FSMC_A4	EVENTOUT
	PF5	-	-	TIM5_CH3	-	-	-	-	-	-	-	-	FSMC_A5	EVENTOUT
	PF6	TRACED0	-	-	TIM10_CH1	-	-	-	-	-	QUADSPI_ BK1_IO3	-	-	EVENTOUT
	PF7	TRACED1	-	-	TIM11_CH1	-	-	-	-	-	QUADSPI_ BK1_IO2	-	-	EVENTOUT
	PF8	-	-	-	-	-	-	-	-	-	TIM13_CH1	QUADSPI_ BK1_IO0	-	EVENTOUT
	PF9	-	-	-	-	-	-	-	-	-	TIM14_CH1	QUADSPI_ BK1_IO1	-	EVENTOUT
	PF10	-	TIM1_ETR	TIM5_CH4	-	-	-	-	-	-	-	-	-	EVENTOUT
	PF11	-	-	-	TIM8_ETR	-	-	-	-	-	-	-	-	EVENTOUT
	PF12	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	FSMC_A6	EVENTOUT
	PF13	-	-	-	-	I2CFMP1_ SMBA	-	-	-	-	-	-	FSMC_A7	EVENTOUT
	PF14	-	-	-	-	I2CFMP1_ SCL	-	-	-	-	-	-	FSMC_A8	EVENTOUT
	PF15	-	-	-	-	I2CFMP1_ SDA	-	-	-	-	-	-	FSMC_A9	EVENTOUT

Table 11. STM32F412xE/G register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 6400- 0x4001 FFFF	Reserved
	0x4001 6000 - 0x4001 63FF	DFSDM1
	0x4001 5400 - 0x4001 5FFF	Reserved
	0x4001 5000 - 0x4001 53FF	SPI5/I2S5
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4/I2S4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7400 - 0x4000 FFFF	Reserved

Table 13. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)(1)	160	mA
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	-160	
ΣI_{VDDUSB}	Total current into V_{DDUSB} power lines (source)	25	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	-100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins (2)	120	
	Total output current sunk by sum of all USB I/Os	25	
	Total output current sourced by sum of all I/Os and control pins(2)	-120	
$I_{INJ(PIN)}$ (3)	Injected current on FT and TC pins (4)	–5/+0	
	Injected current on NRST and B pins (4)		
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, V_{DDUSB}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 14. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	
T_{LEAD}	Maximum lead temperature during soldering (WLCSP64, LQFP64/100/144, UFQFPN48, UFBGA100/144)	see note (1)	

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 19. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

Note: This feature is only available for UFBGA100 and UFBGA144 packages.

6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 20* are derived from tests performed under ambient temperature and V_{DD} supply voltage @ 3.3V.

Table 20. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60(1)	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	

Table 22. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A= 25 °C	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	28.4	28.80(3)	30.84	32.39(3)	mA
			84	23.0	24.09(3)	25.20	26.57(3)	
			64	16.0	16.83(3)	17.77	19.12(3)	
			50	12.6	13.46	13.98	14.68	
			25	6.8	7.63	8.14	8.61	
			20	5.8	6.31	6.74	7.43	
		HSI, PLL OFF(4), all peripherals enabled(2)	16	3.9	4.65	5.33	6.11	
			1	0.6	0.78	1.34	2.00	
		External clock, PLL ON, all peripherals disabled(2)	100	14.3	15.09(3)	16.22	17.90(3)	
			84	11.6	12.28(3)	13.36	14.99(3)	
			64	8.2	8.75(3)	9.68	11.21(3)	
			50	6.5	7.21	7.69	8.47	
			25	3.6	4.22	4.68	5.29	
			20	3.2	3.65	4.18	4.94	
		HSI, PLL OFF, all peripherals disabled(2)	16	2.0	2.48	3.12	3.94	
			1	0.5	0.65	1.26	1.94	

1. Based on characterization, not tested in production unless otherwise specified
2. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
3. Tested in production
4. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. Tested in production.

Table 29. Typical and maximum current consumption in Sleep mode - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Sleep mode**	External clock, PLL ON, Flash deep power down, all peripherals enabled(2)	100	17.3	18.62	19.90	21.40	mA
			84	14.0	15.08	16.04	17.16	
			64	9.7	10.41	11.02	11.80	
			50	7.6	8.27	8.89	9.62	
			25	4.2	4.79	5.35	6.00	
			20	3.7	4.11	4.67	5.31	
		HSI, PLL OFF(2), Flash deep power down, all peripherals enabled	16	2.4	2.81	3.45	4.20	
			1	0.5	0.67	1.27	1.91	
		External clock, PLL ON(2) all peripherals enabled, Flash ON	100	17.8	19.08	20.35	21.90	
			84	14.4	15.49	16.42	17.59	
			64	10.0	10.76	11.43	12.18	
			50	7.9	8.58	9.19	9.94	
			25	4.4	4.99	5.54	6.21	
			20	4.0	4.42	4.95	5.64	
		HSI, PLL OFF(2), all peripherals enabled, Flash ON	16	2.7	3.09	3.75	4.49	
			1	0.8	0.93	1.52	2.18	

pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

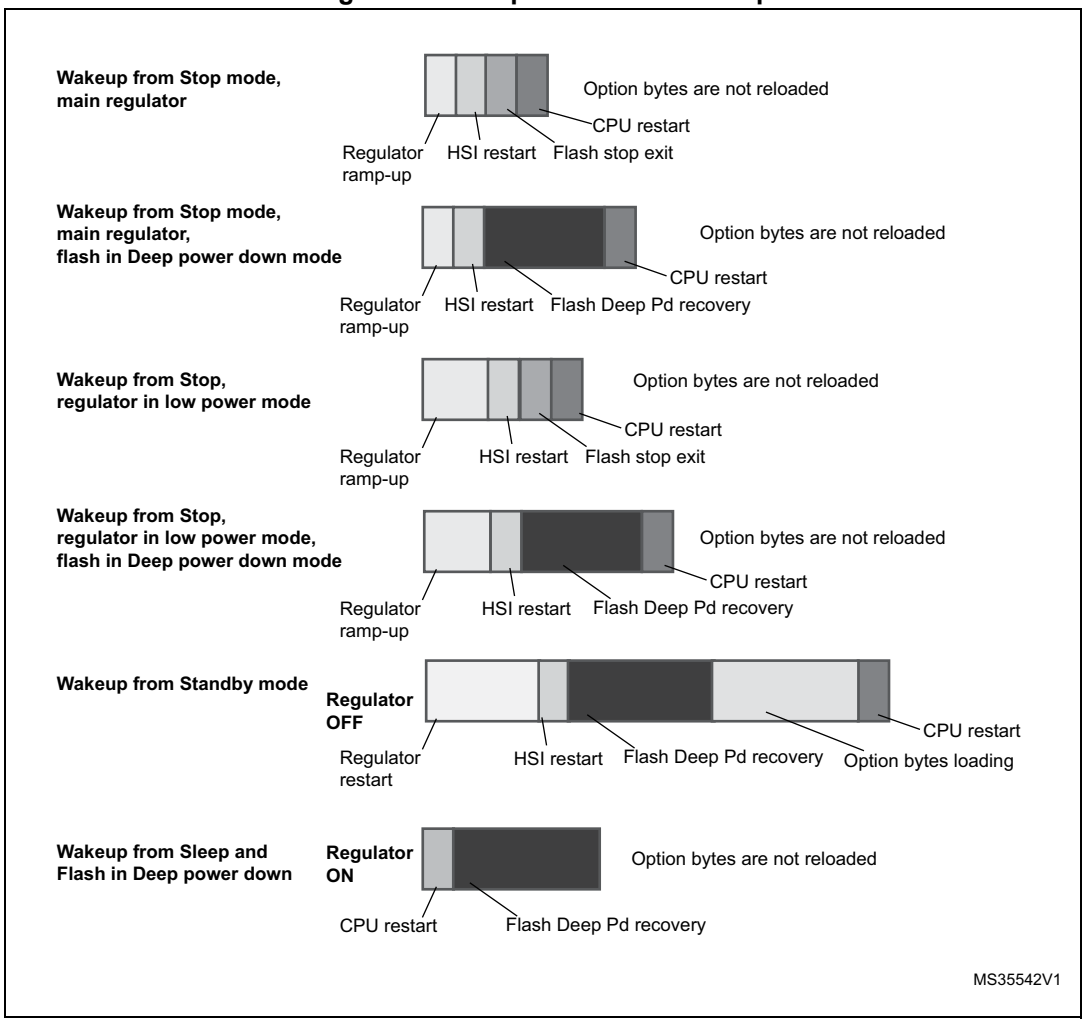
V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Figure 26. Low-power mode wakeup



All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 37. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	-	4	6	clk cycles
$t_{WUSLEEPFDSM}$		Flash memory in Deep power down mode	-	-	50.0	µs

6.3.10 PLL characteristics

The parameters given in *Table 44* and *Table 45* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

Table 44. Main PLL characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-		0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-		24	-	100	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-		-	48	75	MHz
f_{VCO_OUT}	PLL VCO output	-		100	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Cycle-to-cycle jitter	System clock 100 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples.		-	330	-	
$I_{DD(PLL)}$(4)	PLL power consumption on VDD	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on VDDA	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design, not tested in production.
3. The use of two PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization, not tested in production.

Table 45. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(1)	-		0.95(2)	1	2.10	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock	-		-	-	216	
f_{VCO_OUT}	PLLI2S VCO output	-		100	-	432	
t_{LOCK}	PLLI2S lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48 kHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design, not tested in production.
3. Value given with main PLL running.
4. Guaranteed by characterization, not tested in production.

The test results are given in *Table 52*. They are based on the EMS levels and classes defined in application note AN1709.

Table 51. EMS characteristics for LQFP144 package

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-4	4B

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP144 packages and PDR_ON on WLCSP49.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Figure 53. Asynchronous multiplexed PSRAM/NOR write waveforms

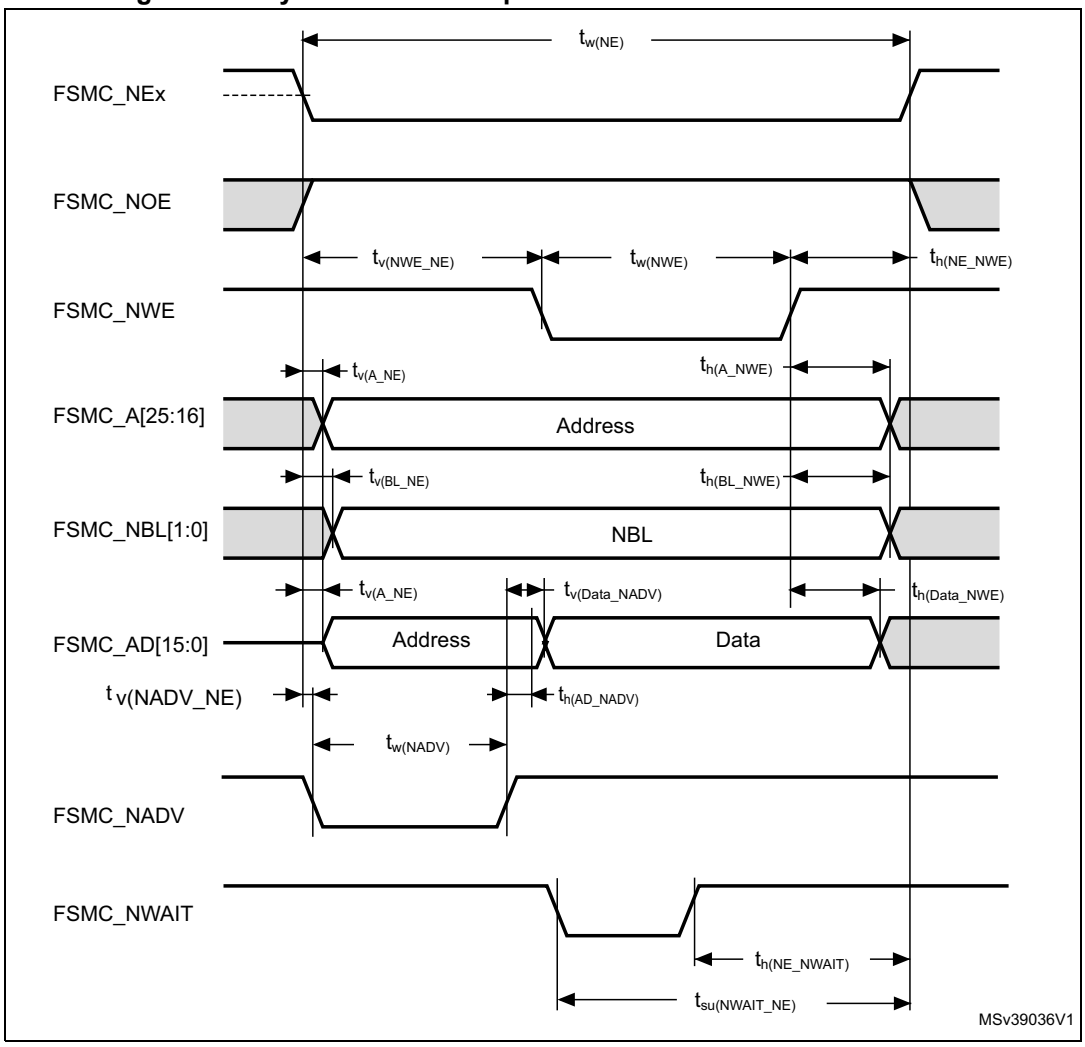


Table 91. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH\_NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	T_{HCLK}	-	
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	1	-	
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	2	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

1. C_L = 30 pF.
2. Based on characterization, not tested in production.

Figure 56. Synchronous non-multiplexed NOR/PSRAM read timings

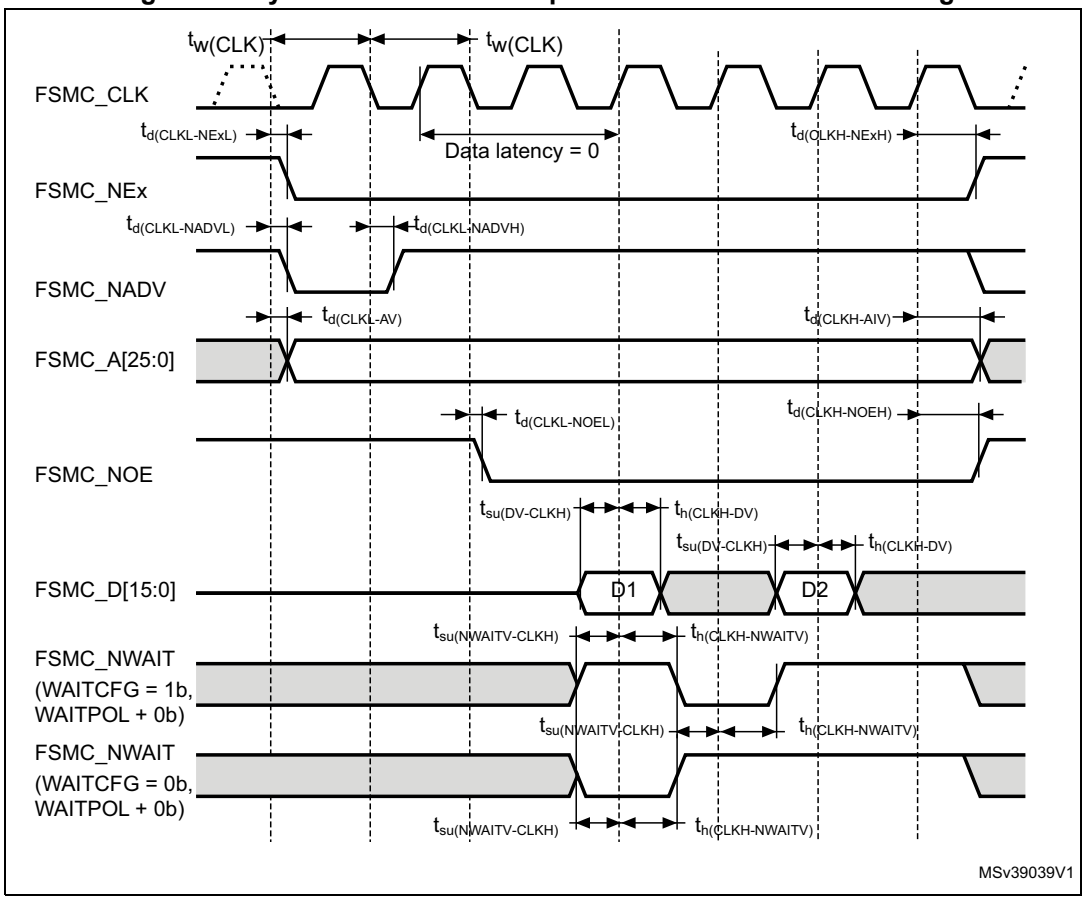


Table 93. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK} - 0.5$	-	ns
$t_{(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} +0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	T_{HCLK}	-	
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	1	-	
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	2	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

Figure 58. SDIO high-speed mode

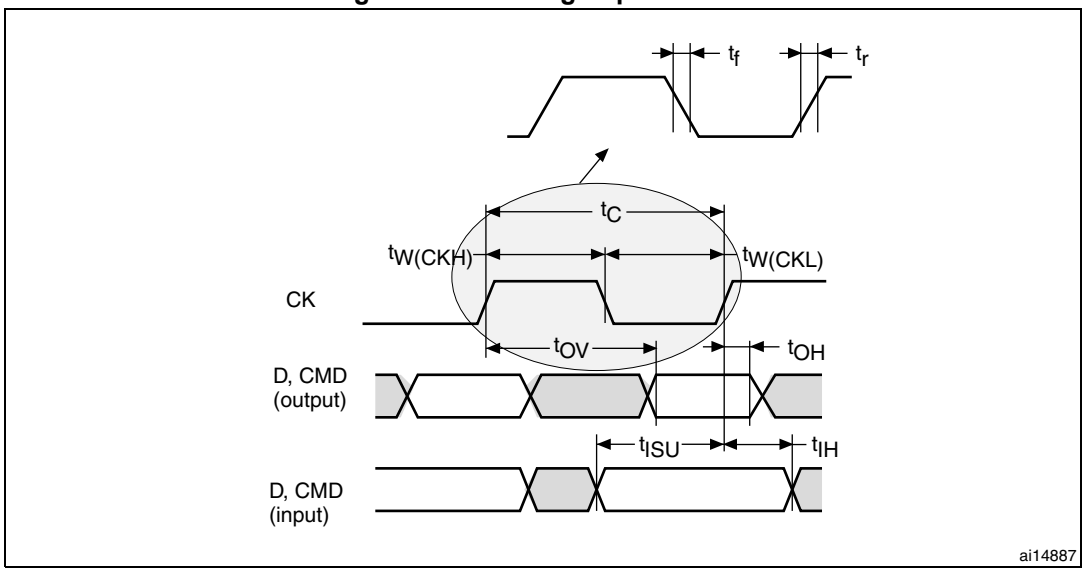


Figure 59. SD default mode

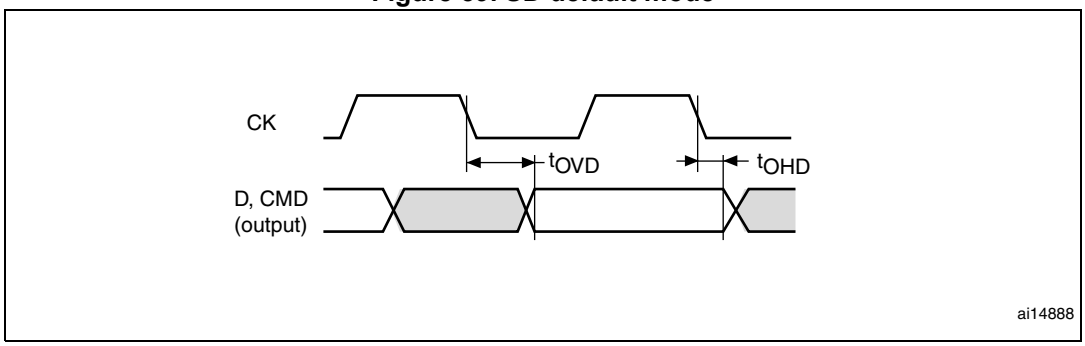
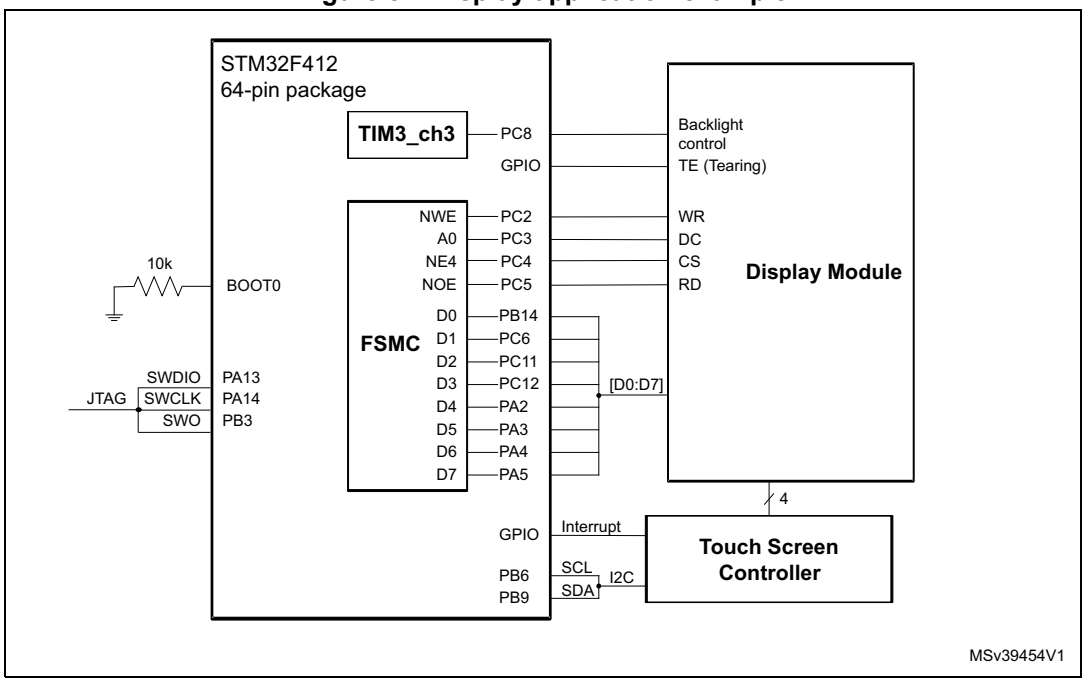


Table 95. Dynamic characteristics: SD / MMC characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50MHz	4	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	13	13.5	ns
t_{OH}	Output hold time HS	fpp =50MHz	11	-	-	

B.3 Display application example

Figure 87. Display application example



Note: 16 bit displays interfaces can be addressed with 100 and 144 pins packages.