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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412vgt6tr

3.18 Power supply supervisor

3.18.1 Internal reset ON

This feature is available for V_{DD} operating voltage range 1.8 V to 3.6 V.

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other package, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

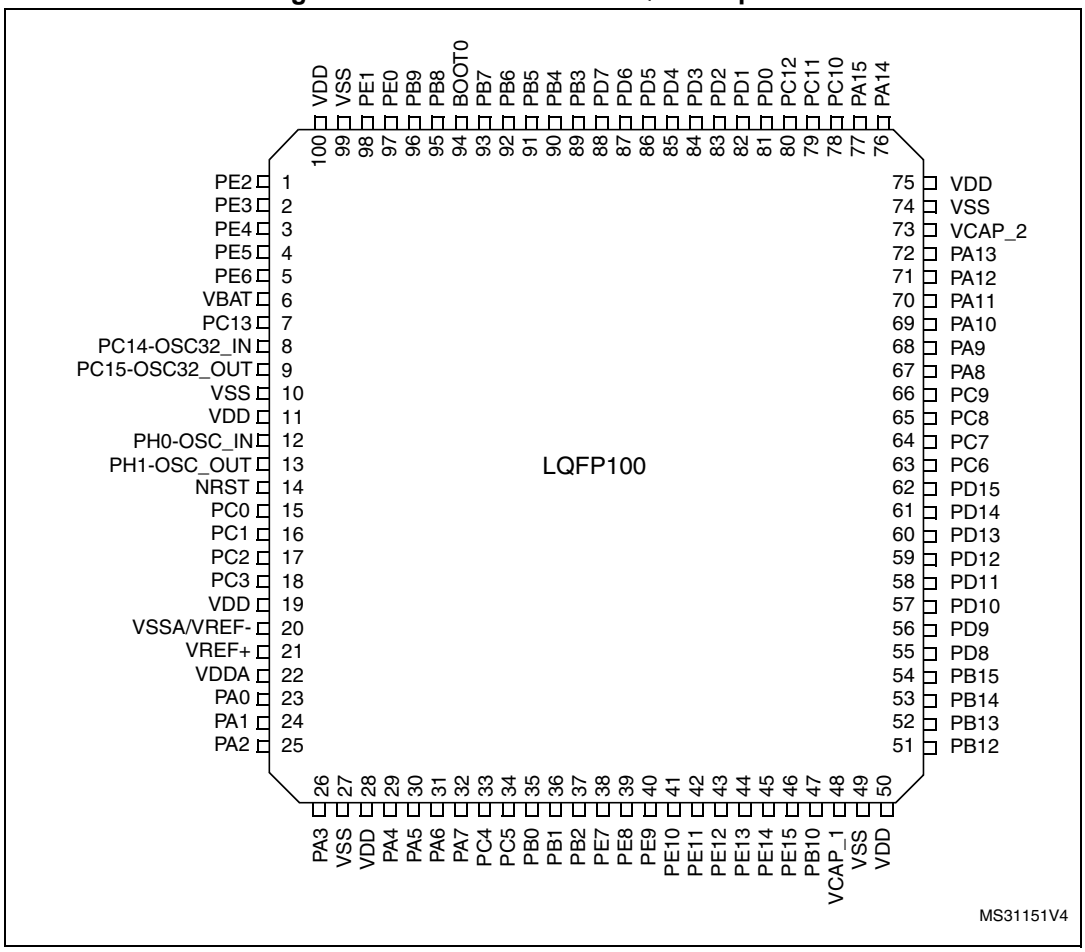
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.18.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor V_{DD} and should set the device in reset mode when V_{DD} is below 1.7 V. NRST should be connected to this external power supply supervisor. Refer to *Figure 7: Power supply supervisor interconnection with internal reset OFF*.

Figure 14. STM32F412xE/G LQFP100 pinout



1. The above figure shows the package top view.

Table 9. STM32F412xE/G pin definition

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	1	B2	A3	1	PE2	I/O	FT	-	TRACECLK, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, QUADSPI_BK1_IO2, FSMC_A23, EVENTOUT	-
-	-	-	2	A1	A2	2	PE3	I/O	FT	-	TRACED0, FSMC_A19, EVENTOUT	-
-	-	-	3	B1	B2	3	PE4	I/O	FT	-	TRACED1, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, DFSDM1_DATIN3, FSMC_A20, EVENTOUT	-
-	-	-	4	C2	B3	4	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SPI5_MISO, DFSDM1_CKIN3, FSMC_A21, EVENTOUT	-
-	-	-	5	D2	B4	5	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, FSMC_A22, EVENTOUT	-
1	1	B7	6	E2	C2	6	VBAT	S	-	-	-	VBAT
2	2	B8	7	C1	A1	7	PC13	I/O	FT	(2)(3)	EVENTOUT	TAMP_1
3	3	C8	8	D1	B1	8	PC14-OSC32_IN	I/O	FT	(2)(3)(4)	EVENTOUT	OSC32_IN
4	4	C7	9	E1	C1	9	PC15-OSC32_OUT	I/O	FT	(2)(4)	EVENTOUT	OSC32_OUT
-	-	-	-	-	C3	10	PF0	I/O	FT	-	I2C2_SDA, FSMC_A0, EVENTOUT	-
-	-	-	-	-	C4	11	PF1	I/O	FT	-	I2C2_SCL, FSMC_A1, EVENTOUT	-
-	-	-	-	-	D4	12	PF2	I/O	FT	-	I2C2_SMBA, FSMC_A2, EVENTOUT	-
-	-	-	-	-	E2	13	PF3	I/O	FT	-	TIM5_CH1, FSMC_A3, EVENTOUT	-
-	-	-	-	-	E3	14	PF4	I/O	FT	-	TIM5_CH2, FSMC_A4, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	-	E4	15	PF5	I/O	FT	-	TIM5_CH3, FSMC_A5, EVENTOUT	-
-	-	-	10	F2	D2	16	VSS	S	-	-	-	-
-	-	-	11	G2	D3	17	VDD	S	-	-	-	-
-	-	-	-	-	F3	18	PF6	I/O	FT	-	TRACED0, TIM10_CH1, QUADSPI_BK1_IO3, EVENTOUT	-
-	-	-	-	-	F2	19	PF7	I/O	FT	-	TRACED1, TIM11_CH1, QUADSPI_BK1_IO2, EVENTOUT	-
-	-	-	-	-	G3	20	PF8	I/O	FT	-	TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	-
-	-	-	-	-	G2	21	PF9	I/O	FT	-	TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	-
-	-	-	-	-	G1	22	PF10	I/O	FT	-	TIM1_ETR, TIM5_CH4, EVENTOUT	-
5	5	D8	12	F1	D1	23	PH0 - OSC_IN	I/O	FT	(4)	EVENTOUT	OSC_IN
6	6	E8	13	G1	E1	24	PH1 - OSC_OUT	I/O	FT	(4)	EVENTOUT	OSC_OUT
7	7	D7	14	H2	F1	25	NRST	I/O	RST	-	-	NRST
-	8	D5	15	H1	H1	26	PC0	I/O	FT	-	EVENTOUT	ADC1_10, WKUP2
-	9	F8	16	J2	H2	27	PC1	I/O	FT	-	EVENTOUT	ADC1_11, WKUP3
-	10	E7	17	J3	H3	28	PC2	I/O	FT	-	SPI2_MISO, I2S2ext_SD, DFSDM1_CKOUT, FSMC_NWE, EVENTOUT	ADC1_12
-	11	D6	18	K2	H4	29	PC3	I/O	FT	-	SPI2_MOSI/I2S2_SD, FSMC_A0, EVENTOUT	ADC1_13
-	-	-	19	-	-	30	VDD	S	-	-	-	-
8	12	G8	20	-	-	31	VSSA/ VREF	S	-	-	-	-
-	-	-	-	J1	J1	-	VSSA	S	-	-	-	-

Table 10. STM32F412xE/G alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port A	PA0	-	TIM2_CH1/ TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	-	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	SPI4_MOSI/I 2S4_SD	-	USART2_RTS	-	QUADSPI_ BK1_IO3	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	I2S2_CKIN	-	USART2_TX	-	-	-	FSMC_D4	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	I2S2_MCK	-	USART2_RX	-	-	-	FSMC_D5	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS/I2 S1_WS	SPI3_NSS/ I2S3_WS	USART2_CK	DFSDM1_ DATIN1	-	-	FSMC_D6	EVENTOUT
	PA5	-	TIM2_CH1/ TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/ I2S1_CK	-	-	DFSDM1_ CKIN1	-	-	FSMC_D7	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	I2S2_MCK	-	-	TIM13_ CH1	QUADSPI_ BK2_IO0	SDIO_CMD	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I 2S1_SD	-	-	-	TIM14_ CH1	QUADSPI_ BK2_IO1	-	EVENTOUT
	PA8	MCO_1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	USB_FS_ SOF	SDIO_D1	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_ SMBA	-	-	USART1_TX	-	-	USB_FS_ VBUS	SDIO_D2	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	SPI5_MOSI/ I2S5_SD	USART1_RX	-	-	USB_FS_ID	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	SPI4_MISO	USART1_CTS	USART6_ TX	CAN1_RX	USB_FS_DM	-	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	SPI5_MISO	USART1_RTS	USART6_ RX	CAN1_TX	USB_FS_DP	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	-	-	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	USART1_TX	-	-	-	-	EVENTOUT

Table 10. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port G	PG0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	FSMC_A10	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	FSMC_A11	EVENTOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	FSMC_A12	EVENTOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	FSMC_A13	EVENTOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	FSMC_A14	EVENTOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	FSMC_A15	EVENTOUT
	PG6	-	-	-	-	-	-	-	-	-	-	QUADSPI_ BK1_NCS	-	EVENTOUT
	PG7	-	-	-	-	-	-	-	-	USART6_ CK	-	-	-	EVENTOUT
	PG8	-	-	-	-	-	-	-	-	USART6_ RTS	-	-	-	EVENTOUT
	PG9	-	-	-	-	-	-	-	-	USART6_ RX	QUADSPI_ BK2_IO2	-	FSMC_NE2	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	-	-	FSMC_NE3	EVENTOUT
	PG11	-	-	-	-	-	-	-	-	-	CAN2_RX	-	-	EVENTOUT
	PG12	-	-	-	-	-	-	-	-	USART6_ RTS	CAN2_TX	-	FSMC_NE4	EVENTOUT
	PG13	TRACED2	-	-	-	-	-	-	-	USART6_ CTS	-	-	FSMC_A24	EVENTOUT
	PG14	TRACED3	-	-	-	-	-	-	-	USART6_ TX	QUADSPI_ BK2_IO3	-	FSMC_A25	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_ CTS	-	-	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 11. STM32F412xE/G register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 6400- 0x4001 FFFF	Reserved
	0x4001 6000 - 0x4001 63FF	DFSDM1
	0x4001 5400 - 0x4001 5FFF	Reserved
	0x4001 5000 - 0x4001 53FF	SPI5/I2S5
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4/I2S4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7400 - 0x4000 FFFF	Reserved

6.3 Operating conditions

6.3.1 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale3: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x01	0	-	64	MHz
		Power Scale2: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x10	0	-	84	
		Power Scale1: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x11	0	-	100	
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	50	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	-	100	MHz
V_{DD}	Standard operating voltage	-	1.7(1)	-	3.6	V
V_{DDA}(2)(3)	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}(4)	1.7(1)	-	2.4	V
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11 and PA12 pins)	USB not used	1.7	3.3	3.6	V
		USB used(5)	3.0	-	3.6	
V_{BAT}	Backup operating voltage	-	1.65	-	3.6	V
V_{12}	Regulator ON: 1.2 V internal voltage on VCAP_1/VCAP_2 pins	VOS[1:0] bits in PWR_CR register = 0x01 Max frequency 64 MHz	1.08(6)	1.14	1.20(6)	V
		VOS[1:0] bits in PWR_CR register = 0x10 Max frequency 84 MHz	1.20(6)	1.26	1.32(6)	
		VOS[1:0] bits in PWR_CR register = 0x11 Max frequency 100 MHz	1.26	1.32	1.38	
V_{12}	Regulator OFF: 1.2 V external voltage must be supplied on VCAP_1/VCAP_2 pins	Max frequency 64 MHz	1.10	1.14	1.20	V
		Max frequency 84 MHz	1.20	1.26	1.32	
		Max frequency 100 MHz	1.26	1.32	1.38	
V_{IN}	Input voltage on RST, FT and TC pins(7)	$2\ V \le V_{DD} \le 3.6\ V$	–0.3	-	5.5	V
		$V_{DD} \le 2\ V$	–0.3	-	5.2	
	Input voltage on BOOT0 pin	-	0	-	9	

Table 24. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)	100	27.2	28.70(4)	30.14	31.98	mA
			84	21.9	23.60	24.31	25.37	
			64	15.2	16.45	17.03	17.87	
			50	12.1	13.12	13.67	14.46	
			25	6.6	7.59	8.12	8.77	
			20	5.7	6.51	7.07	7.77	
		HSI, PLL OFF, all peripherals enabled(3)	16	4.0	4.32	4.88	5.69	
			1	0.8	1.14	1.67	2.38	
		External clock, PLL ON(2) all peripherals disabled(3)	100	13.0	14.06(4)	15.34	17.27	
			84	10.5	11.21	12.16	13.47	
			64	7.5	8.29	9.01	9.88	
			50	6.0	6.73	7.32	8.27	
			25	3.5	4.18	4.73	5.57	
			20	3.1	3.72	4.25	5.10	
		HSI, PLL OFF, all peripherals disabled(3)	16	2.1	2.41	2.94	3.75	
			1	0.7	0.99	1.51	2.30	

1. Based on characterization, not tested in production unless otherwise specified.
2. Refer to *Table 44* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
4. Tested in production.

Table 27. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	38.9	41.10	42.85	44.28	mA
			84	32.8	34.61	35.77	36.72	
			64	23.6	24.96	25.84	26.64	
			50	18.7	19.90	20.67	21.45	
			25	10.1	11.11	11.70	12.40	
			20	8.6	9.46	10.07	10.81	
		HSI, PLL OFF, all peripherals enabled	16	6.3	6.77	7.42	8.21	
			1	1.1	1.35	1.84	2.59	
		External clock, PLL ON(2) all peripherals disabled	100	24.7	26.11	27.59	28.84	
			84	21.4	22.22	23.53	24.66	
			64	15.8	16.80	17.90	18.99	
			50	12.6	13.51	14.52	15.54	
			25	7.0	7.85	8.57	9.39	
			20	6.0	6.67	7.37	8.26	
		HSI, PLL OFF, all peripherals disabled	16	4.5	4.80	5.47	6.33	
			1	0.9	1.25	1.81	2.58	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

The LSE high-power mode allows to cover a wider range of possible crystals but with a cost of higher power consumption.

Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

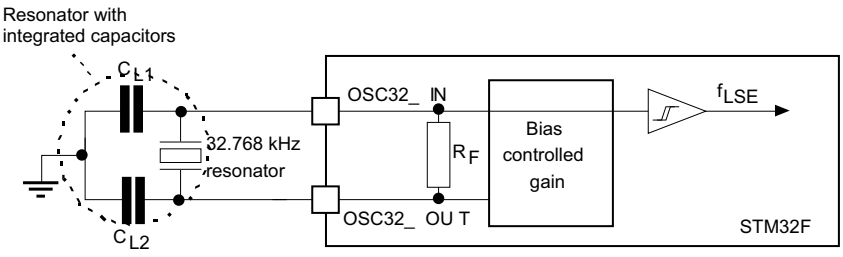
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	MΩ
I_{DD}	LSE current consumption	Low-power mode (default)	-	-	1	µA
		High-drive mode	-	-	3	
ACC_{LSE} (2)	LSE accuracy	-	-500	-	500	ppm
G_m_crit_max	Maximum critical crystal g_m	Startup, low-power mode	-	-	0.56	µA/V
		Startup, high-drive mode	-	-	1.50	
$t_{SU(LSE)}$ (3)	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.
2. This parameter depends on the crystal used in the application. Refer to the application note AN2867.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is guaranteed by characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

For information about the LSE high-power mode, refer to the reference manual RM0383.

Figure 30. Typical application with a 32.768 kHz crystal



6.3.9 Internal clock source characteristics

The parameters given in *Table 42* and *Table 43* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

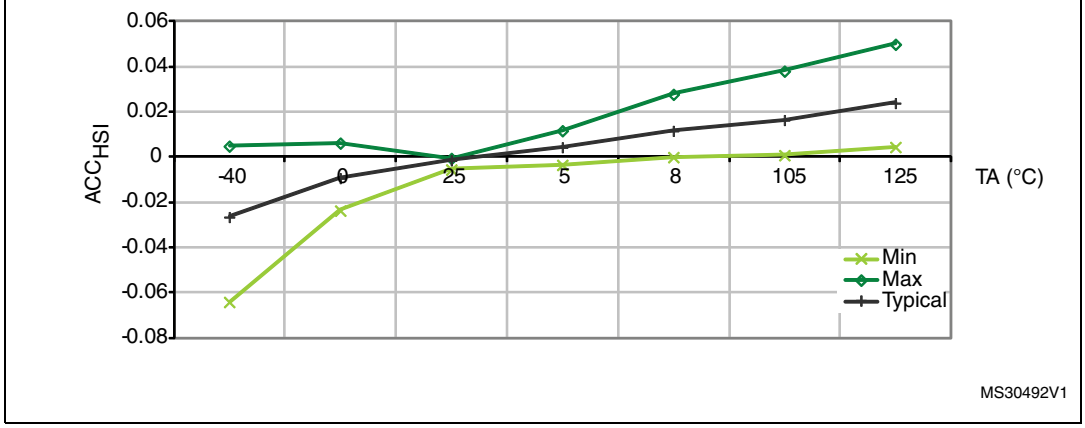
High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	–8	-	4.5	%
		T_A = –10 to 85 °C(3)	–4	-	4	%
		T_A = 25 °C(4)	–1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production
3. Based on characterization, not tested in production
4. Factory calibrated, parts not soldered.

Figure 31. ACC_{HSI} versus temperature



1. Guaranteed by characterization, not tested in production.

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 61*. Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

The I²C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more details about the complete solution, contact your local ST sales representative.

Table 61. I²C characteristics

Symbol	Parameter	Standard mode I²C(1)(2)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	3450(3)	0	900(4)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard fast mode	-	-	50	120(5)	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

FMPI^{2}C characteristics

The following table presents FMPI^{2}C characteristics.

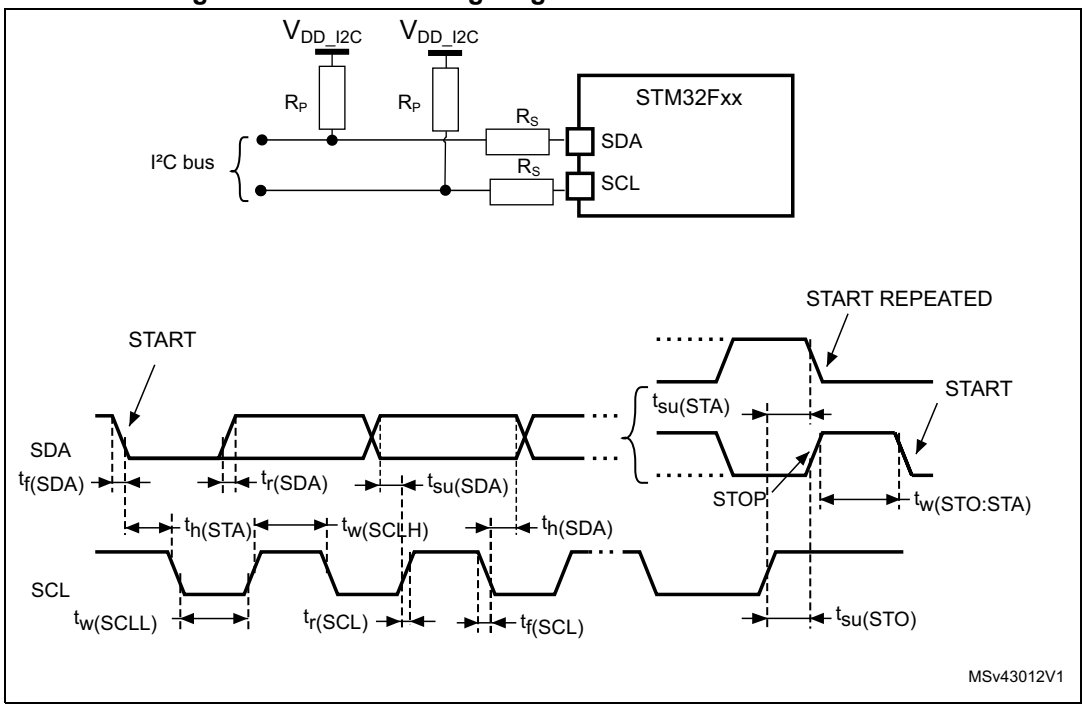
Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output function characteristics (SDA and SCL).

Table 63. FMPI^{2}C characteristics(1)

	Parameter	Standard mode		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
$f_{FMPI2CC}$	$F_{MPI2CCLK}$ frequency	2	-	8	-	18	-	µs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	
$t_{su(SDA)}$	SDA setup time	0.25	-	0.10	-	0.05	-	
$t_{H(SDA)}$	SDA data hold time	0	-	0	-	0	-	
$t_{v(SDA,ACK)}$	Data, ACK valid time	-	3.45	-	0.9	-	0.45	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1.0	-	0.30	-	0.12	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	0.30	-	0.30	-	0.12	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	0.26	-	
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	0.26	-	
$t_{su(STO)}$	Stop condition setup time	4	-	0.6	-	0.26	-	
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	0.5	-	
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	-	-	0.05	0.1	0.05	0.1	
C_b	Capacitive load for each bus Line	-	400	-	400	-	550(2)	pF

1. Based on characterization results, not tested in production.
2. Can be limited. Maximum supported value can be retrieved by referring to the following formulas:
   $t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$
   $R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$

Figure 39. FMPI^{2}C timing diagram and measurement circuit



I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 65* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 65. I²S dynamic characteristics(1)

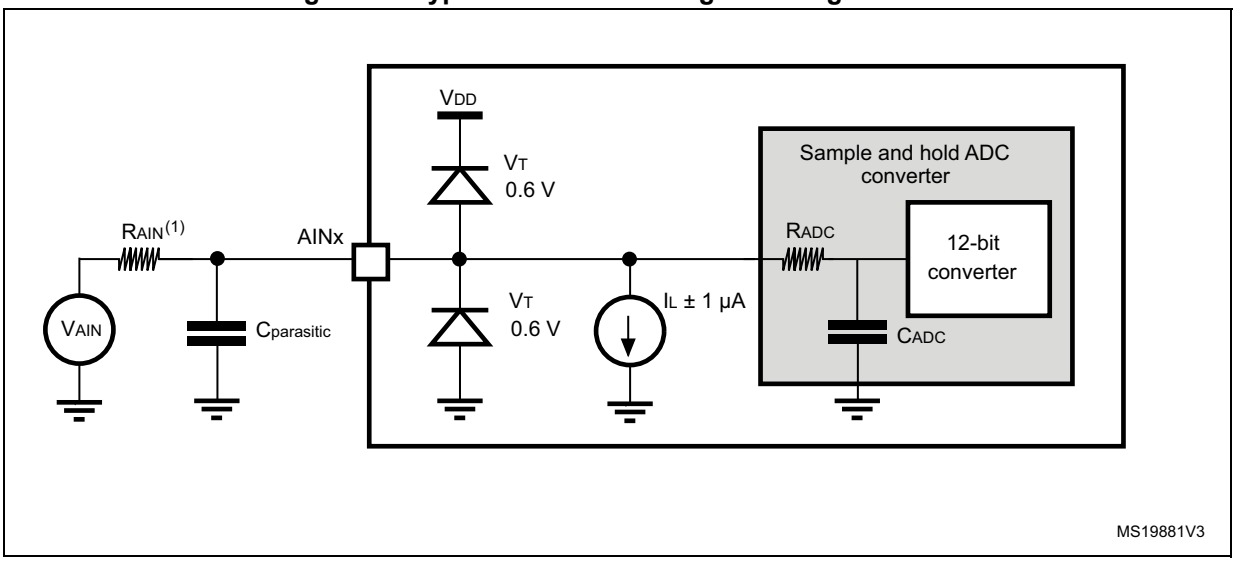
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	2	-	
$t_{h(WS)}$	WS hold time	Slave mode	0.5	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	0	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	15	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	2.5	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	6	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization, not tested in production.
2. The maximum value of 256xFs is 50 MHz (APB1 maximum frequency).

Note: Refer to the I2S section of RM0383 reference manual for more details on the sampling frequency (F_S).

*f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Figure 47. Typical connection diagram using the ADC



1. Refer to *Table 71* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.22 V_{BAT} monitoring characteristics

Table 79. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.23 Embedded reference voltage

The parameters given in *Table 80* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

Table 80. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

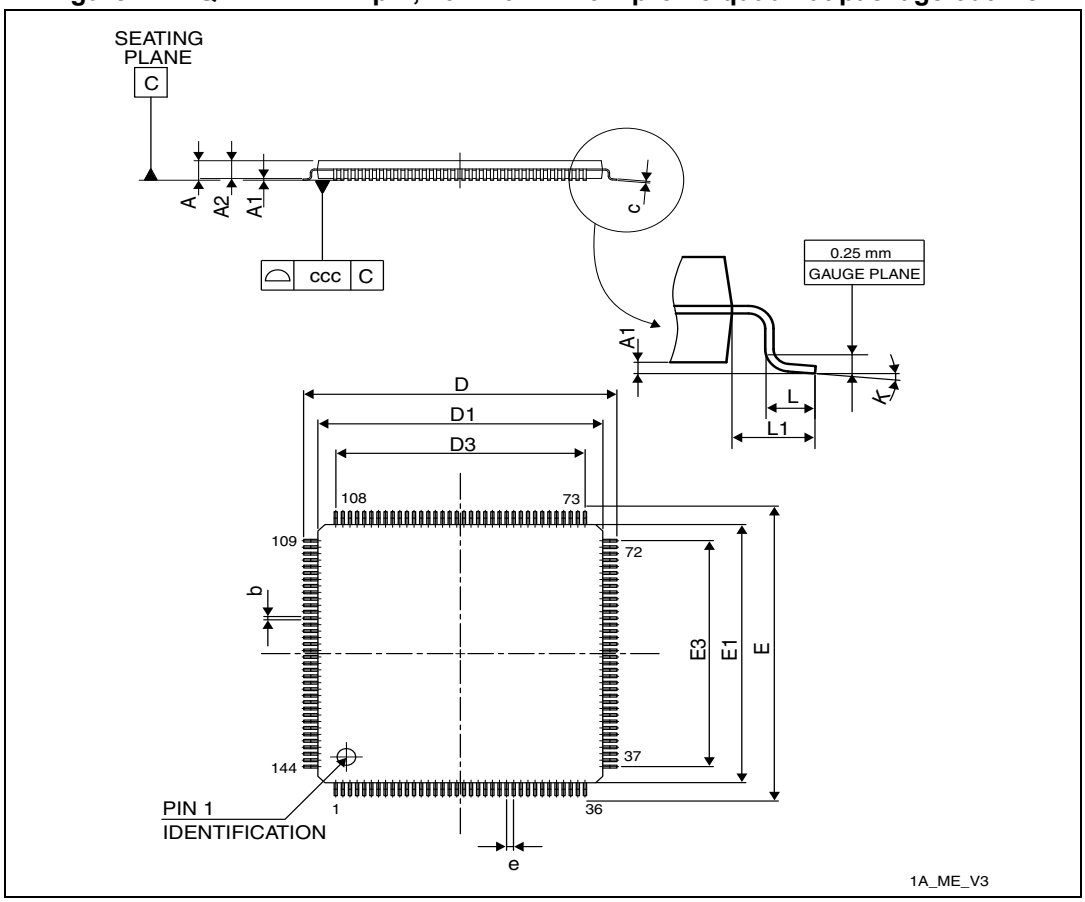
1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production

Table 81. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C V_{DDA} = 3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

7.5 LQFP144 package information

Figure 72. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.