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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 114 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-UFBGA |
| Supplier Device Package | 144-UFBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412zej3 |

The DMA can be used with the main peripherals:

- SPI and $I^2S$
- $I^2C$ and $I^2CFMP$
- USART
- General-purpose, basic and advanced-control timers TIMx
- SD/SDIO/MMC/eMMC host interface
- Quad-SPI
- ADC
- Digital Filter for sigma-delta modulator (DFSDM) with a separate stream for each filter.

## 3.11 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes a NOR/PSRAM memory controller. It features four Chip Select outputs supporting the following modes: SRAM, PSRAM and NOR Flash memory.

The main functions are:

- 8-,16-bit data bus width
- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 90 MHz.

### LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

## 3.12 Quad-SPI memory interface (QUAD-SPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting single, dual or quad-SPI Flash memories. It can work in direct mode through registers, external Flash status register polling mode and memory mapped mode. Up to 256 Mbyte of external Flash memory are mapped. They can be accessed in 8, 16 or 32-bit mode. Code execution is also supported. The opcode and the frame format are fully programmable. Communication can be performed either in single data rate or dual data rate.

## 3.13 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 81 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

## 3.14 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 21 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

## 3.15 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 100 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses and high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the $I^2S$ master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

Table 9. STM32F412xE/G pin definition (continued)

| Pin Number | | | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP64 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | - | - | 44 | M10 | K8 | 66 | PE13 | I/O | FT | - | TIM1_CH3, SPI4_MISO, SPI5_MISO, FSMC_D10/FSMC_DA10, EVENTOUT | - |
| - | - | - | 45 | M11 | L8 | 67 | PE14 | I/O | FT | - | TIM1_CH4, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, FSMC_D11/FSMC_DA11, EVENTOUT | - |
| - | - | - | 46 | M12 | M8 | 68 | PE15 | I/O | FT | - | TIM1_BKIN, FSMC_D12/FSMC_DA12, EVENTOUT | - |
| 21 | 29 | H4 | 47 | L10 | M9 | 69 | PB10 | I/O | FT | - | TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, I2S3_MCK, USART3_TX, I2CFMP1_SCL, SDIO_D7, EVENTOUT | - |
| - | - | - | - | K9 | M10 | 70 | PB11 | I/O | FT | - | TIM2_CH4, I2C2_SDA, I2S2_CKIN, USART3_RX, EVENTOUT | - |
| 22 | 30 | H3 | 48 | L11 | H7 | 71 | VCAP_1 | S | - | - | - | - |
| 23 | 31 | H2 | 49 | F12 | H6 | - | VSS | S | - | - | - | - |
| 24 | 32 | H1 | 50 | G12 | G7 | 72 | VDD | S | - | - | - | - |
| 25 | 33 | G3 | 51 | L12 | M11 | 73 | PB12 | I/O | FT | - | TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, SPI4_NSS/I2S4_WS, SPI3_SCK/I2S3_CK, USART3_CK, CAN2_RX, DFSDM1_DATIN1, FSMC_D13/FSMC_DA13, EVENTOUT | - |
| 26 | 34 | G2 | 52 | K12 | M12 | 74 | PB13 | I/O | FT | - | TIM1_CH1N, I2CFMP1_SMBA, SPI2_SCK/I2S2_CK, SPI4_SCK/I2S4_CK, USART3_CTS, CAN2_TX, DFSDM1_CKIN1, EVENTOUT | - |

**Table 29. Typical and maximum current consumption in Sleep mode - $V_{DD}$ = 1.7 V (continued)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in **Sleep mode** | All peripherals disabled, External clock, PLL ON(2), Flash deep power down | 100 | 2.9 | 3.51 | 4.14 | 4.90 | mA |
| | | | 84 | 2.4 | 2.83 | 3.46 | 4.16 | |
| | | | 64 | 1.7 | 2.08 | 2.59 | 3.18 | |
| | | | 50 | 1.4 | 1.77 | 2.23 | 2.84 | |
| | | | 25 | 1.0 | 1.37 | 1.88 | 2.50 | |
| | | | 20 | 1.3 | 1.37 | 1.88 | 2.50 | |
| | | All peripherals disabled, HSI, PLL OFF(2), Flash deep power down | 16 | 0.5 | 0.63 | 1.23 | 1.91 | |
| | | | 1 | 0.4 | 0.52 | 1.13 | 1.81 | |
| | | All peripherals disabled, External clock, PLL ON(2), Flash ON | 100 | 3.3 | 3.22 | 3.98 | 4.90 | |
| | | | 84 | 2.8 | 2.62 | 3.30 | 4.16 | |
| | | | 64 | 2.1 | 1.89 | 2.50 | 3.18 | |
| | | | 50 | 1.7 | 1.58 | 2.16 | 2.84 | |
| | | | 25 | 1.2 | 1.28 | 1.82 | 2.50 | |
| | | | 20 | 1.3 | 1.28 | 1.82 | 2.50 | |
| | | All peripherals disabled, HSI, PLL OFF(2), Flash ON | 16 | 0.8 | 0.88 | 1.36 | 1.91 | |
| | | | 1 | 0.7 | 0.77 | 1.26 | 1.81 | |

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

**Table 30. Typical and maximum current consumptions in Stop mode - $V_{DD}$ = 1.7 V**

| Symbol | Conditions | Parameter | Typ(1) | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD\_STOP}$ | Flash in Stop mode, all oscillators OFF, no independent watchdog | Main regulator usage | 121.1 | 168.0 | 648.7 | 1213.0 | µA |
| | | Low power regulator usage | 50.8 | 104.7 | 667.4 | 1328.0 | |
| | Flash in Deep power down mode, all oscillators OFF, no independent watchdog | Main regulator usage | 79.1 | 122.0 | 609.1 | 1181.0 | |
| | | Low power regulator usage | 22.4 | 74.7 | 631.9 | 1286.0 | |
| | | Low power low voltage regulator usage | 18.5 | 58.5 | 558.3 | 1145.0 | |

1. Based on characterization, not tested in production.

### On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off,
  - with only one peripheral clocked on,
  - scale 1 with $f_{HCLK}$ = 100 MHz,
  - scale 2 with $f_{HCLK}$ = 84 MHz,
  - scale 3 with $f_{HCLK}$ = 64 MHz.
- Ambient operating temperature is 25 °C and $V_{DD}$=3.3 V.

**Table 36. Peripheral current consumption**

| Peripheral | | $I_{DD}$ (Typ) | | | Unit |
|---|---|---|---|---|---|
| | | Scale 1 | Scale 2 | Scale 3 | |
| AHB1 | GPIOA | 1.84 | 1.75 | 1.55 | µA/MHz |
| | GPIOB | 1.90 | 1.80 | 1.61 | |
| | GPIOC | 1.77 | 1.67 | 1.50 | |
| | GPIOD | 1.67 | 1.58 | 1.42 | |
| | GPIOE | 1.75 | 1.67 | 1.48 | |
| | GPIOF | 1.65 | 1.56 | 1.39 | |
| | GPIOG | 1.65 | 1.56 | 1.39 | |
| | GPIOH | 0.62 | 0.57 | 0.53 | |
| | CRC | 0.26 | 0.25 | 0.22 | |
| | DMA1(1) | 1,71N+2,98 | 1,62N+2,87 | 1,45N+2,58 | |
| | DMA2(1) | 1,78N+2,62 | 1,70N+2.53 | 1,52N+2.26 | |
| AHB2 | RNG | 0.77 | 0.74 | 0.66 | |
| | USB_OTG_FS | 19.68 | 18.73 | 16.78 | |
| AHB3 | FSMC | 5.36 | 5.11 | 4.56 | |
| | QSPI | 9.99 | 9.51 | 8.53 | |

## Low-speed internal (LSI) RC oscillator

**Table 43. LSI oscillator characteristics (1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$ (2) | Frequency | 17 | 32 | 47 | kHz |
| $t_{su(LSI)}$ (3) | LSI oscillator startup time | - | 15 | 40 | µs |
| $I_{DD(LSI)}$ (3) | LSI oscillator power consumption | - | 0.4 | 0.6 | µA |

1. $V_{DD}$ = 3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design, not tested in production.

**Figure 32. $ACC_{LSI}$ versus temperature**

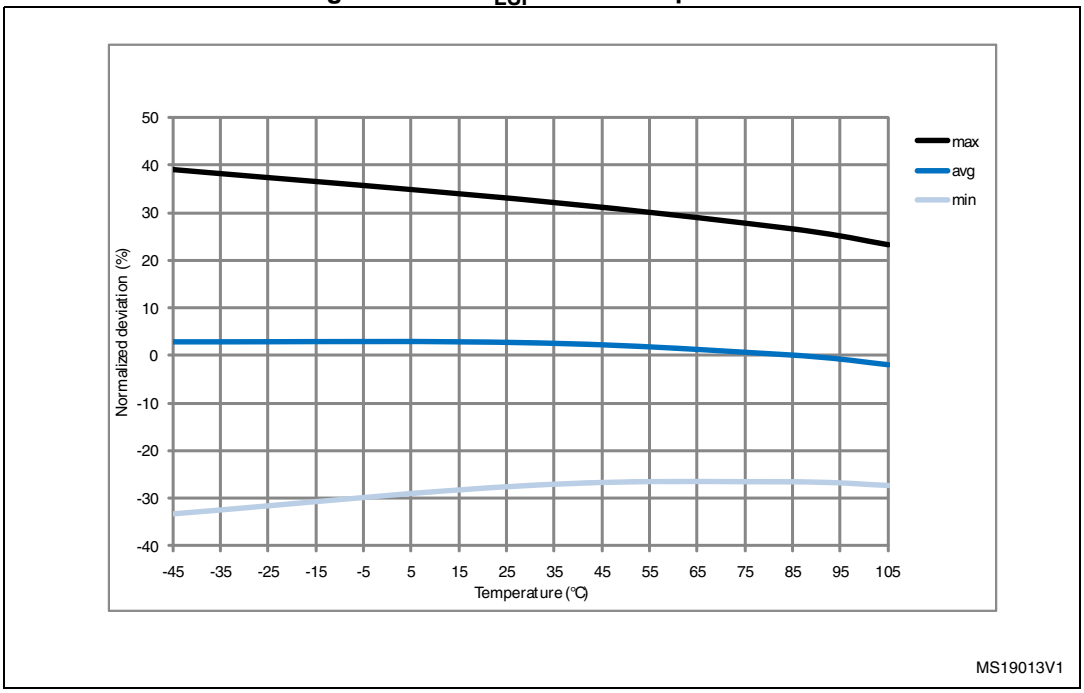
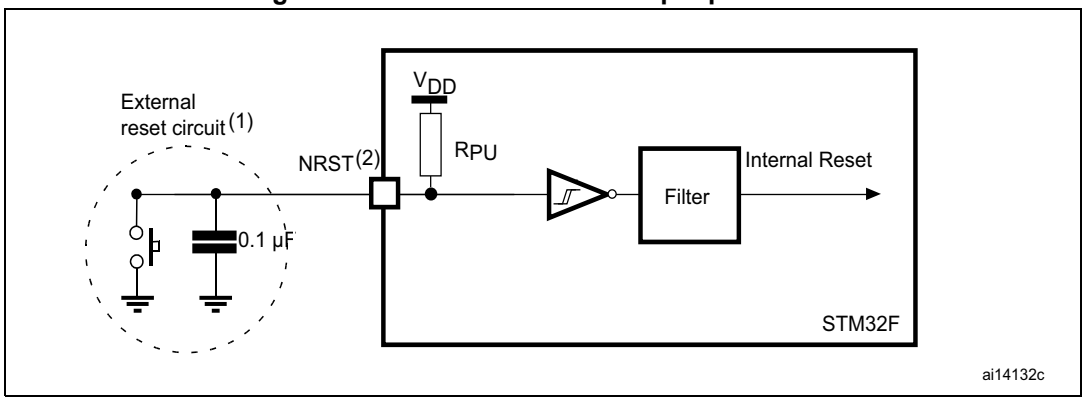


**Figure 37. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 59*. Otherwise the reset is not taken into account by the device.

## 6.3.18 TIM timer characteristics

The parameters given in *Table 60* are guaranteed by design.

Refer to *Section 6.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 60. TIMx characteristics(1)(2)**

| Symbol | Parameter | Conditions(3) | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 100 MHz | 1 | - | $t_{TIMxCLK}$ |
| | | | 11.9 | - | ns |
| | | AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 100 MHz | 1 | - | $t_{TIMxCLK}$ |
| | | | 11.9 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | $f_{TIMxCLK}$ = 100 MHz | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | | 0 | 50 | MHz |
| $Res_{TIM}$ | Timer resolution | | - | 16/32 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | $f_{TIMxCLK}$ = 100 MHz | 0.0119 | 780 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count with 32-bit counter | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 100 MHz | - | 51.1 | S |

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.
2. Guaranteed by design, not tested in production.
3. The maximum timer frequency on APB1 is 50 MHz and on APB2 is up to 100 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK >= 4x PCLKx.

## 6.3.19 Communications interfaces

### I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

The I²C characteristics are described in *Table 61*. Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

The I²C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more details about the complete solution, contact your local ST sales representative.

**Table 61. I²C characteristics**

| Symbol | Parameter | Standard mode I²C(1)(2) | | Fast mode I²C(1)(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | 3450(3) | 0 | 900(4) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 1000 | - | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 300 | - | 300 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | - | 0.6 | - | µs |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | - | 1.3 | - | µs |
| $t_{SP}$ | Pulse width of the spikes that are suppressed by the analog filter for standard fast mode | - | - | 50 | 120(5) | ns |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

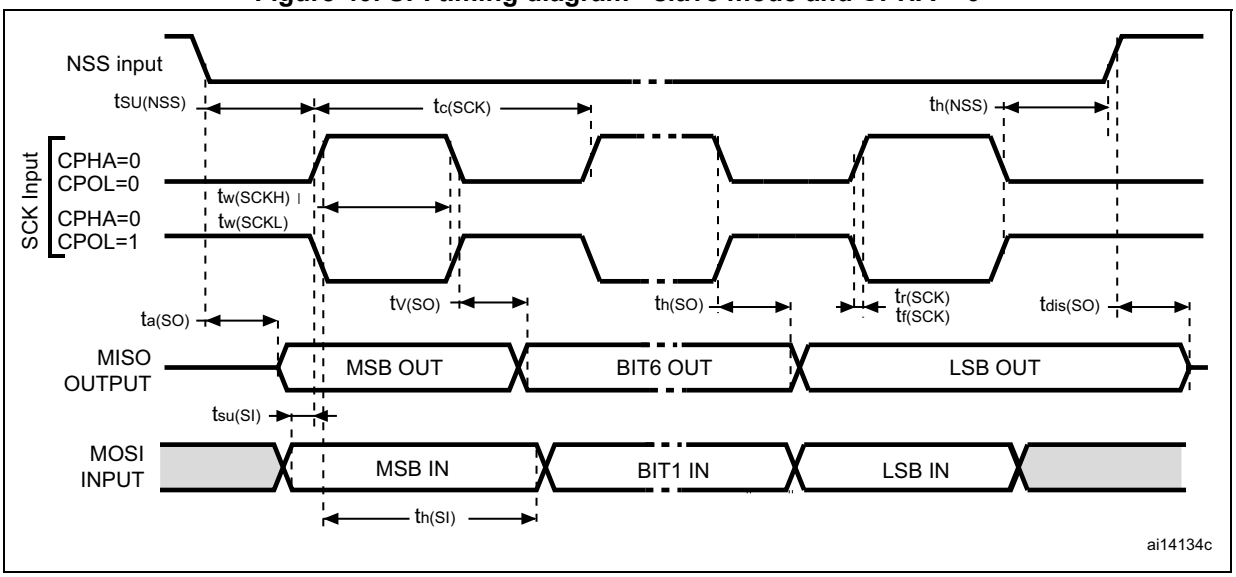
1. Guaranteed by design, not tested in production.
2. $f_{PCLK1}$ must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

**Table 64. SPI dynamic characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{a(SO)}$ | Data output access time | Slave mode | 7 | - | 21 | ns |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 5 | - | 12 | ns |
| $t_{v(SO)}$ | Data output valid time | Slave mode (after enable edge), 2.7 V < $V_{DD}$ < 3.6 V | - | 7.5 | 9 | ns |
| | | Slave mode (after enable edge), 1.7 V < $V_{DD}$ < 3.6 V | - | 7.5 | 14 | ns |
| $t_{h(SO)}$ | Data output hold time | Slave mode (after enable edge), 1.7 V < $V_{DD}$ < 3.6 V | 5.5 | - | - | ns |
| $t_{v(MO)}$ | Data output valid time | Master mode (after enable edge) | - | 3 | 8 | ns |
| $t_{h(MO)}$ | Data output hold time | Master mode (after enable edge) | 2 | - | - | ns |

1. Guaranteed by characterization, not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

**Figure 40. SPI timing diagram - slave mode and CPHA = 0**



### I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 65* for the I²S interface are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

**Table 65. I²S dynamic characteristics(1)**

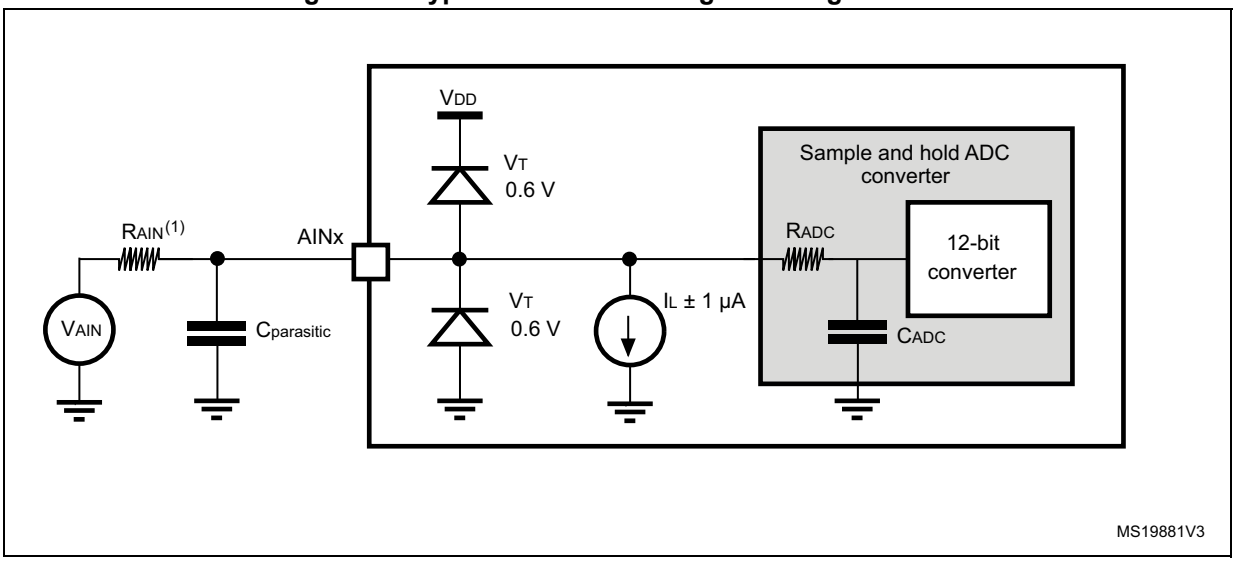
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCK}$ | I2S Main clock output | - | 256x8K | 256xFs(2) | MHz |
| $f_{CK}$ | I2S clock frequency | Master data: 32 bits | - | 64xFs | MHz |
| | | Slave data: 32 bits | - | 64xFs | |
| $D_{CK}$ | I2S clock frequency duty cycle | Slave receiver | 30 | 70 | % |
| $t_{v(WS)}$ | WS valid time | Master mode | - | 5 | ns |
| $t_{h(WS)}$ | WS hold time | Master mode | 0 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 2 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 0.5 | - | |
| $t_{su(SD\_MR)}$ | Data input setup time | Master receiver | 0 | - | |
| $t_{su(SD\_SR)}$ | | Slave receiver | 2 | - | |
| $t_{h(SD\_MR)}$ | Data input hold time | Master receiver | 0 | - | |
| $t_{h(SD\_SR)}$ | | Slave receiver | 2.5 | - | |
| $t_{v(SD\_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 15 | |
| $t_{v(SD\_MT)}$ | | Master transmitter (after enable edge) | - | 2.5 | |
| $t_{h(SD\_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 6 | - | |
| $t_{h(SD\_MT)}$ | | Master transmitter (after enable edge) | 0 | - | |

1. Guaranteed by characterization, not tested in production.
2. The maximum value of 256xFs is 50 MHz (APB1 maximum frequency).

*Note: Refer to the I2S section of RM0383 reference manual for more details on the sampling frequency ($F_S$).*

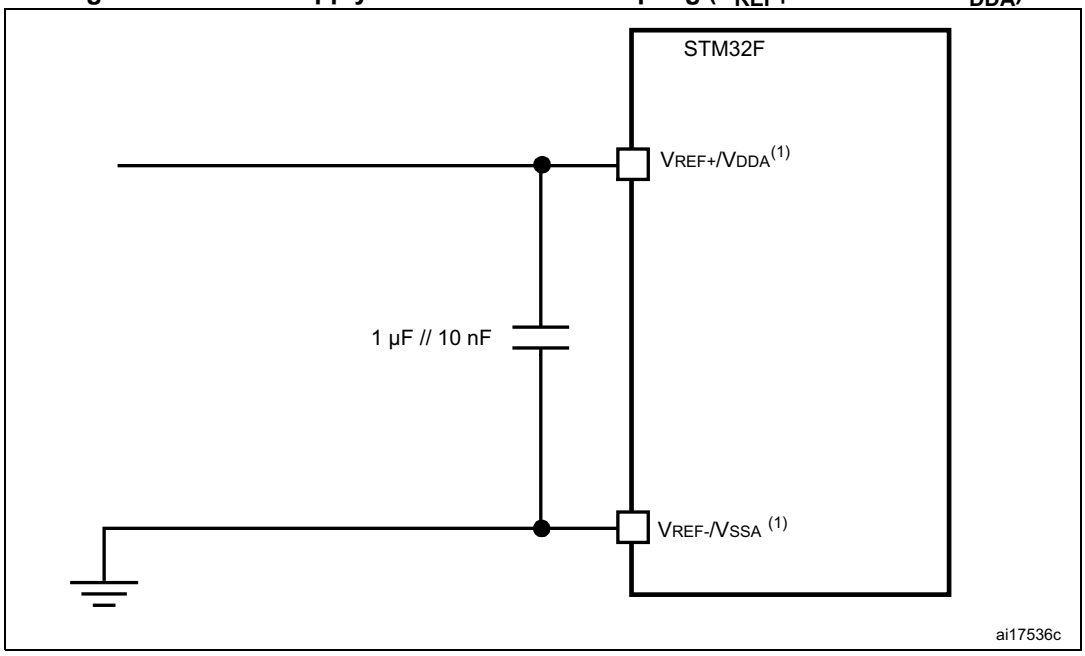
*$f_{MCK}$, $f_{CK}$, and $D_{CK}$ values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. $D_{CK}$ depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). $F_S$ maximum value is supported for each mode/condition.*

**Figure 47. Typical connection diagram using the ADC**




1. Refer to *Table 71* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

**Figure 49. Power supply and reference decoupling ($V_{REF+}$ connected to $V_{DDA}$)**




1. $V_{REF+}$ and $V_{REF-}$ inputs are both available on UFBGA100. $V_{REF+}$ is also available on LQFP100. When $V_{REF+}$ and $V_{REF-}$ are not available, they are internally connected to $V_{DDA}$ and $V_{SSA}$.

## 6.3.21 Temperature sensor characteristics

**Table 77. Temperature sensor characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$(1) | $V_{SENSE}$ linearity with temperature | - | ±1 | ±2 | °C |
| Avg_Slope(1) | Average slope | - | 2.5 | - | mV/°C |
| $V_{25}$(1) | Voltage at 25 °C | - | 0.76 | - | V |
| $t_{START}$(2) | Startup time | - | 6 | 10 | µs |
| $T_{S\_temp}$(2) | ADC sampling time when reading the temperature (1 °C accuracy) | 10 | - | - | µs |

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.

**Table 78. Temperature sensor calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$= 3.3 V | 0x1FFF 7A2C - 0x1FFF 7A2D |
| TS_CAL2 | TS ADC raw data acquired at temperature of 110 °C, $V_{DDA}$= 3.3 V | 0x1FFF 7A2E - 0x1FFF 7A2F |

### 6.3.24 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 82* for DFSDM are derived from tests performed under the ambient temperature, $f_{APB2}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 15: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x VDD

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM_CKINy, DFSDM_DATINy, DFSDM_CKOUT for DFSDM).

**Table 82. DFSDM characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{DFSDMCLK}$ | DFSDM clock | - | - | - | $f_{SYSCLK}$ | MHz |
| $f_{CKIN}$ ($1/T_{CKIN}$) | Input clock frequency | SPI mode (SITP[1:0] = 01) | - | - | 20 ($f_{DFSDMCLK}/4$) | |
| $f_{CKOUT}$ | Output clock frequency | - | - | - | 20 | MHz |
| $DuCy_{CKOUT}$ | Output clock frequency duty cycle | - | 30 | 50 | 75 | % |
| $t_{wh(CKIN)}$ $t_{wl(CKIN)}$ | Input clock high and low time | SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0) | $T_{CKIN}/2-0.5$ | $T_{CKIN}/2$ | - | ns |
| $t_{su}$ | Data input setup time | SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0) | 1 | - | - | |
| $t_h$ | Data input hold time | SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0) | 1 | - | - | |
| $T_{Manchester}$ | Manchester data period (recovered clock period) | Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0) | (CKOUT DIV+1) x $T_{DFSDMCLK}$ | - | (2 x CKOUTDIV) x $T_{DFSDMCLK}$ | |

1. Data based on characterization results, not tested in production.

**Table 83. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $2T_{HCLK} – 1$ | $2\ T_{HCLK} + 0.5$ | ns |
| $t_{v(NOE\_NE)}$ | FSMC_NEx low to FSMC_NOE low | 0 | 1 | |
| $t_{w(NOE)}$ | FSMC_NOE low time | $2T_{HCLK}$ - 1.5 | $2T_{HCLK}$ | |
| $t_{h(NE\_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | 0 | - | |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 1.5 | |
| $t_{h(A\_NOE)}$ | Address hold time after FSMC_NOE high | 0 | - | |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 0.5 | |
| $t_{h(BL\_NOE)}$ | FSMC_BL hold time after FSMC_NOE high | 0 | - | |
| $t_{su(Data\_NE)}$ | Data to FSMC_NEx high setup time | $T_{HCLK}$ - 1 | - | |
| $t_{su(Data\_NOE)}$ | Data to FSMC_NOEx high setup time | $T_{HCLK}$ - 1 | - | |
| $t_{h(Data\_NOE)}$ | Data hold time after FSMC_NOE high | 0 | - | |
| $t_{h(Data\_NE)}$ | Data hold time after FSMC_NEx high | 0 | - | |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | - | 0 | |
| $t_{w(NADV)}$ | FSMC_NADV low time | - | $T_{HCLK} + 0.5$ | |

1. $C_L$ = 30 pF.
2. Based on characterization, not tested in production.

**Table 84. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $7T_{HCLK}$ - 1 | $7T_{HCLK} + 0.5$ | ns |
| $t_{w(NOE)}$ | FSMC_NWE low time | $5T_{HCLK} – 1.5$ | $5T_{HCLK}$ | |
| $t_{w(NWAIT)}$ | FSMC_NWAIT low time | $T_{HCLK} – 0.5$ | - | |
| $t_{su(NWAIT\_NE)}$ | FSMC_NWAIT valid before FSMC_NEx high | $5T_{HCLK}$ -1 | - | |
| $t_{h(NE\_NWAIT)}$ | FSMC_NEx hold time after FSMC_NWAIT invalid | $4T_{HCLK} + 1$ | - | |

1. $C_L$ = 30 pF.
2. Based on characterization, not tested in production.

1. $C_L$ = 30 pF.
2. Based on characterization, not tested in production.

**Table 86. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $8T_{HCLK}$ - 1 | $8T_{HCLK}$ + 0.5 | ns |
| $t_{w(NWE)}$ | FSMC_NWE low time | $6T_{HCLK}$ + 0.5 | $6T_{HCLK}$ + 1 | |
| $t_{su(NWAIT\_NE)}$ | FSMC_NWAIT valid before FSMC_NEx high | $6T_{HCLK}$ + 0.5 | - | |
| $t_{h(NE\_NWAIT)}$ | FSMC_NEx hold time after FSMC_NWAIT invalid | $4T_{HCLK}$ + 1 | - | |

1. $C_L$ = 30 pF.
2. Based on characterization, not tested in production.

**Figure 52. Asynchronous multiplexed PSRAM/NOR read waveforms**

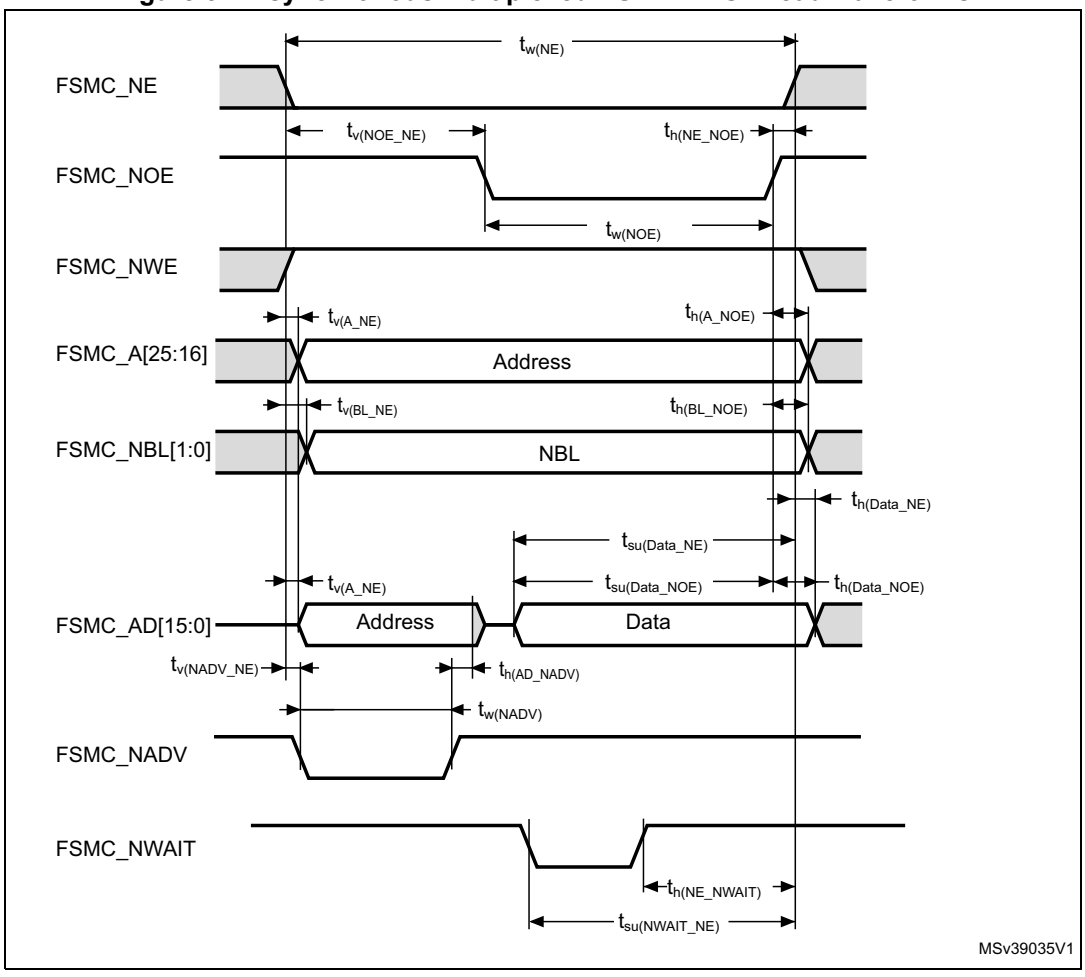
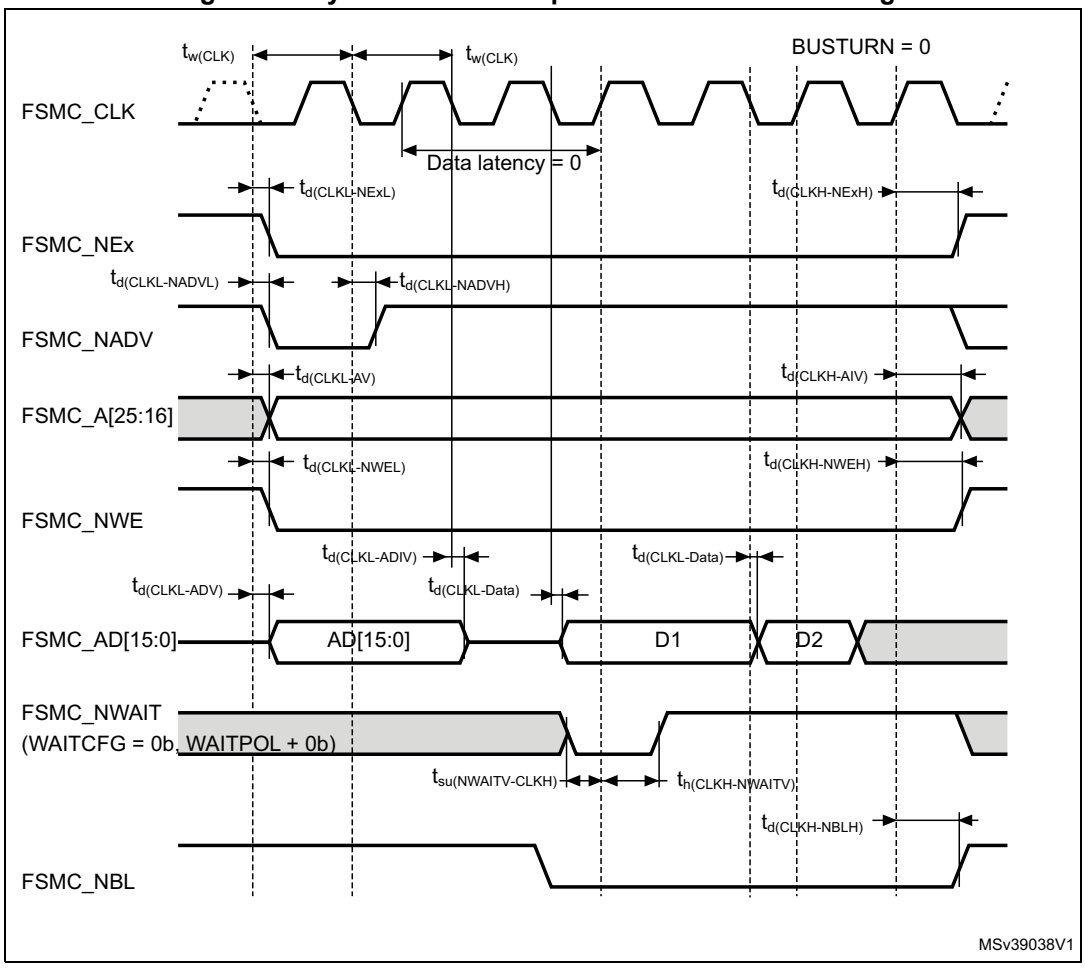


**Figure 55. Synchronous multiplexed PSRAM write timings**

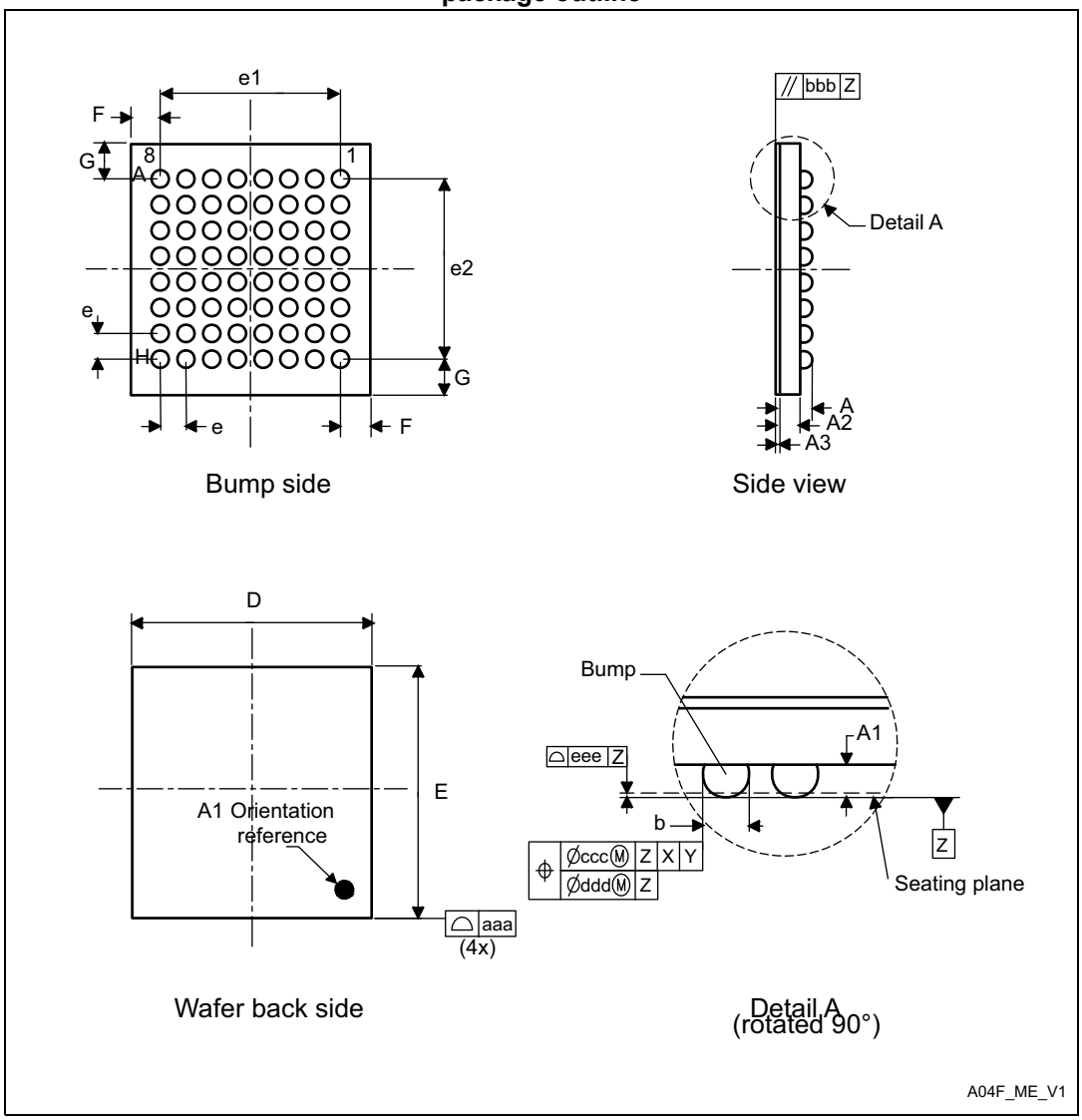


# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

## 7.1 WLCSP64 package information

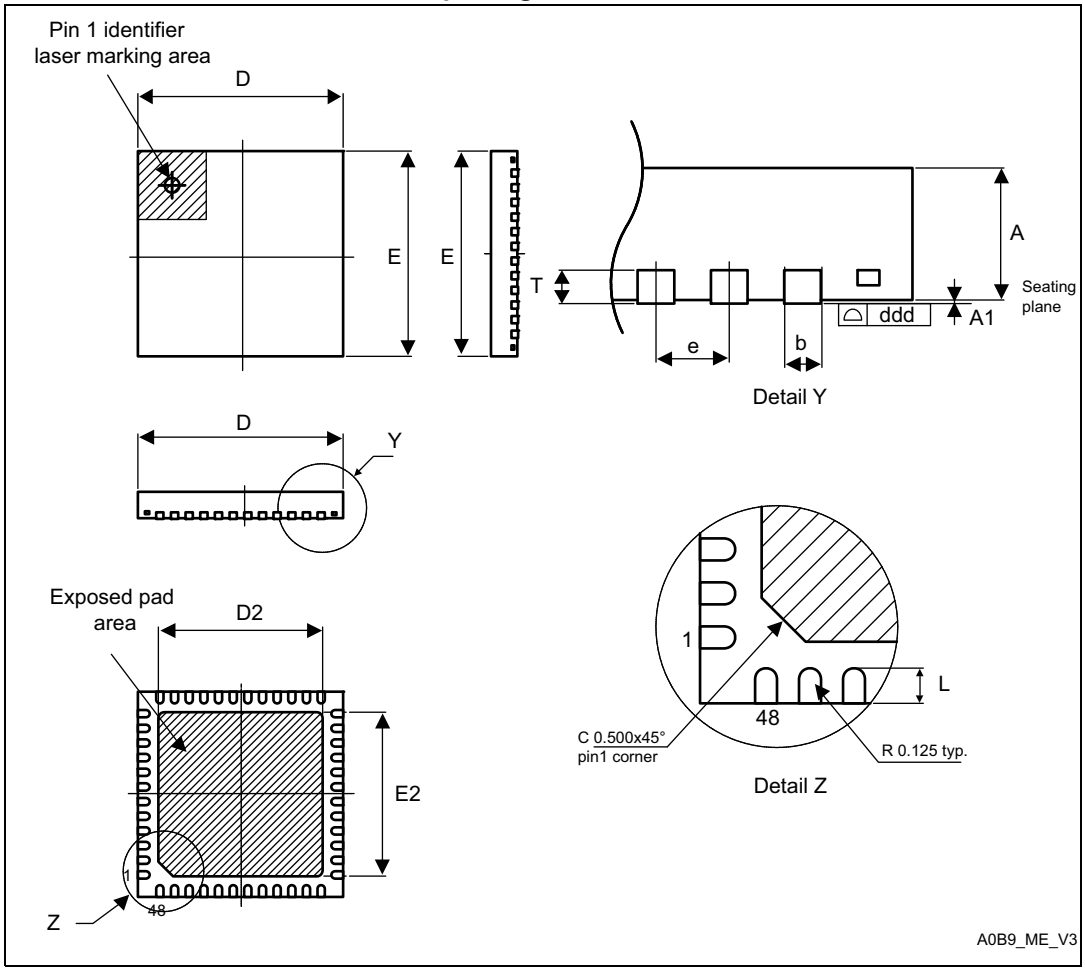
**Figure 60. WLCSP64 - 64-pin, 3.658 x 3.686 mm, 0.4 mm pitch wafer level chip scale package outline**




1. Drawing is not to scale.

## 7.2 UFQFPN48 package information

**Figure 63. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline**




1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

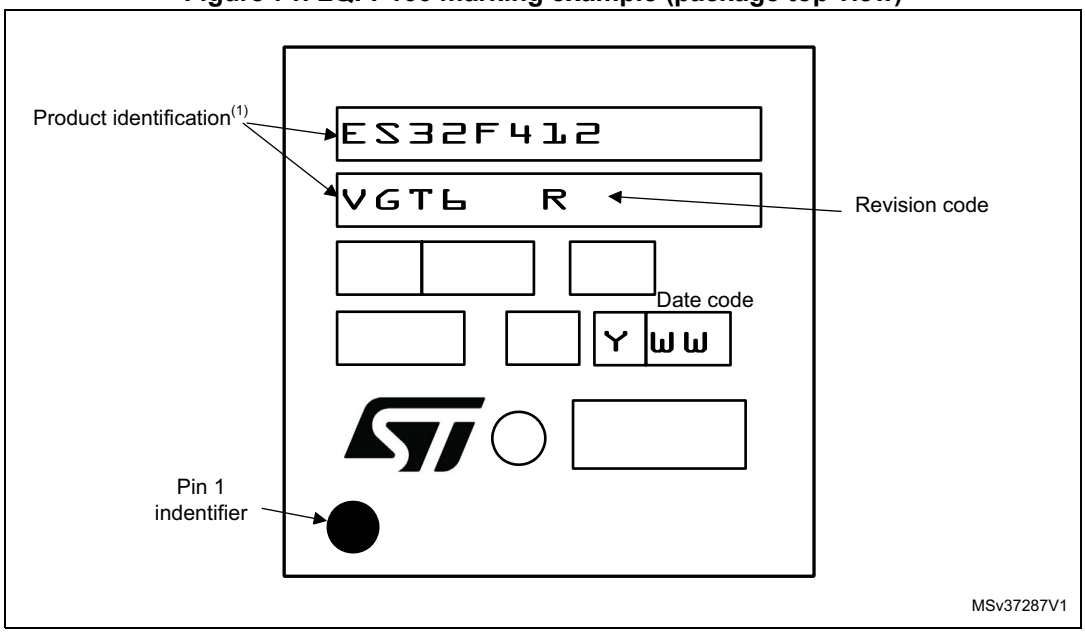
**Table 100. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| D | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| E | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| D2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |

### Device marking for LQFP100

The following figure gives an example of topside marking and pin 1 position identifier location.

**Figure 71. LQFP100 marking example (package top view)**

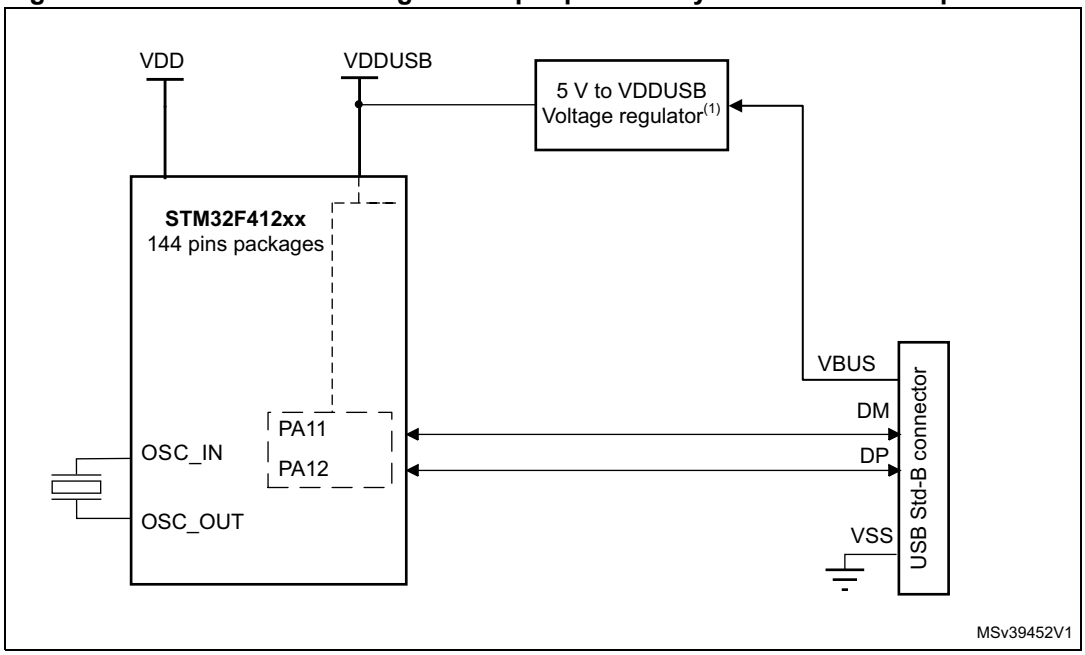



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

# Appendix B Application block diagrams

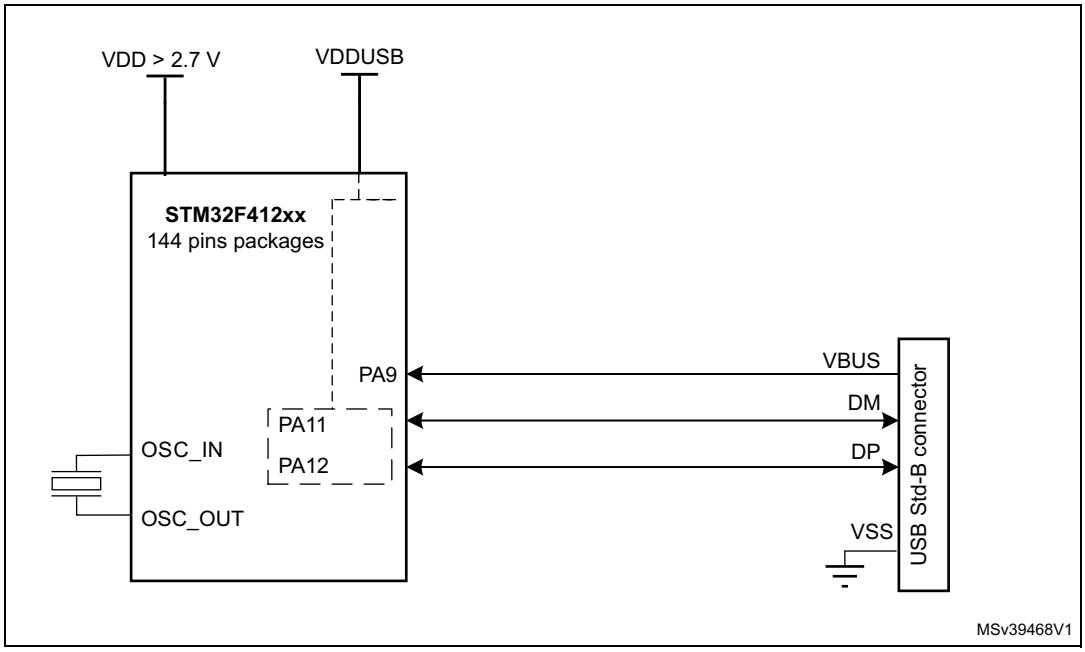
## B.1 USB OTG full speed (FS) interface solutions

**Figure 81. USB controller configured as peripheral-only and used in Full speed mode**




1. External voltage regulator only needed when building a $V_{BUS}$ powered device.

**Figure 82. USB peripheral-only Full speed mode with direct connection for VBUS sense**




1. External voltage regulator only needed when building a $V_{BUS}$ powered device.