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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412zej6

2.1 Compatibility with STM32F4 series

The STM32F412xE/G are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F412xE/G can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

Figure 1. Compatible board design for LQFP100 package

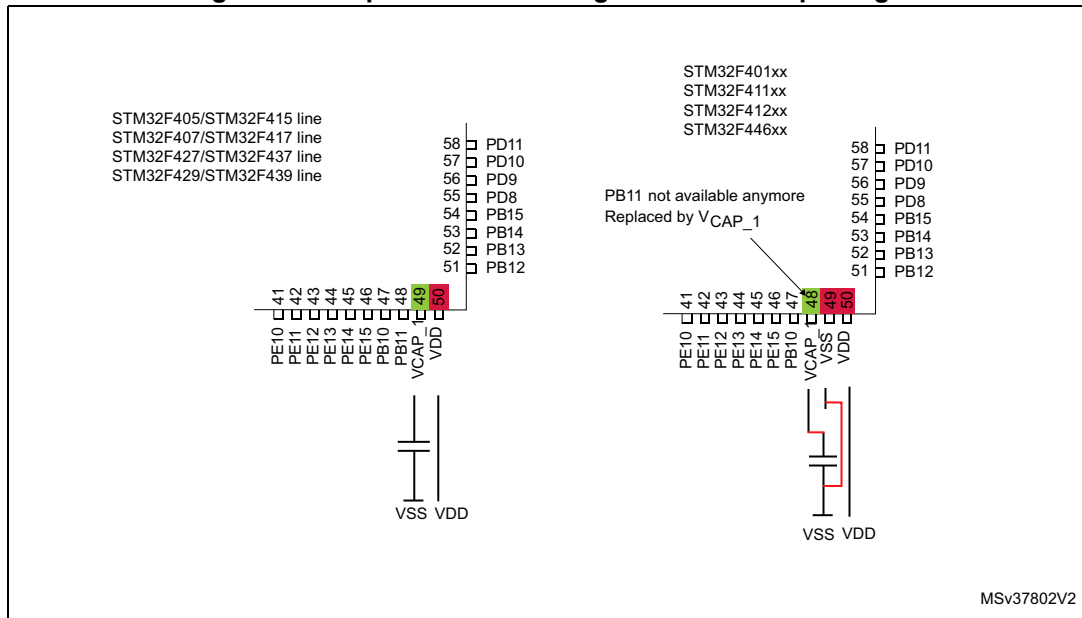
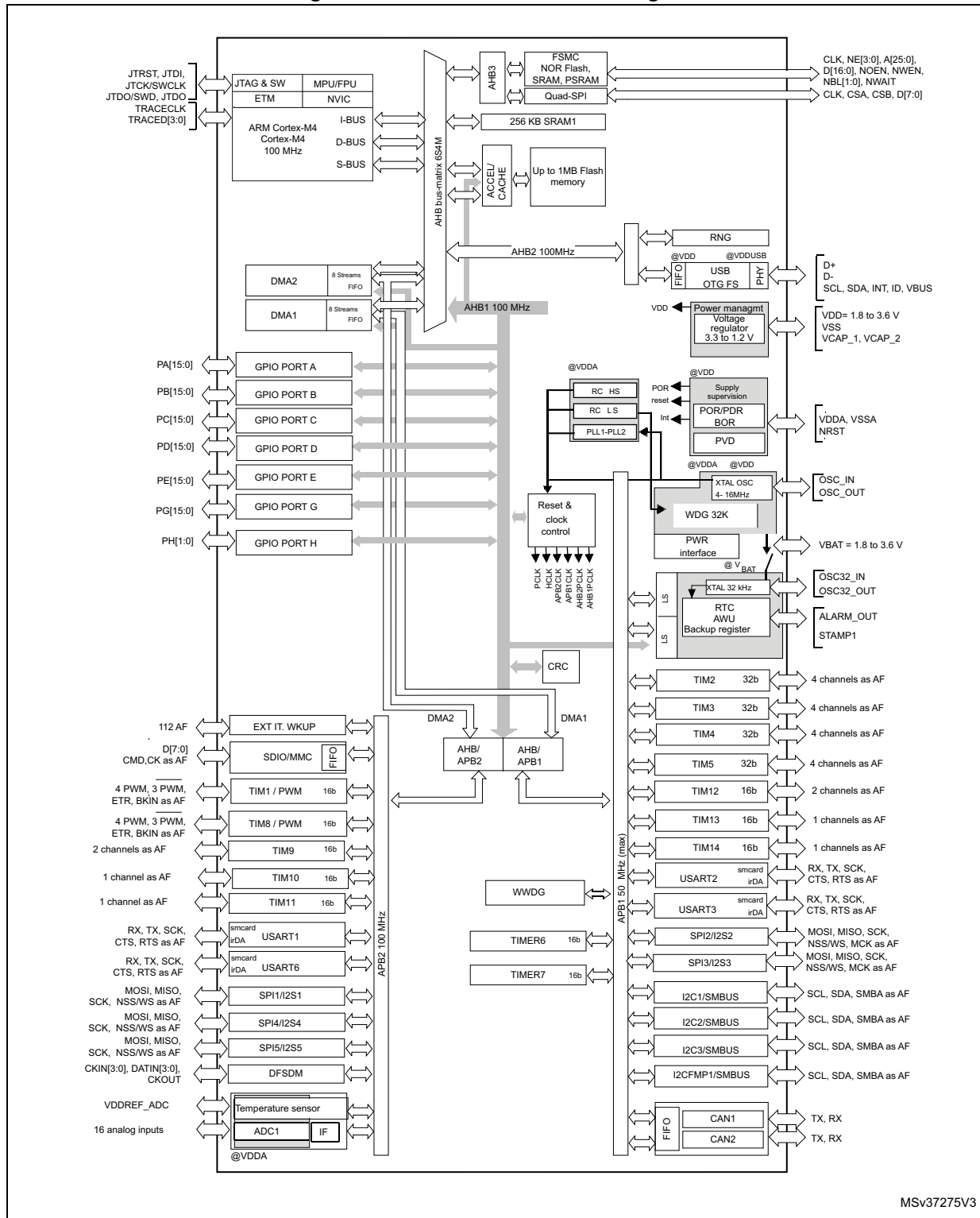


Figure 4. STM32F412xE/G block diagram



MSv37275V3

1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 50 MHz.

3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 byte and the whole 4 Gbyte of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.5 Embedded Flash memory

The devices embed up to 1 Mbyte of Flash memory available for storing programs and data.

The Flash user area can be protected against reading by an entrusted code (Read Protection, RDP) with different protection levels.

The flash user sectors can also be individually protected against write operation.

Furthermore the proprietary readout protection (PCROP) can also individually protect the flash user sectors against D-bus read accesses.

(Additional information can be found in the product reference manual).

To optimize the power consumption the Flash memory can also be switched off in Run or in Sleep mode (see [Section 3.21: Low-power modes](#)).

Two modes are available: Flash in Stop mode or in DeepSleep mode (trade off between power saving and startup time).

Before disabling the Flash, the code must be executed from the internal RAM.

3.6 One-time programmable bytes

A one-time programmable area is available with 16 OTP blocks of 32 bytes. Each block can be individually locked

(Additional information can be found in the product reference manual)

3.7 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C and I²C/FMP
- USART
- General-purpose, basic and advanced-control timers TIMx
- SD/SDIO/MMC/eMMC host interface
- Quad-SPI
- ADC
- Digital Filter for sigma-delta modulator (DFSDM) with a separate stream for each filter.

3.11 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes a NOR/PSRAM memory controller. It features four Chip Select outputs supporting the following modes: SRAM, PSRAM and NOR Flash memory.

The main functions are:

- 8-, 16-bit data bus width
- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 90 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.12 Quad-SPI memory interface (QUAD-SPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting single, dual or quad-SPI Flash memories. It can work in direct mode through registers, external Flash status register polling mode and memory mapped mode. Up to 256 Mbyte of external Flash memory are mapped. They can be accessed in 8, 16 or 32-bit mode. Code execution is also supported. The opcode and the frame format are fully programmable. Communication can be performed either in single data rate or dual data rate.

The DFSDM peripheral supports:

- 4 multiplexed input digital serial channels:
 - configurable SPI interface to connect various SD modulator(s)
 - configurable Manchester coded 1 wire interface support
 - PDM (Pulse Density Modulation) microphone input support
 - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
 - clock output for SD modulator(s): 0...20 MHz
- alternative inputs from 4 internal digital parallel channels (up to 16 bit input resolution):
 - internal sources: device memory data streams (DMA)
- 2 digital filter modules with adjustable digital signal processing:
 - Sinc^x filter: filter order/type (1...5), oversampling ratio (up to 1...1024)
 - integrator: oversampling ratio (1...256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by
 - software trigger
 - internal timers
 - external events
 - start-of-conversion synchronously with first digital filter module (DFSDM1FLT0)
- analog watchdog feature:
 - low value and high value data threshold registers
 - dedicated configurable Sinc^x digital filter (order = 1...3, oversampling ratio = 1...32)
 - input from digital output data or from selected input digital serial channels
 - continuous monitoring independently from standard conversion
- short circuit detector to detect saturated analog input values (bottom and top range):
 - up to 8-bit counter to detect 1...256 consecutive 0's or 1's on serial data stream
 - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
 - storage of minimum and maximum values of final conversion data
 - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit input serial channel clock absence
- “regulator” or injected” conversions:
 - “regular” conversions can be requested at any time or even in continuous mode without having any impact on the timing of “injected” conversions
 - “injected” conversions for precise timing and with high conversion priority.

3.30 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC/eMMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.31 Controller area network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOs with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 byte of SRAM are allocated for each CAN.

3.32 Universal serial bus on-the-go full-speed (USB_OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The Battery Charging Detection (BCD) can detect and identify the type of port, it is connected to (standard USB or charger). The type of charging is also detected: Dedicated Charging Port (DCP), Charging Downstream Port (CDP) and Standard Downstream Port (SDP). Some packages provide a dedicated USB power rail allowing a different supply for the USB and for the rest of the chip. For instance the chip can be powered with the minimum specified supply and the USB running at the level defined by the standard. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- Link Power Management (LPM)
- Battery Charging Detection (BCD) supporting DCP, CDP and SDP

3.33 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.34 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

3.35 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

3.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value. Refer to the reference manual for additional information.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.37 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Table 9. STM32F412xE/G pin definition

Pin Number							Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WL CSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	1	B2	A3	1	PE2	I/O	FT	-	TRACECLK, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, QUADSPI_BK1_IO2, FSMC_A23, EVENTOUT	-
-	-	-	2	A1	A2	2	PE3	I/O	FT	-	TRACED0, FSMC_A19, EVENTOUT	-
-	-	-	3	B1	B2	3	PE4	I/O	FT	-	TRACED1, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, DFSDM1_DATIN3, FSMC_A20, EVENTOUT	-
-	-	-	4	C2	B3	4	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SPI5_MISO, DFSDM1_CKIN3, FSMC_A21, EVENTOUT	-
-	-	-	5	D2	B4	5	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, FSMC_A22, EVENTOUT	-
1	1	B7	6	E2	C2	6	VBAT	S	-	-	-	VBAT
2	2	B8	7	C1	A1	7	PC13	I/O	FT	(2)(3)	EVENTOUT	TAMP_1
3	3	C8	8	D1	B1	8	PC14- OSC32_IN	I/O	FT	(2)(3) (4)	EVENTOUT	OSC32_IN
4	4	C7	9	E1	C1	9	PC15- OSC32_ OUT	I/O	FT	(2)(4)	EVENTOUT	OSC32_ OUT
-	-	-	-	-	C3	10	PF0	I/O	FT	-	I2C2_SDA, FSMC_A0, EVENTOUT	-
-	-	-	-	-	C4	11	PF1	I/O	FT	-	I2C2_SCL, FSMC_A1, EVENTOUT	-
-	-	-	-	-	D4	12	PF2	I/O	FT	-	I2C2_SMBA, FSMC_A2, EVENTOUT	-
-	-	-	-	-	E2	13	PF3	I/O	FT	-	TIM5_CH1, FSMC_A3, EVENTOUT	-
-	-	-	-	-	E3	14	PF4	I/O	FT	-	TIM5_CH2, FSMC_A4, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

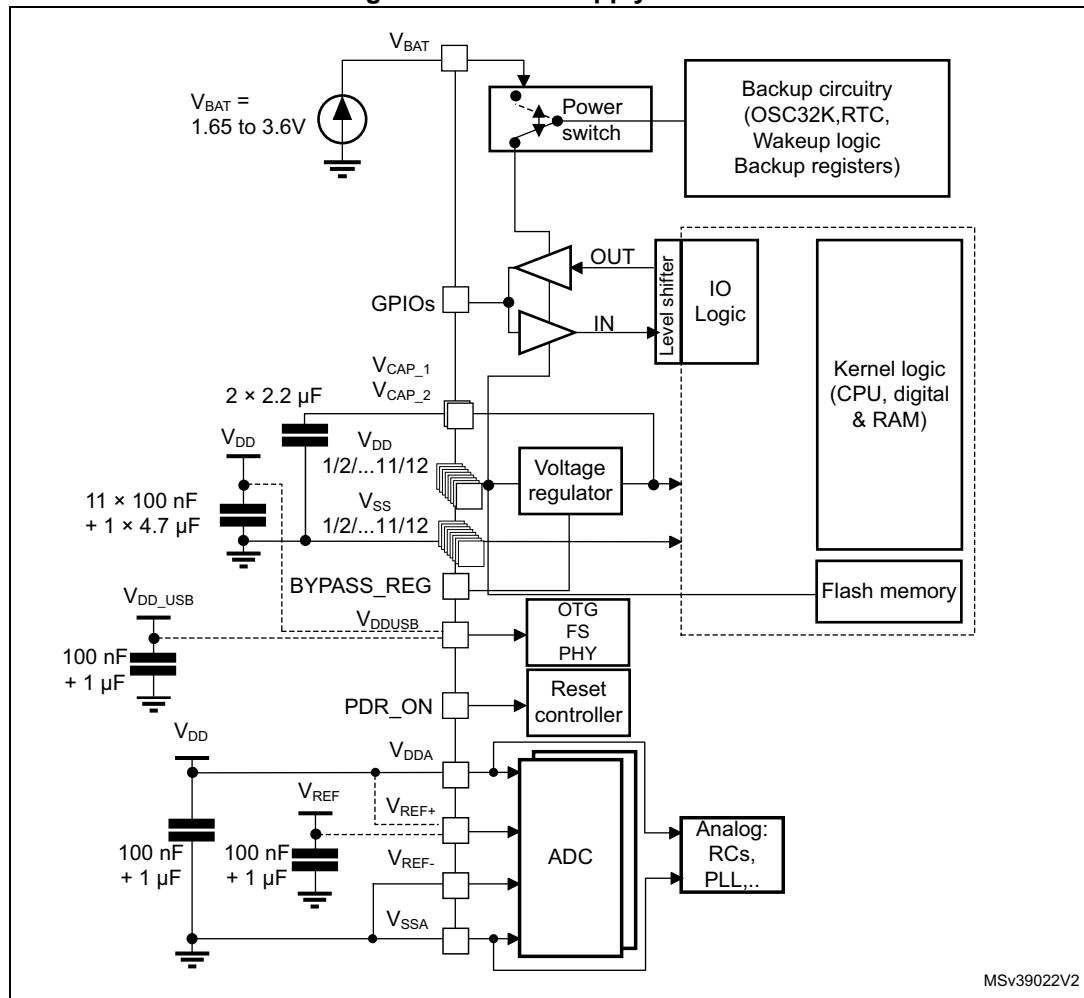
Pin Number							Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
16	22	H6	31	L4	L3	42	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, I2S2_MCK, TIM13_CH1, QUADSPI_BK2_IO0, SDIO_CMD, EVENTOUT	ADC1_6
17	23	E5	32	M4	M3	43	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, QUADSPI_BK2_IO1, EVENTOUT	ADC1_7
-	24	E4	33	K5	J4	44	PC4	I/O	FT	-	I2S1_MCK, QUADSPI_BK2_IO2, FSMC_NE4, EVENTOUT	ADC1_14
-	25	G5	34	L5	K4	45	PC5	I/O	FT	-	I2CFMP1_SMBA, USART3_RX, QUADSPI_BK2_IO3, FSMC_NOE, EVENTOUT	ADC1_15
18	26	H5	35	M5	L4	46	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI5_SCK/I2S5_CK, EVENTOUT	ADC1_8
19	27	F4	36	M6	M4	47	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, SPI5_NSS/I2S5_WS, DFSDM1_DATIN0, QUADSPI_CLK, EVENTOUT	ADC1_9
20	28	G4	37	L6	J5	48	PB2	I/O	FT	-	DFSDM1_CKIN0, QUADSPI_CLK, EVENTOUT	BOOT1
-	-	-	-	-	M5	49	PF11	I/O	FT	-	TIM8_ETR, EVENTOUT	-
-	-	-	-	-	L5	50	PF12	I/O	FT	-	TIM8_BKIN, FSMC_A6, EVENTOUT	-
-	-	-	-	-	-	51	VSS	S	-	-	-	-
-	-	-	-	-	G5	52	VDD	S	-	-	-	-
-	-	-	-	-	K5	53	PF13	I/O	FT	-	I2CFMP1_SMBA, FSMC_A7, EVENTOUT	-

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WL CSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	51	C3	78	B11	B11	111	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, QUADSPI_BK1_IO1, SDIO_D2, EVENTOUT	-
-	52	B3	79	C10	B10	112	PC11	I/O	FT	-	I2S3ext_SD, SPI3_MISO, USART3_RX, QUADSPI_BK2_NCS, FSMC_D2, SDIO_D3, EVENTOUT	-
-	53	A3	80	B10	C10	113	PC12	I/O	FT	-	SPI3_MOSI/I2S3_SD, USART3_CK, FSMC_D3, SDIO_CK, EVENTOUT	-
-	-	-	81	C9	E10	114	PD0	I/O	FT	-	CAN1_RX, FSMC_D2/FSMC_DA2, EVENTOUT	-
-	-	-	82	B9	D10	115	PD1	I/O	FT	-	CAN1_TX, FSMC_D3/FSMC_DA3, EVENTOUT	-
-	54	A4	83	C8	E9	116	PD2	I/O	FT	-	TIM3_ETR, FSMC_NWE, SDIO_CMD, EVENTOUT	-
-	-	-	84	B8	D9	117	PD3	I/O	FT	-	TRACED1, SPI2_SCK/I2S2_CK, DFSDM1_DATIN0, USART2_CTS, QUADSPI_CLK, FSMC_CLK, EVENTOUT	-
-	-	-	85	B7	C9	118	PD4	I/O	FT	-	DFSDM1_CKIN0, USART2_RTS, FSMC_NOE, EVENTOUT	-
-	-	-	86	A6	B9	119	PD5	I/O	FT	-	USART2_TX, FSMC_NWE, EVENTOUT	-
-	-	-	-	-	E7	120	VSS	S	-	-	-	-
-	-	-	-	-	F7	121	VDD	S	-	-	-	-
-	-	-	87	B6	A8	122	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, DFSDM1_DATIN1, USART2_RX, FSMC_NWAIT, EVENTOUT	-

6.1.6 Power supply scheme

Figure 21. Power supply scheme



1. To connect PDR_ON pin, refer to Section: Power supply supervisor.
2. The 4.7 μF ceramic capacitor must be connected to one of the V_{DD} pin.
3. VCAP_2 pad is only available on 100-pin and 144-pin packages.
4. $V_{DDA}=V_{DD}$ and $V_{SSA}=V_{SS}$.
5. V_{DDUSB} is a dedicated independent USB power supply for the on-chip full-speed OTG PHY module and associated DP/DM GPIOs. V_{DDUSB} value does not depend on the V_{DD} and V_{DDA} values, but it must be the last supply to be provided and the first to disappear.

Caution: Each power supply pair (for example V_{DD}/V_{SS} , V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

Table 23. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- $V_{DD} = 1.7\text{ V}$

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾				Unit
				T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C		
I _{DD}	Supply current in Run mode	External clock, PLL ON, all peripherals enabled ⁽²⁾⁽³⁾	100	26.9	28.78	29.86	31.30	mA	
			84	21.6	23.14	23.93	24.89		
			64	15.0	16.08	16.70	17.46		
			50	11.8	12.74	13.33	14.07		
			25	6.3	7.13	7.69	8.30		
			20	5.5	6.09	6.64	7.30		
		HSI, PLL OFF, all peripherals enabled ⁽²⁾	16	3.9	4.20	4.78	4.49		
			1	0.9	0.98	1.50	2.20		
		External clock, PLL ON ⁽⁴⁾ all peripherals disabled ⁽²⁾	100	12.7	13.82	14.71	15.76		
			84	10.3	11.20	11.97	12.96		
			64	7.2	7.87	8.57	9.41		
			50	5.7	6.33	7.02	7.87		
			25	3.2	3.77	4.38	5.13		
			20	2.9	3.31	3.93	4.69		
		HSI, PLL OFF, all peripherals disabled ⁽²⁾	16	2.1	2.25	2.83	3.56		
			1	0.7	0.83	1.42	2.12		

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.
4. Refer to [Table 44](#) and RM0383 for the possible PLL VCO setting

Table 40. HSE 4-26 MHz oscillator characteristics⁽¹⁾

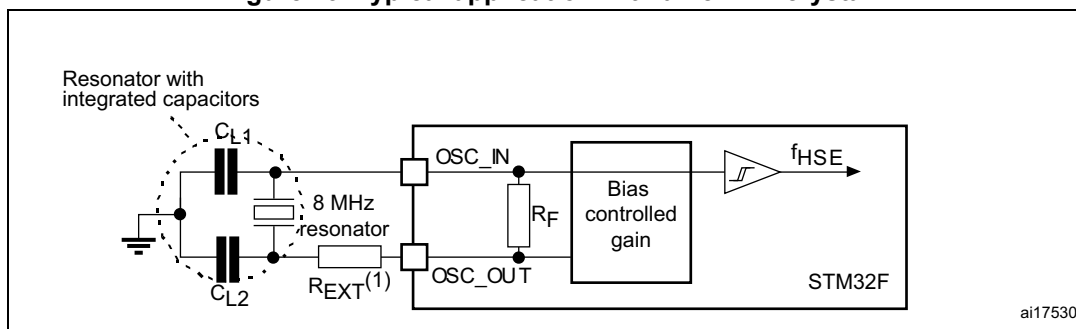
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	-	26	MHz
R_F	Feedback resistor		-	200	-	k Ω
I_{DD}	HSE current consumption	$V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=5\text{ pF @25 MHz}$	-	450	-	μA
		$V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=10\text{ pF @25 MHz}$	-	530	-	
$ACC_{HSE}^{(2)}$	HSE accuracy	-	-500	-	500	ppm
$G_{m_crit_max}$	Maximum critical crystal g_m	Startup	-	-	1	mA/V
$t_{SU(HSE)}^{(3)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design, not tested in production.
2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 29](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 29. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 41](#). In the application, the resonator and the load capacitors have to be placed as close as

Table 49. Flash memory programming with V_{PP} voltage

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t _{prog}	Double word programming	T _A = 0 to +40 °C V _{DD} = 3.3 V V _{PP} = 8.5 V	-	16	100 ⁽²⁾	μs
t _{ERASE16KB}	Sector (16 KB) erase time		-	230	-	ms
t _{ERASE64KB}	Sector (64 KB) erase time		-	490	-	
t _{ERASE128KB}	Sector (128 KB) erase time		-	875	-	
t _{ME}	Mass erase time		-	6.9	-	s
V _{prog}	Programming voltage	-	2.7	-	3.6	V
V _{PP}	V _{PP} voltage range	-	7	-	9	V
I _{PP}	Minimum current sunk on the V _{PP} pin	-	10	-	-	mA
t _{VPP} ⁽³⁾	Cumulative time during which V _{PP} is applied	-	-	-	1	hour

1. Guaranteed by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 50. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min ⁽¹⁾	
N _{END}	Endurance	T _A = -40 to +85 °C (6 suffix versions) T _A = -40 to +105 °C (7 suffix versions)	10	kcycles
t _{RET}	Data retention	1 kcycle ⁽²⁾ at T _A = 85 °C	30	Years
		1 kcycle ⁽²⁾ at T _A = 105 °C	10	
		10 kcycle ⁽²⁾ at T _A = 55 °C	20	

1. Guaranteed by characterization, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

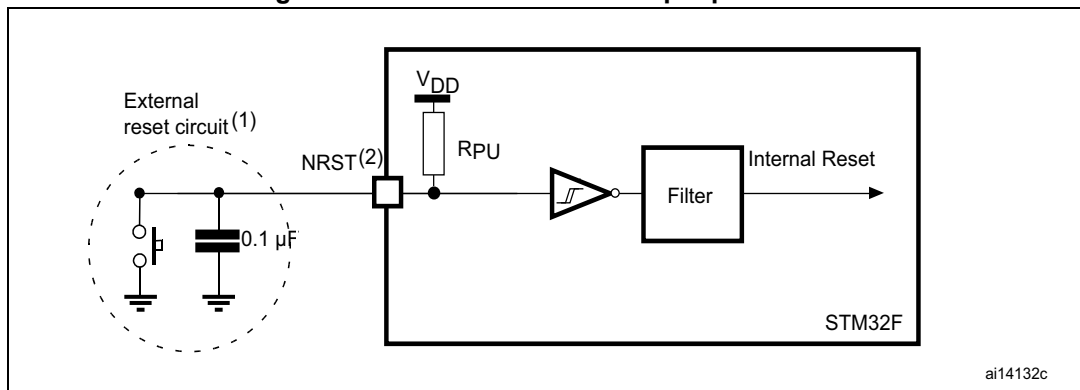
Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

Figure 37. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 59](#). Otherwise the reset is not taken into account by the device.

6.3.18 TIM timer characteristics

The parameters given in [Table 60](#) are guaranteed by design.

Refer to [Section 6.3.16: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 60. TIMx characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions ⁽³⁾	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK} = 100\text{ MHz}$	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APBx prescaler>4, $f_{TIMxCLK} = 100\text{ MHz}$	1	-	$t_{TIMxCLK}$
			11.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK} = 100\text{ MHz}$	0	$f_{TIMxCLK}/2$	MHz
			0	50	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	$f_{TIMxCLK} = 100\text{ MHz}$	0.0119	780	μs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 100\text{ MHz}$	-	51.1	S

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.
2. Guaranteed by design, not tested in production.
3. The maximum timer frequency on APB1 is 50 MHz and on APB2 is up to 100 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then $TIMxCLK = HCLK$, otherwise $TIMxCLK \geq 4 \times PCLKx$.

Table 73. ADC accuracy at $f_{\text{ADC}} = 30 \text{ MHz}^{(1)}$

Symbol	Parameter	Test conditions	Typ	Max ⁽²⁾	Unit
ET	Total unadjusted error	$f_{\text{ADC}} = 30 \text{ MHz}$, $R_{\text{AIN}} < 10 \text{ k}\Omega$, $V_{\text{DDA}} = 2.4 \text{ to } 3.6 \text{ V}$, $V_{\text{REF}} = 1.7 \text{ to } 3.6 \text{ V}$, $V_{\text{DDA}} - V_{\text{REF}} < 1.2 \text{ V}$	± 2	± 5	LSB
EO	Offset error		± 1.5	± 2.5	
EG	Gain error		± 1.5	± 4	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 1.5	± 3	

1. Better performance could be achieved in restricted V_{DD} , frequency and temperature ranges.
2. Guaranteed by characterization, not tested in production.

Table 74. ADC accuracy at $f_{\text{ADC}} = 36 \text{ MHz}^{(1)}$

Symbol	Parameter	Test conditions	Typ	Max ⁽²⁾	Unit
ET	Total unadjusted error	$f_{\text{ADC}} = 36 \text{ MHz}$, $V_{\text{DDA}} = 2.4 \text{ to } 3.6 \text{ V}$, $V_{\text{REF}} = 1.7 \text{ to } 3.6 \text{ V}$, $V_{\text{DDA}} - V_{\text{REF}} < 1.2 \text{ V}$	± 4	± 7	LSB
EO	Offset error		± 2	± 3	
EG	Gain error		± 3	± 6	
ED	Differential linearity error		± 2	± 3	
EL	Integral linearity error		± 3	± 6	

1. Better performance could be achieved in restricted V_{DD} , frequency and temperature ranges.
2. Guaranteed by characterization, not tested in production.

Table 75. ADC dynamic accuracy at $f_{\text{ADC}} = 18 \text{ MHz}$ - limited test conditions⁽¹⁾

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	$f_{\text{ADC}} = 18 \text{ MHz}$ $V_{\text{DDA}} = V_{\text{REF}+} = 1.7 \text{ V}$ Input Frequency = 20 kHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		-	-72	-67	

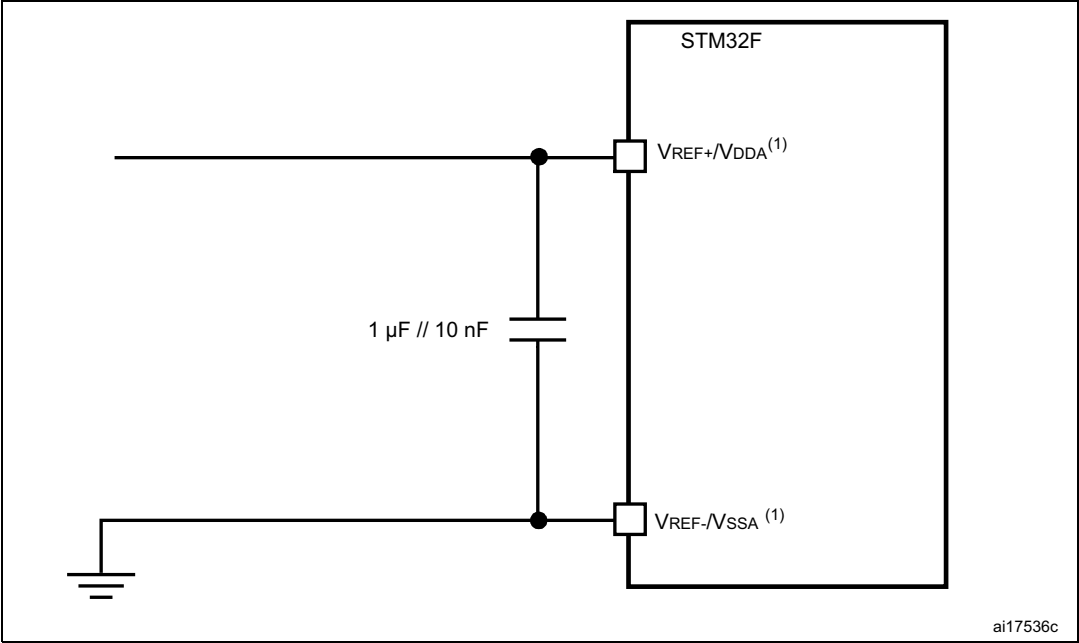
1. Guaranteed by characterization, not tested in production.

Table 76. ADC dynamic accuracy at $f_{\text{ADC}} = 36 \text{ MHz}$ - limited test conditions⁽¹⁾

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	$f_{\text{ADC}} = 36 \text{ MHz}$ $V_{\text{DDA}} = V_{\text{REF}+} = 3.3 \text{ V}$ Input Frequency = 20 kHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		-	-72	-70	

1. Guaranteed by characterization, not tested in production.

Figure 49. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA} .

6.3.21 Temperature sensor characteristics

Table 77. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	-	2.5	-	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	-	0.76	-	V
$t_{START}^{(2)}$	Startup time	-	6	10	μs
$T_{S_temp}^{(2)}$	ADC sampling time when reading the temperature (1 $^{\circ}\text{C}$ accuracy)	10	-	-	μs

1. Guaranteed by characterization, not tested in production.

2. Guaranteed by design, not tested in production.

Table 78. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 $^{\circ}\text{C}$, V_{DDA} = 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 $^{\circ}\text{C}$, V_{DDA} = 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output characteristics.

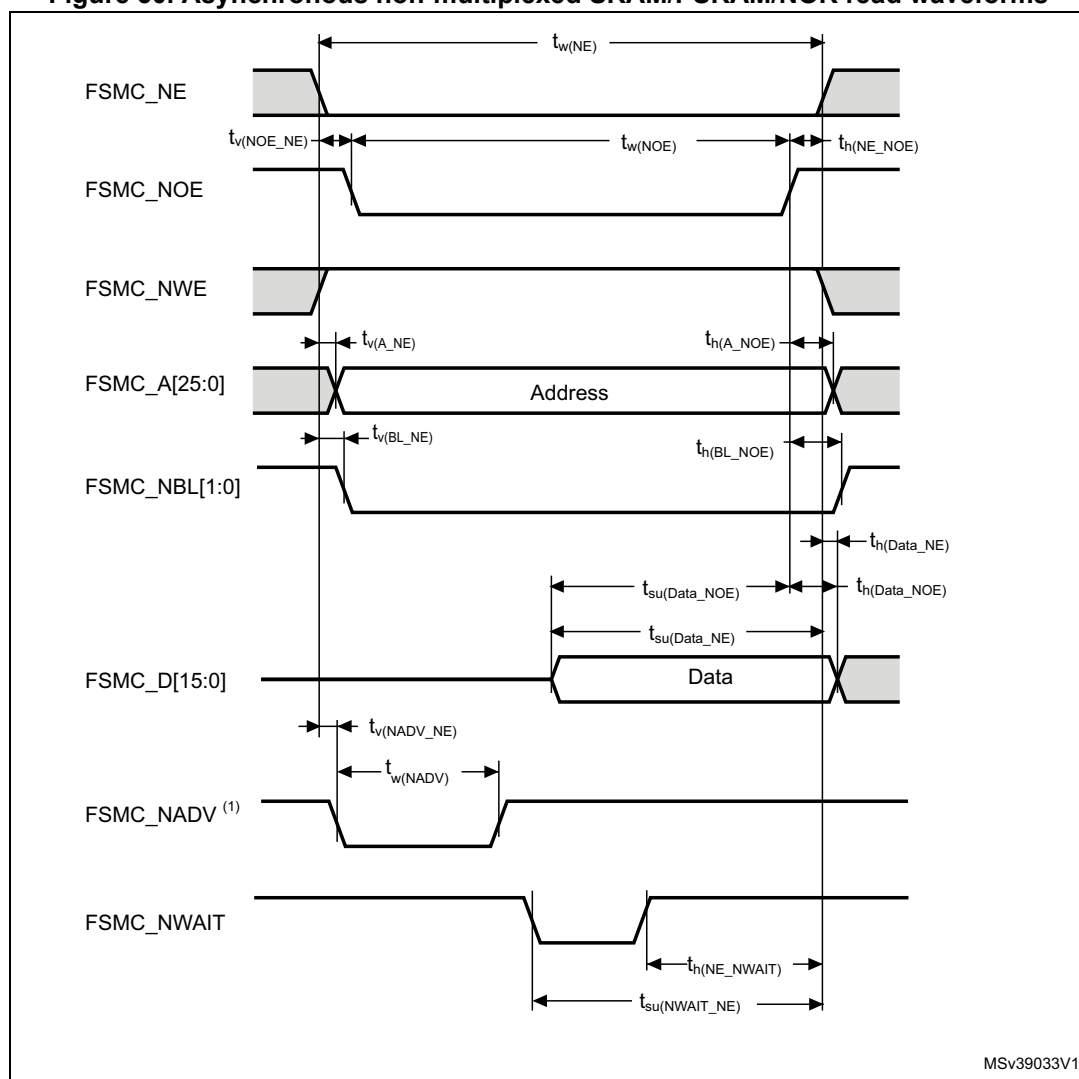
Asynchronous waveforms and timings

[Figure 50](#) through [Figure 53](#) represent asynchronous waveforms and [Table 83](#) through [Table 90](#) provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

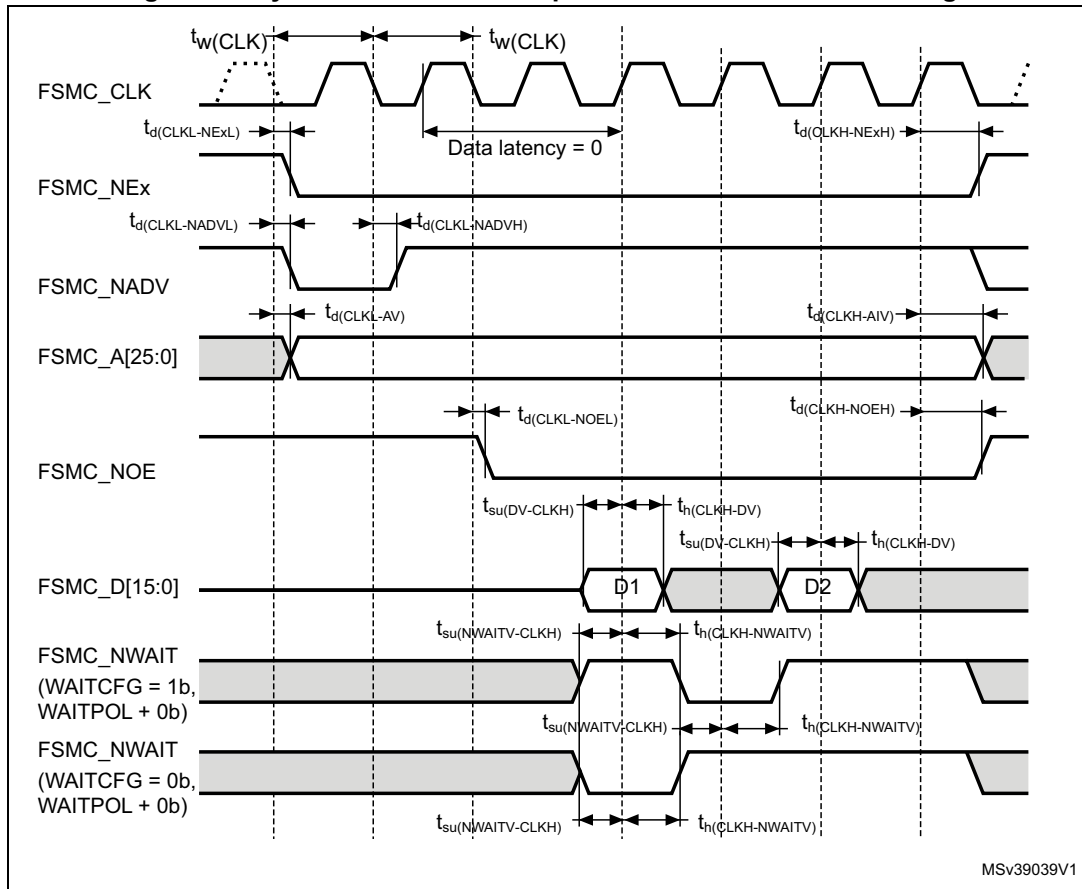
In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 50. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

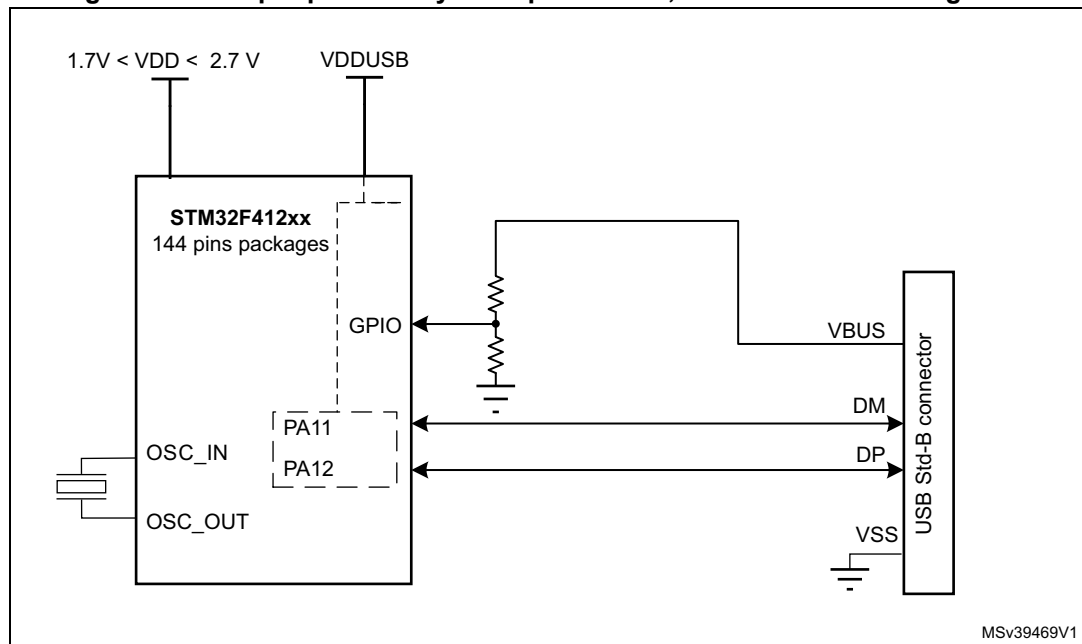


1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

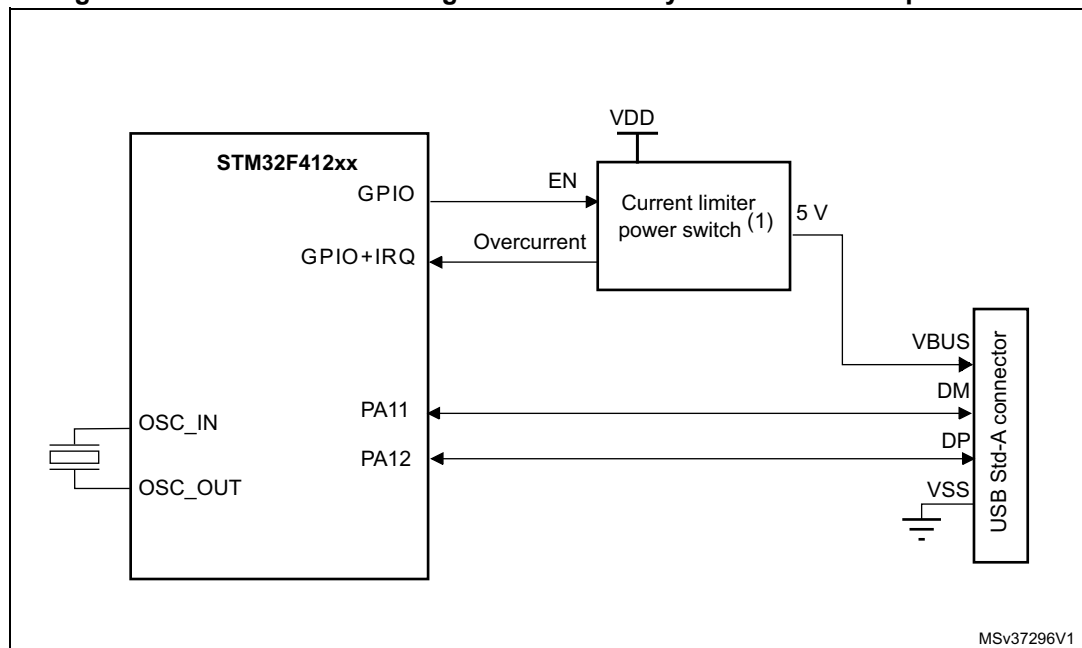
Figure 56. Synchronous non-multiplexed NOR/PSRAM read timings

Table 93. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{CLK})$	FSMC_CLK period	$2T_{\text{HCLK}} - 0.5$	-	ns
$t_{\text{d}}(\text{CLKL-NExL})$	FSMC_CLK low to FSMC_NEx low ($x=0..2$)	-	1	
$t_{\text{d}}(\text{CLKH-NExH})$	FSMC_CLK high to FSMC_NEx high ($x=0..2$)	$T_{\text{HCLK}} + 0.5$	-	
$t_{\text{d}}(\text{CLKL-NADVL})$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{\text{d}}(\text{CLKL-NADVH})$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{\text{d}}(\text{CLKL-AV})$	FSMC_CLK low to FSMC_Ax valid ($x=16..25$)	-	2	
$t_{\text{d}}(\text{CLKH-AIV})$	FSMC_CLK high to FSMC_Ax invalid ($x=16..25$)	T_{HCLK}	-	
$t_{\text{d}}(\text{CLKL-NOEL})$	FSMC_CLK low to FSMC_NOE low	-	1.5	
$t_{\text{d}}(\text{CLKH-NOEH})$	FSMC_CLK high to FSMC_NOE high	T_{HCLK}	-	
$t_{\text{su}}(\text{DV-CLKH})$	FSMC_D[15:0] valid data before FSMC_CLK high	1	-	
$t_{\text{h}}(\text{CLKH-DV})$	FSMC_D[15:0] valid data after FSMC_CLK high	2	-	
$t_{\text{su}}(\text{NWAIT-CLKH})$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{\text{h}}(\text{CLKH-NWAIT})$	FSMC_NWAIT valid after FSMC_CLK high	2	-	

Figure 83. USB peripheral-only Full speed mode, VBUS detection using GPIO

1. External voltage regulator only needed when building a V_{BUS} powered device.

Figure 84. USB controller configured as host-only and used in full speed mode

1. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.