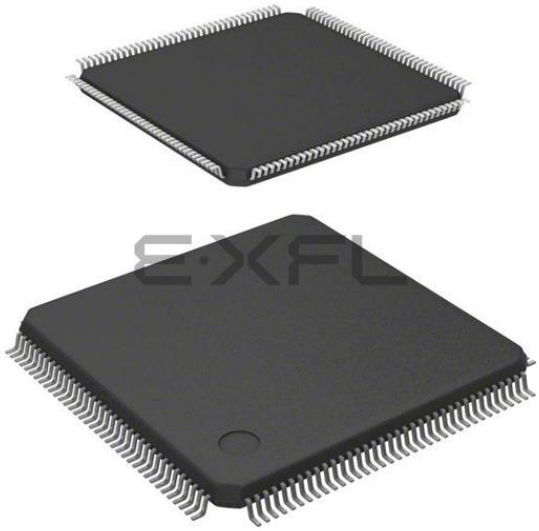

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f412zgt6

Contents

3 Functional overview

3.1 ARM® Cortex®-M4 with FPU core with embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F412xE/G devices are compatible with all ARM tools and software.

Figure 4 shows the general block diagram of the STM32F412xE/G.

Note: Cortex®-M4 with FPU is binary compatible with Cortex®-M3.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 125 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 100 MHz.

3.3 Batch Acquisition mode (BAM)

The Batch acquisition mode allows enhanced power efficiency during data batching. It enables data acquisition through any communication peripherals directly to memory using the DMA in reduced power consumption as well as data processing while the rest of the system is in low-power mode (including the flash and ART). For example in an audio system, a smart combination of PDM audio sample acquisition and processing from the DFSDM directly to RAM (flash and ART™ stopped) with the DMA using BAM followed by some very short processing from flash allows to drastically reduce the power consumption of the application. A dedicated application note (AN4515) describes how to implement the STM32F412xE/G BAM to allow the best power efficiency.

3.19.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal power supply supervisor availability

Package	Regulator ON	Regulator OFF	Power supply supervisor ON	Power supply supervisor OFF
UFQFPN48	Yes	No	Yes	No
WLCSP64	Yes	No	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP64	Yes	No	Yes	No
LQFP100	Yes	No	Yes	No
LQFP144	Yes	No	Yes PDR_ON set to VDD	Yes PDR_ON set to V_{SS}
UFBGA100	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD		
UFBGA144	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD		

3.20 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 byte of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.21: Low-power modes*).

3.23 Timers and watchdogs

The devices embed two advanced-control timer, ten general-purpose timers, two basic timers, two watchdog timers and one SysTick timer.

All timer counters can be frozen in debug mode.

Table 5 compares the features of the advanced-control and general-purpose timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max. interface clock (MHz)	Max. timer clock (MHz)
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	100	100
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	50	100
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	50	100
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	100	100
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	100	100
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	50	100
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	50	100
Basic timers	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	50	100

Table 9. STM32F412xE/G pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP64	LQFP100	UFBGA100	UFBGA144	LQFP144						
42	58	B5	92	B5	C6	136	PB6	I/O	FT	-	TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, SDIO_D0, EVENTOUT	-
43	59	A6	93	B4	D6	137	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FSMC_NL, EVENTOUT	-
44	60	D4	94	A4	D5	138	BOOT0	I	B	-	-	VPP
45	61	C5	95	A3	C5	139	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, SPI5_MOSI/I2S5_SD, CAN1_RX, I2C3_SDA, SDIO_D4, EVENTOUT	-
46	62	B6	96	B3	B5	140	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, I2C2_SDA, SDIO_D5, EVENTOUT	-
-	-	-	97	C3	A5	141	PE0	I/O	FT	-	TIM4_ETR, FSMC_NBL0, EVENTOUT	-
-	-	-	98	A2	A4	142	PE1	I/O	FT	-	FSMC_NBL1, EVENTOUT	-
47	63	A7	99	-	E6	-	VSS	S	-	-	-	-
-	-	C6	-	H3	E5	143	PDR_ON	I	FT	-	-	-
48	64	A8	100	-	F5	144	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F412xE/Greference manual.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

Table 10. STM32F412xE/G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
		SYS_AF	TIM1/ TIM2	TIM3/ TIM4/ TIM5	TIM8/ TIM9/ TIM10/ TIM11	I2C1/ I2C2/ I2C3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/SPI3 /I2S3/SPI4/ I2S4/SPI5/I2S5 /DFSDM1	SPI3/I2S3/ USART1/ USART2/ USART3	DFSDM1/ USART3/ USART6/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/CAN2 /TIM12/ TIM13/TIM14 /QUADSPI	DFSDM1/ QUADSPI/ FSMC /OTG1_FS	FSMC /SDIO	SYS_AF
Port C	PC0	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	I2S2ext_SD	-	DFSDM1_ CKOUT	-	-	FSMC_NWE	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI/I 2S2_SD	-	-	-	-	-	FSMC_A0	EVENTOUT
	PC4	-	-	-	-	-	I2S1_MCK	-	-	-	-	QUADSPI_ BK2_IO2	FSMC_NE4	EVENTOUT
	PC5	-	-	-	-	I2CFMP1_ SMBA	-	-	USART3_RX	-	-	QUADSPI_ BK2_IO3	FSMC_NOE	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	I2CFMP1_ SCL	I2S2_MCK	DFSDM1_ CKIN3	-	USART6_ TX	-	FSMC_D1	SDIO_D6	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	I2CFMP1_ SDA	SPI2_SCK/ I2S2_CK	I2S3_MCK	-	USART6_ RX	-	DFSDM1_ DATIN3	SDIO_D7	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_ CK	QUADSPI_ BK1_IO2	-	SDIO_D0	EVENTOUT
	PC9	MCO_2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	-	-	-	QUADSPI_ BK1_IO0	-	SDIO_D1	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK/ I2S3_CK	USART3_TX	-	QUADSPI_ BK1_IO1	-	SDIO_D2	EVENTOUT
	PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO	USART3_RX	-	QUADSPI_ BK2_NCS	FSMC_D2	SDIO_D3	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/ I2S3_SD	USART3_CK	-	-	FSMC_D3	SDIO_CK	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3 σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2 σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 19*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 20*.

Figure 19. Pin loading conditions

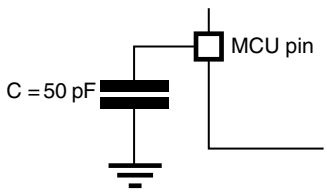


Figure 20. Input voltage measurement

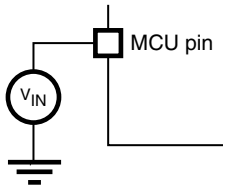


Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)	100	36.3	38.95	41.19	42.95	mA
			84	31.1	33.22	34.81	36.10	
			64	22.3	23.97	25.10	26.23	
			50	18.3	19.77	20.65	21.73	
			25	10.1	11.39	12.16	13.11	
			20	8.6	9.60	10.25	11.06	
		HSI, PLL OFF, all peripherals enabled(3)	16	6.3	6.85	7.51	8.38	
			1	1.1	1.39	1.82	2.61	
		External clock, PLL ON(2) all peripherals disabled(3)	100	22.1	23.95	25.80	27.50	
			84	19.7	20.79	22.52	24.12	
			64	14.5	15.88	17.21	18.54	
			50	12.2	13.38	14.59	15.79	
			25	7.0	8.05	8.89	10.16	
			20	6.0	6.84	7.51	8.52	
		HSI, PLL OFF, all peripherals disabled(3)	16	4.4	4.91	5.56	6.54	
			1	0.9	1.25	1.79	2.59	

1. Based on characterization, not tested in production unless otherwise specified.
2. Refer to *Table 44* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 29. Typical and maximum current consumption in Sleep mode - V_{DD} = 1.7 V (continued)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Sleep mode**	All peripherals disabled, External clock, PLL ON(2), Flash deep power down	100	2.9	3.51	4.14	4.90	mA
			84	2.4	2.83	3.46	4.16	
			64	1.7	2.08	2.59	3.18	
			50	1.4	1.77	2.23	2.84	
			25	1.0	1.37	1.88	2.50	
			20	1.3	1.37	1.88	2.50	
		All peripherals disabled, HSI, PLL OFF(2), Flash deep power down	16	0.5	0.63	1.23	1.91	
			1	0.4	0.52	1.13	1.81	
		All peripherals disabled, External clock, PLL ON(2), Flash ON	100	3.3	3.22	3.98	4.90	
			84	2.8	2.62	3.30	4.16	
			64	2.1	1.89	2.50	3.18	
			50	1.7	1.58	2.16	2.84	
			25	1.2	1.28	1.82	2.50	
			20	1.3	1.28	1.82	2.50	
		All peripherals disabled, HSI, PLL OFF(2), Flash ON	16	0.8	0.88	1.36	1.91	
			1	0.7	0.77	1.26	1.81	

1. Based on characterization, not tested in production unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 30. Typical and maximum current consumptions in Stop mode - V_{DD} = 1.7 V

Symbol	Conditions	Parameter	Typ(1)	Max(1)			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	121.1	168.0	648.7	1213.0	µA
		Low power regulator usage	50.8	104.7	667.4	1328.0	
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	79.1	122.0	609.1	1181.0	
		Low power regulator usage	22.4	74.7	631.9	1286.0	
		Low power low voltage regulator usage	18.5	58.5	558.3	1145.0	

1. Based on characterization, not tested in production.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 52. EMI characteristics for LQFP144

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/100 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP144 package, conforming to IEC 61967-2, EEMBC, ART ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	20	dBµV
			30 to 130 MHz	28	
			130 MHz to 1 GHz	21	
			EMI Level	3.5	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

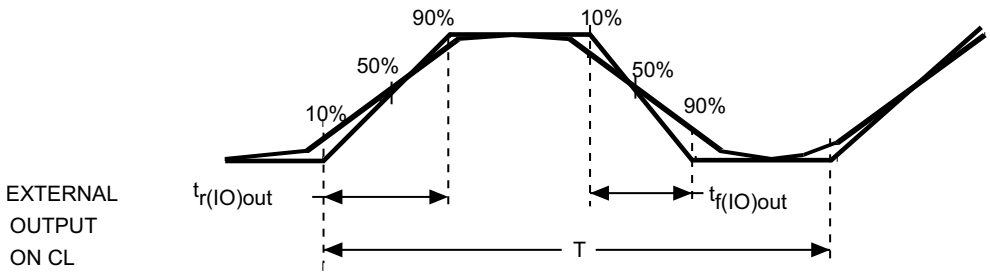
Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 53. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1, UFBGA144, UFBGA100, LQFP100, LQFP64, UFQFPN48	4	500	
		T_A = +25 °C conforming to ANSI/ESD STM5.3.1, WLCSP64	3	400	
		T_A = +25 °C conforming to ANSI/ESD STM5.3.1, LQFP144	3	250	

1. Guaranteed by characterization, not tested in production.

Figure 36. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

ai14131d

6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 56*).

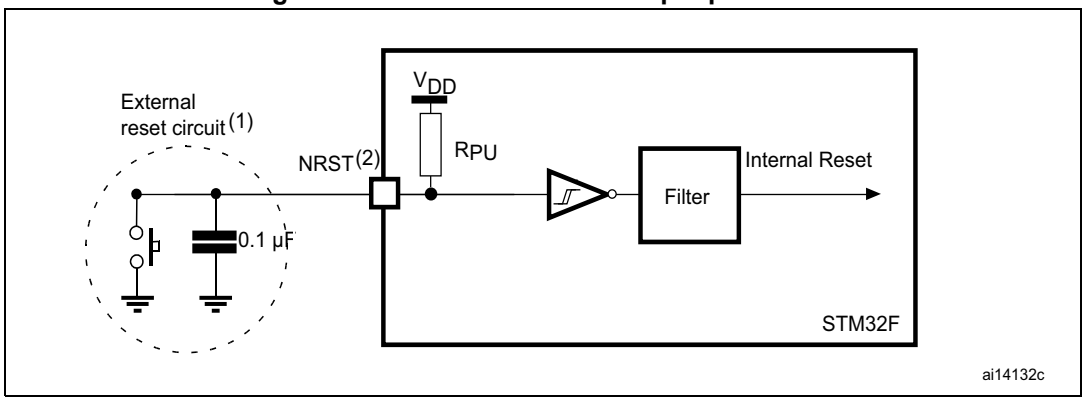
Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*. Refer to *Table 56: I/O static characteristics* for the values of VIH and VIL for NRST pin.

Table 59. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design, not tested in production.

Figure 37. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 59*. Otherwise the reset is not taken into account by the device.

6.3.18 TIM timer characteristics

The parameters given in *Table 60* are guaranteed by design.

Refer to *Section 6.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 60. TIMx characteristics(1)(2)

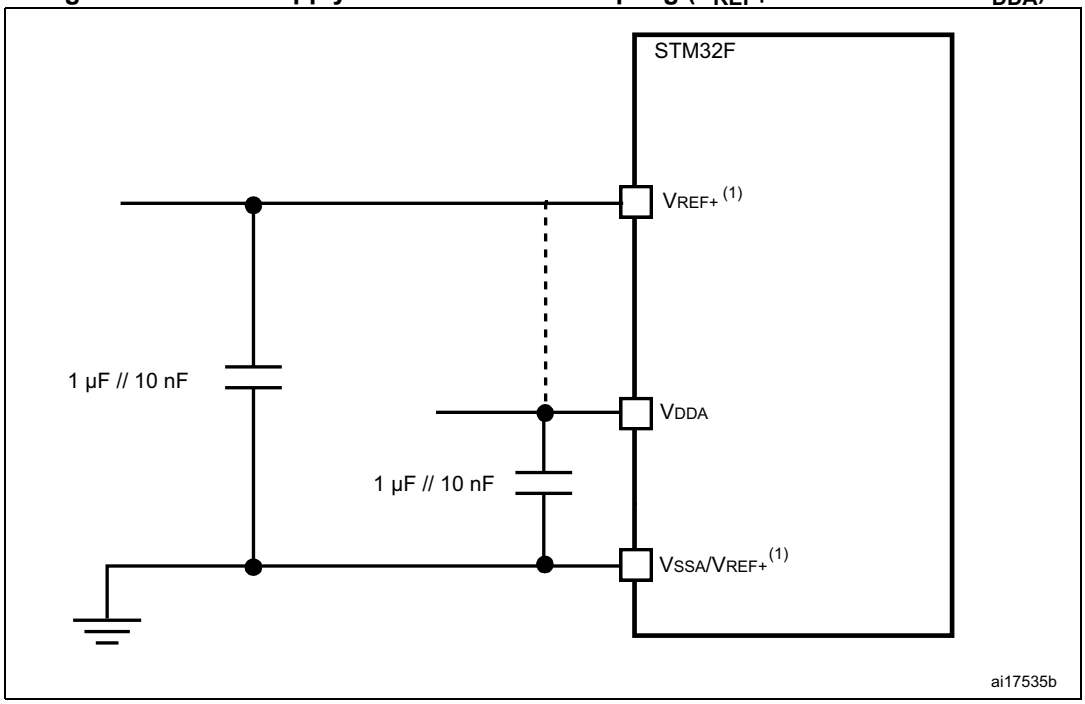
Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 100 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 100 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 100 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	50	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	$f_{TIMxCLK}$ = 100 MHz	0.0119	780	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 100 MHz	-	51.1	S

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.
2. Guaranteed by design, not tested in production.
3. The maximum timer frequency on APB1 is 50 MHz and on APB2 is up to 100 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK >= 4x PCLKx.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 48* or *Figure 49*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 48. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



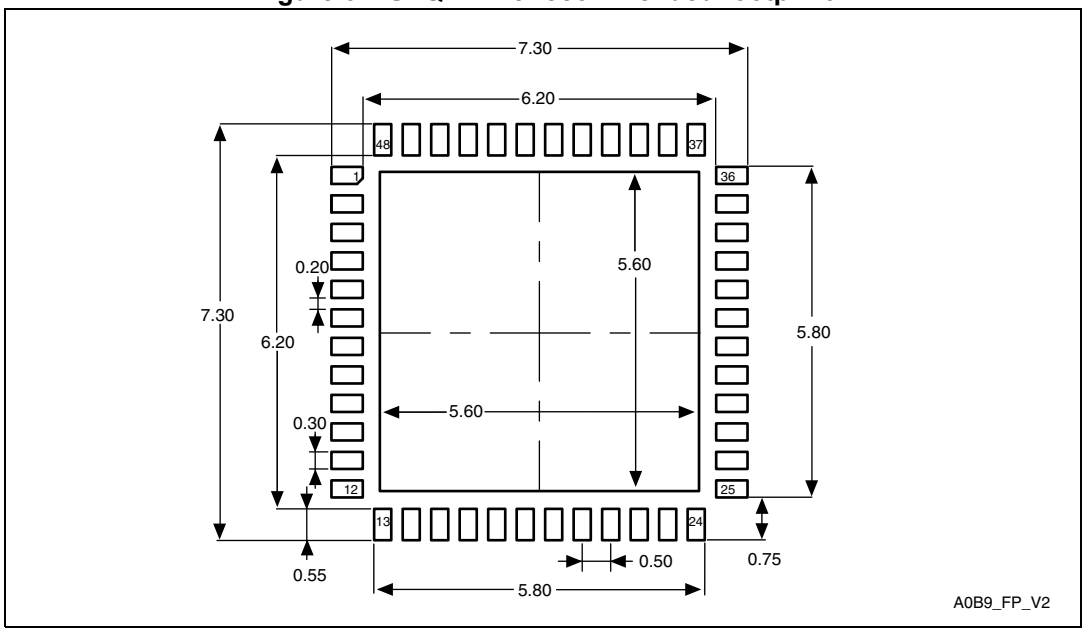
1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Table 100. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 64. UFQFPN48 recommended footprint



1. Dimensions are in millimeters.

Table 104. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 76. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

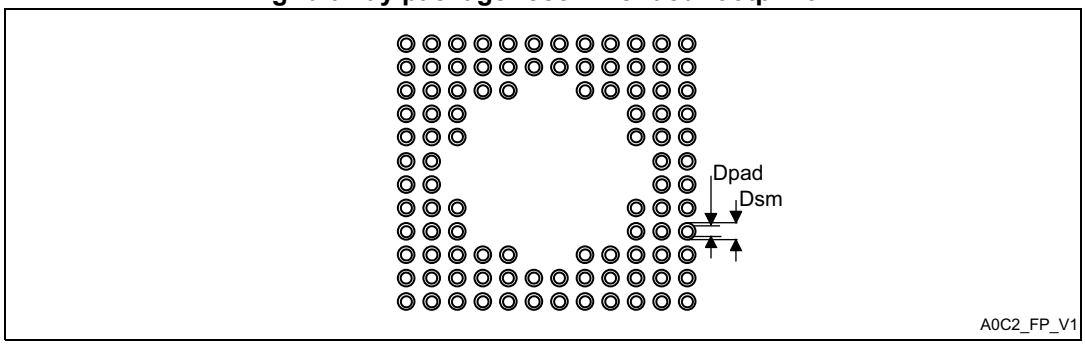


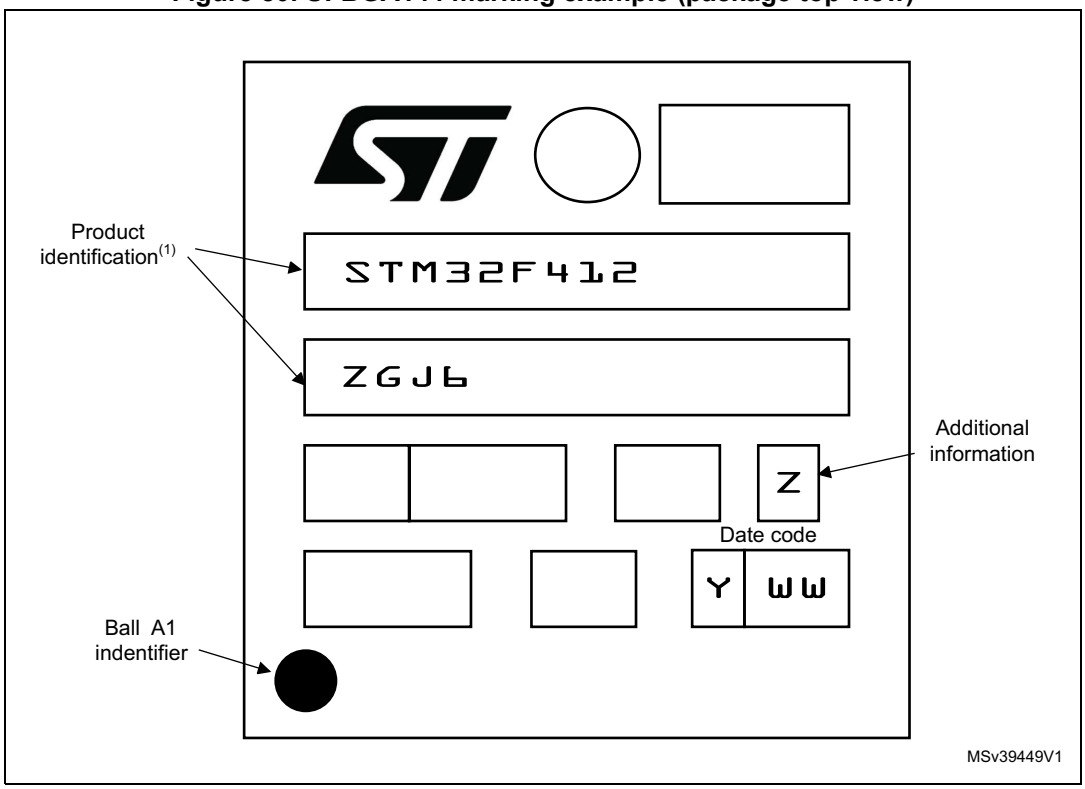
Table 105. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Device marking for UFBGA144

The following figure gives an example of topside marking and ball A1 position identifier location.

Figure 80. UFBGA144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

8 Part numbering

Table 109. Ordering information scheme

Example: STM32 F 412 C E T 6 TR

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = General-purpose

Device subfamily

412 = 412 line

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Z = 144 pins

Flash memory size

E = 512 Kbytes of Flash memory

G = 1024 Kbytes of Flash memory

Package

H = UFBGA 7 x 7 mm

J = UFBGA 10 x 10 mm

T = LQFP

U = UFQFPN

Y = WLCSP

Temperature range

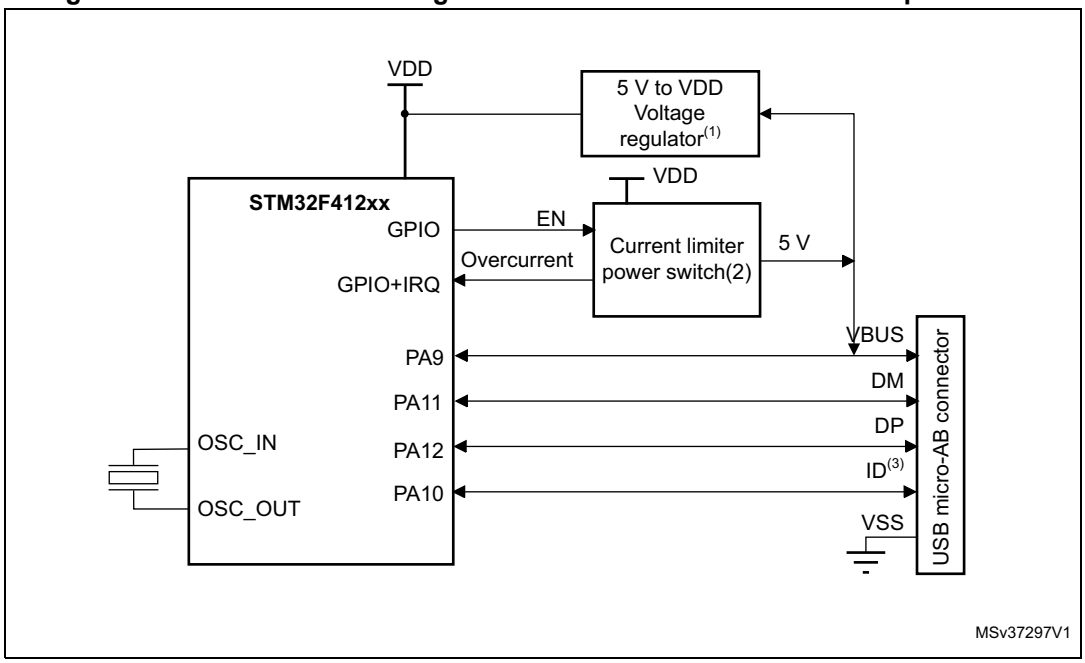
6 = Industrial temperature range, –40 to 85 °C

Packing

TR = tape and reel

No character = tray or tube

Figure 85. USB controller configured in dual mode and used in full speed mode



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.

B.2 Sensor Hub application example

Figure 86. Sensor Hub application example

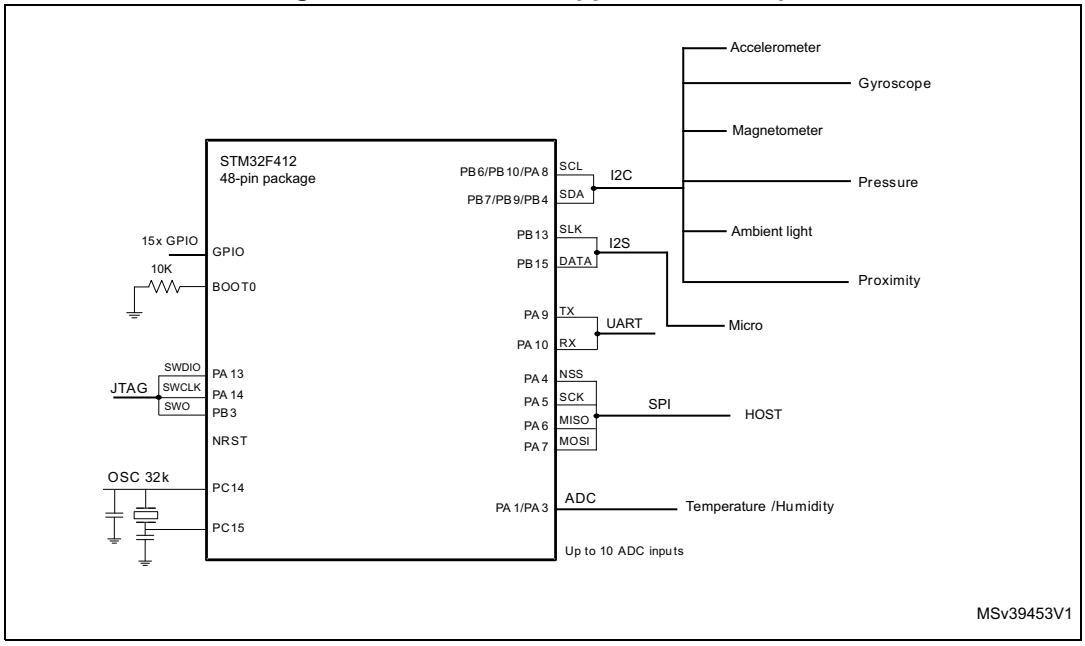


Table 110. Document revision history

Date	Revision	Changes
25-Mar-2016	3	Added: – *Figure 82: USB peripheral-only Full speed mode with direct connection for VBUS sense* – *Figure 83: USB peripheral-only Full speed mode, VBUS detection using GPIO* Updated: – *Figure 15: STM32F412xE/G LQFP144 pinout* – *Section 6.3.6: Supply current characteristics* – *Table 9: STM32F412xE/G pin definition* – *Table 10: STM32F412xE/G alternate functions* – *Table 11: STM32F412xE/G register boundary addresses* – *Table 15: General operating conditions* – *Table 36: Peripheral current consumption* – *Table 96: Dynamic characteristics: eMMC characteristics VDD = 1.7 V to 1.9 V*
27-May-2016	4	Updated: – *Section 3.23.2: General-purpose timers (TIMx)* – *Table 21: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - VDD = 1.7 V* – *Table 22: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - VDD = 3.6 V* – *Table 23: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- VDD = 1.7 V* – *Table 24: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - VDD = 3.6 V* – *Table 25: Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - VDD = 3.6 V* – *Table 26: Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - VDD = 1.7 V* – *Table 27: Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - VDD = 3.6 V* – *Table 28: Typical and maximum current consumption in Sleep mode - VDD = 3.6 V* – *Table 29: Typical and maximum current consumption in Sleep mode - VDD = 1.7 V* – *Table 37: Low-power mode wakeup timings(1)* – *Figure 38: I2C bus AC waveforms and measurement circuit* – *Figure 39: FMPI2C timing diagram and measurement circuit*