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Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n79e822arg

4 PIN CONFIGURATION

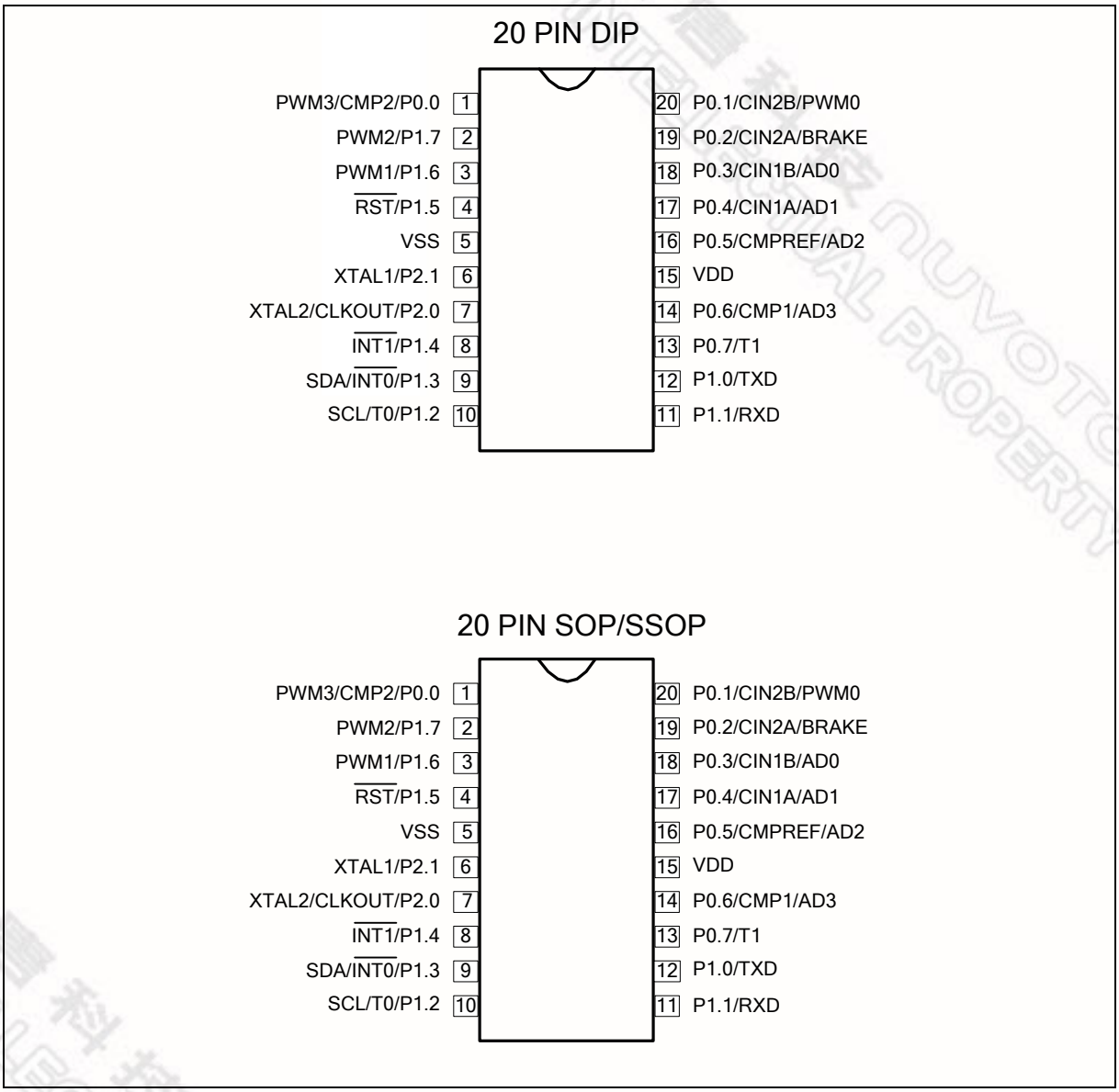

Figure 4-1: Pin Configuration

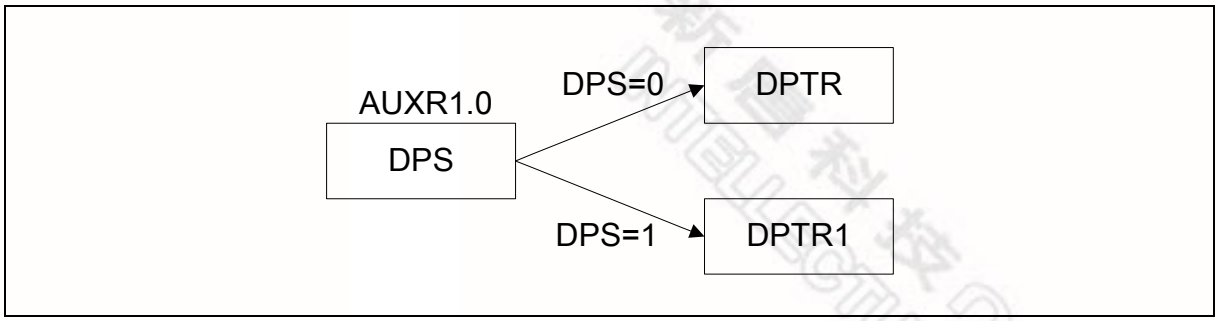

Figure 6-1: Dual DPTR

6.7 Architecture

The N79E825 series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

6.7.1 ALU

The ALU is the heart of the N79E825 series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the N79E825 series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.7.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.7.5 Scratch-pad RAM

The N79E825 series have a **256** bytes on-chip scratch-pad RAM. These can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

SYMBOL	DEFINITION	ADDRESS	MSB LSB BIT_ADDRESS, SYMBOL								RESET
IP1	Interrupt priority 1	F8H	(FF) -	(FE) -	(FD) PPWM	(FC) PWDI	(FB) PC2	(FA) PC1	(F9) PKB	(F8) PI2	xx000000B
IP1H	Interrupt high priority 1	F7H	-	-	PPWMH	PWDIH	PC2H	PC1H	PKBH	PI2H	xx000000B
P0IDS	Port 0 Digital Input Disable	F6H									00000000B
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	00000000B
EIE	Interrupt enable 1	E8H	(EF) -	(EE) -	(ED) EPWM	(EC) EWDI	(EB) EC2	(EA) EC1	(E9) EKB	(E8) EI2C	xx000000B
ADCH	ADC converter result	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	xxxxxxxxB
ADCCON	ADC control register	E1H	ADC.1	ADC.0	ADCEX	ADCI	ADCS	RCCLK	AADR1	AADR0	xx000x00B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	00000000B
PWMCON2	PWM control register 2	DFH	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B	00000000B
PWM3L	PWM 3 low bits register	DEH	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0	00000000B
PWM2L	PWM 2 low bits register	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	00000000B
PWMCON1	PWM control register 1	DCH	PWMRUN	load	CF	CLRPWM	PWM3I	PWM2I	PWM1I	PWM0I	00000000B
PWM1L	PWM 1 low bits register	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	00000000B
PWM0L	PWM 0 low bits register	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	00000000B
PWMPL	PWM counter low register	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	00000000B
WDCON	Watch-Dog control	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	0x000000B
PWMCON3	PWM control register 3	D7H	-	-	-	-	-	-	-	BKF	xxxxxxx0B
PWM3H	PWM 3 high bits register	D6H	-	-	-	-	-	-	PWM3.9	PWM3.8	xxxxxx00B
PWM2H	PWM 2 high bits register	D5H	-	-	-	-	-	-	PWM2.9	PWM2.8	xxxxxx00B
PWM1H	PWM 1 high bits register	D3H	-	-	-	-	-	-	PWM1.9	PWM1.8	xxxxxx00B
PWM0H	PWM 0 high bits register	D2H	-	-	-	-	-	-	PWM0.9	PWM0.8	xxxxxx00B
PWMPH	PWM counter high register	D1H	-	-	-	-	-	-	PWMP0.9	PWMP0.8	xxxxxx00B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	00000000B
NVMDATA	NVM Data	CFH									00000000B
NVMCON	NVM Control	CEH	EER	EWR	-	-	-	-	-	-	00000000B
TA	Timed Access Protection	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	11111111B
NVMADDR	NVM address	C6H									00000000B
I2ADDR	I2C address1	C1H	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxxxxx0B
I2CON	I2C Control register	C0H	(C7) -	(C6) ENS1	(C5) STA	(C4) STO	(C3) SI	(C2) AA	(C1) -	(C0) -	x00000xxB
I2TIMER	I2C Timer Counter register	BFH	-	-	-	-	-	ENTI	DIV4	TIF	00000000B
I2CLK	I2C Clock Rate	BEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	00000000B
I2STATUS		BDH									1111000B
I2DAT		BCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxxxxxxB
SADEN	Slave address mask	B9H									00000000B
IP0	Interrupt priority	B8H	(BF) -	(BE) PADC	(BD) PBO	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x0000000B
IP0H	Interrupt high priority	B7H	-	PADCH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H	x0000000B
P2M2	Port 2 output mode 2	B6H	-	-	-	-	-	-	P2M2.1	P2M2.0	xxxxxx00B
P2M1	Port 2 output mode 1	B5H	P2S	P1S	P0S	ENCLK	T1OE	T0OE	P2M1.1	P2M1.0	00000000B
P1M2	Port 1 output mode 2	B4H	P1M2.7	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	00000000B
P1M1	Port 1 output mode 1	B3H	P1M1.7	P1M1.6	-	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	00000000B
P0M2	Port 0 output mode 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	00000000B
P0M1	Port 0 output mode 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	00000000B

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	-	-	T1M	T0M	-	-	-

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7-5	-	Reserved.
4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 4 clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 4 clocks.
2-0	-	Reserved.

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P1.7	PWM 2 Pin.
6	P1.6	PWM 1 Pin.
5	P1.5	/RST Pin or Input Pin by alternative.
4	P1.4	/INT1 interrupt.
3	P1.3	/INT0 interrupt or SDA of I2C.
2	P1.2	Timer 0 or SCL of I2C.
1	P1.1	RXD of Serial port.
0	P1.0	TXD of Serial port.

Note: The initial value of the port is set by CONFIG1.PRHI bit. The default setting for CONFIG1.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG1.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

DIVIDER CLOCK

Bit:	7	6	5	4	3	2	1	0
	DIVM.7	DIVM.6	DIVM.5	DIVM.4	DIVM.3	DIVM.2	DIVM.1	DIVM.0

Mnemonic: DIVM Address: 95h

Continued.

BIT	NAME	FUNCTION
3	CN1	Comparator negative input select: 0: The comparator reference pin CMPREF is selected as the negative comparator input. 1: The internal comparator reference Vref is selected as the negative comparator input.
2	OE1	Output enable: 1: The comparator output is connected to the CMP1 pin if the comparator is enabled (CE1 = 1). This output is asynchronous to the CPU clock.
1	CO1	Comparator output: Synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CE1 = 0).
0	CMF1	Comparator interrupt flag: This bit is set by hardware whenever the comparator output CO1 changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CE1 = 0).

COMPARATOR 2 CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	CE2	CP2	CN2	OE2	CO2	CMF2

Mnemonic: CMP2 Address: ADh

BIT	NAME	FUNCTION
7	-	Reserved.
6	-	Reserved.
5	CE2	Comparator enable: 0: Disable Comparator. 1: Enabled Comparator. Comparator output need wait stable 10 us after CE2 is first set.
4	CP2	Comparator positive input select: 0: CIN2A is selected as the positive comparator input. 1: CIN2B is selected as the positive comparator input.
3	CN2	Comparator negative input select: 0: The comparator reference pin CMPREF is selected as the negative comparator input. 1: The internal comparator reference Vref is selected as the negative comparator input.

```
TA      REG     C7H
WDCON   REG     D8H
MOV     TA, #AAH            ; To access protected bits
MOV     TA, #55H
SETB    WDCON.0             ; Reset watchdog timer
ORL     WDCON, #00110000B   ; Select 26 bits watchdog timer
MOV     TA, #AAH
MOV     TA, #55H
ORL     WDCON, #00000010B   ; Enable watchdog
```

PWMP COUNTER LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWMP.7	PWMP.6	PWMP.5	PWP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.1

Mnemonic: PWMPL Address: D9h

BIT	NAME	FUNCTION
7~0	PWMP.[7:0]	PWM Counter Low Bits Register.

PWM0 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.1

Mnemonic: PWM0L Address: DAh

BIT	NAME	FUNCTION
7~0	PWM0.[7:0]	PWM 0 Low Bits Register.

PWM1 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Mnemonic: PWM1L Address: DBh

BIT	NAME	FUNCTION
7~0	PWM1.[7:0]	PWM 1 Low Bits Register.

PWM CONTROL REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	Load	CF	CLRPWM	PWM3I	PWM2I	PWM1I	PWM0I

Mnemonic: PWMCON1 Address: DCh

ADDC A, @R1	37	1	1	4	12	3

Continued

OP-CODE	HEX CODE	BYTES	N79E825 SERIES MACHINE CYCLE	N79E825 SERIES CLOCK CYCLES	8032 CLOCK CYCLES	N79E825 SERIES VS. 8032 SPEED RATIO
ADDC A, direct	35	2	2	8	12	1.5
ADDC A, #data	34	2	2	8	12	1.5
SUBB A, R0	98	1	1	4	12	3
SUBB A, R1	99	1	1	4	12	3
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3
SUBB A, @R0	96	1	1	4	12	3
SUBB A, @R1	97	1	1	4	12	3
SUBB A, direct	95	2	2	8	12	1.5
SUBB A, #data	94	2	2	8	12	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3
INC R5	0D	1	1	4	12	3
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3

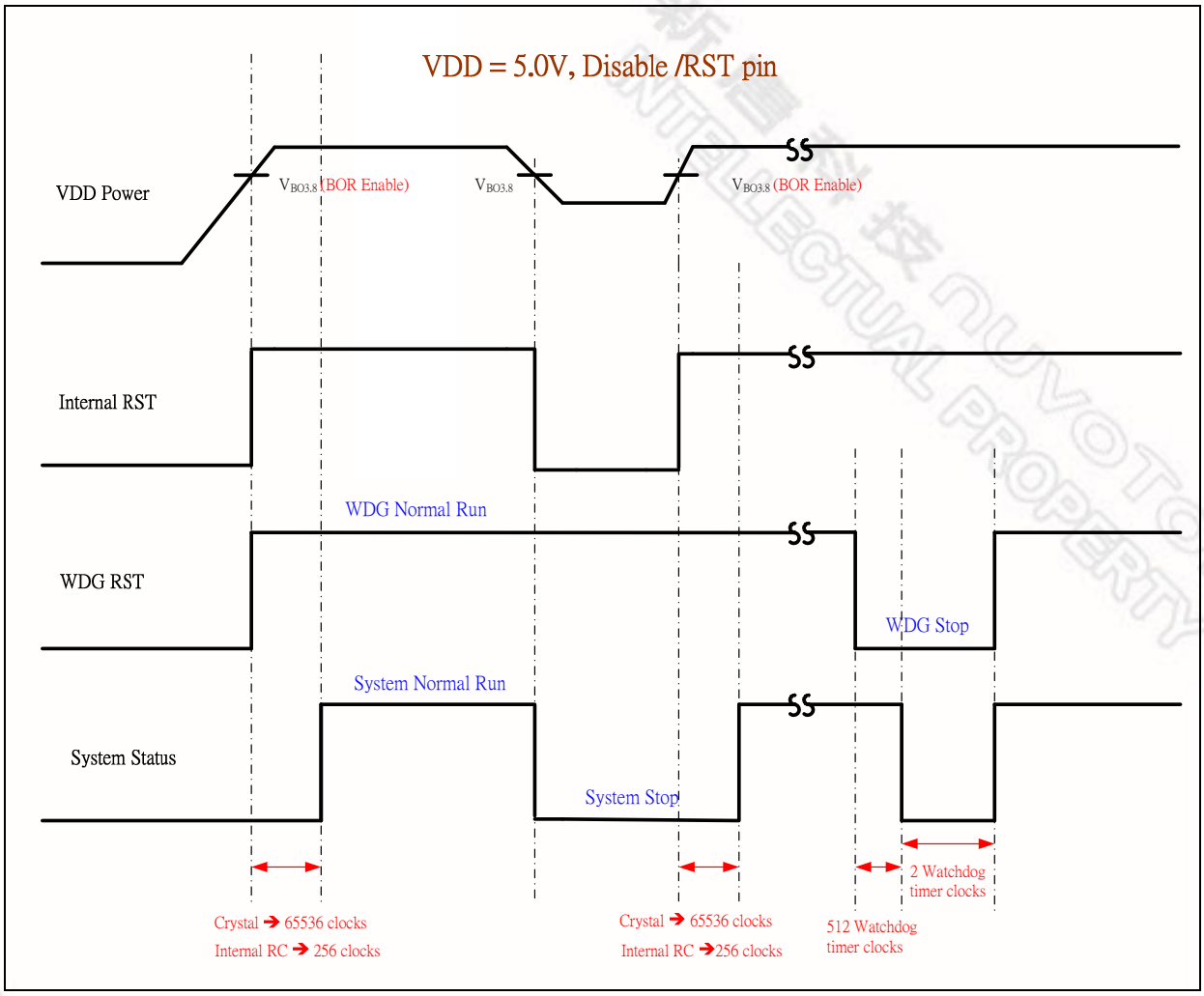

Figure 11-1: Internal reset and VDD monitor timing diagram

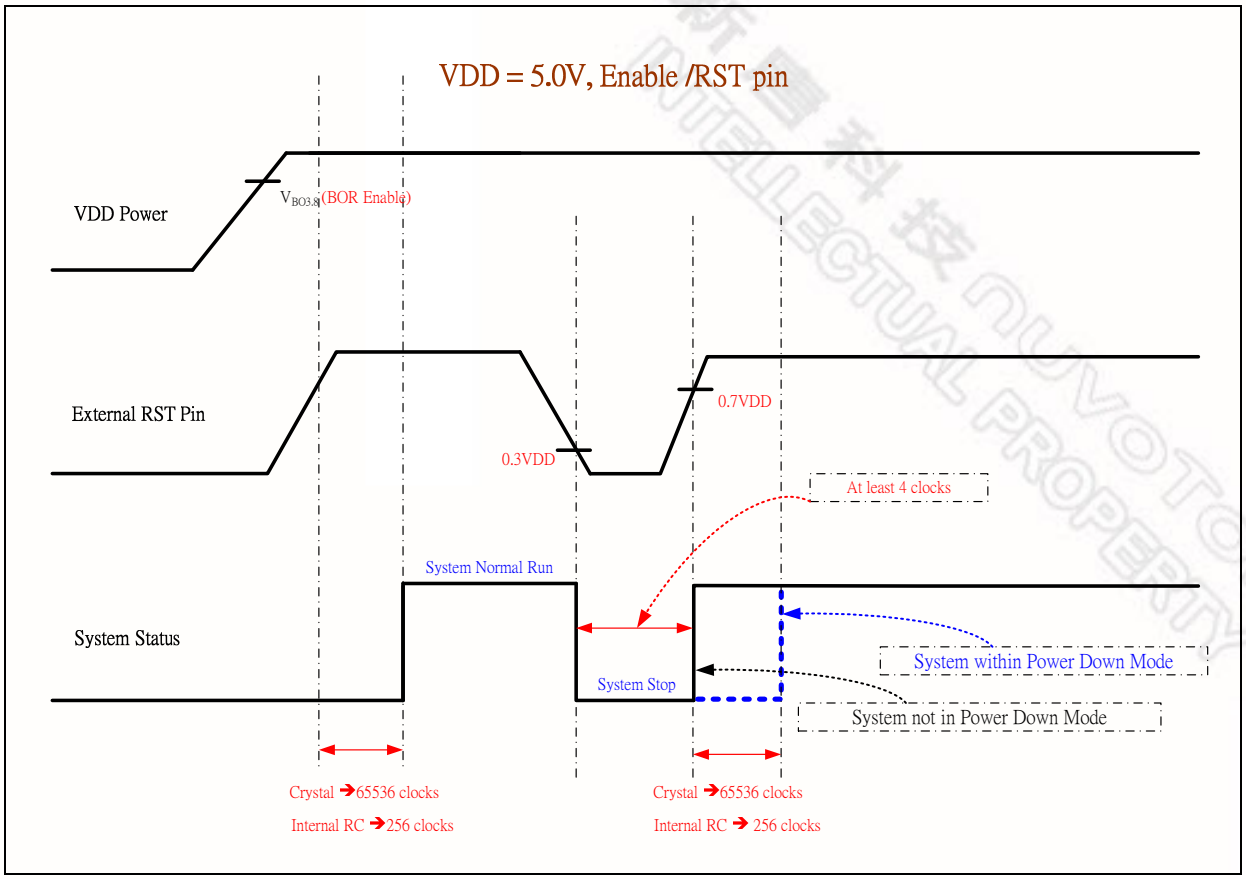

Figure 11-2: External reset timing diagram

13 PROGRAMMABLE TIMERS/COUNTERS

The N79E825 series have two 16-bit programmable timer/counters and one programmable Watchdog Timer. The Watchdog Timer is operationally quite different from the other two timers. It's timer/counters have additional timer 0 or timer 1 overflow toggle output enable feature as compare to conventional timer/counters. This timer overflow toggle output can be configured to automatically toggle T0 or T1 pin output whenever a timer overflow occurs.

13.1 Timer/Counters 0 & 1

The N79E825 series have two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 for Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/8 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

13.1.1 Time-Base Selection

The N79E825 series can operate like the standard 8051/52 family, counting at the rate of 1/12 of the clock speed, or in turbo mode, counting at the rate of 1/4 clock speed. The speed is controlled by the T0M and T1M bits in CKCON, and the default value is zero, which uses the standard 8051/52 speed.

13.1.2 Mode 0

In Mode 0, the timer/counter is a 13-bit counter. The 13-bit counter consists of THx (8 MSB) and the five lower bits of TLx (5 LSB). The upper three bits of TLx are ignored. The timer/counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. When $C/\overline{T}$ is 0, the timer/counter counts clock cycles; when $C/\overline{T}$ is 1, it counts falling edges on T0 (P1.2 for Timer 0) or T1 (P0.7 for Timer 1). For clock cycles, the time base may be 1/12 or 1/4 clock speed, and the falling edge of the clock increments the counter. When the 13-bit value moves from 1FFFh to 0000h, the timer overflow flag TFx is set, and an interrupt occurs if enabled. This is illustrated in next figure below.

In "Timer" mode, if output toggle enable bit of P2M1.T0OE or P2M1.T1OE is enabled, T0 or T1 output pin will toggle whenever a timer overflow occurs.

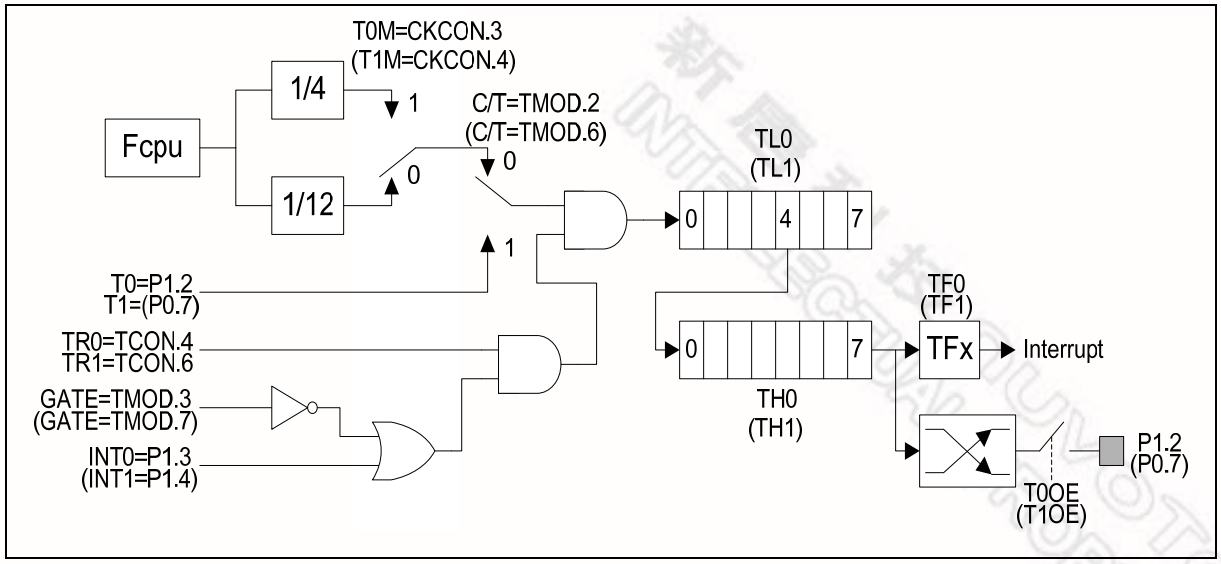

Figure 13-1: Timer/Counters 0 & 1 in Mode 0

13.1.3 Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16-bit counter, rather than a 13-bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

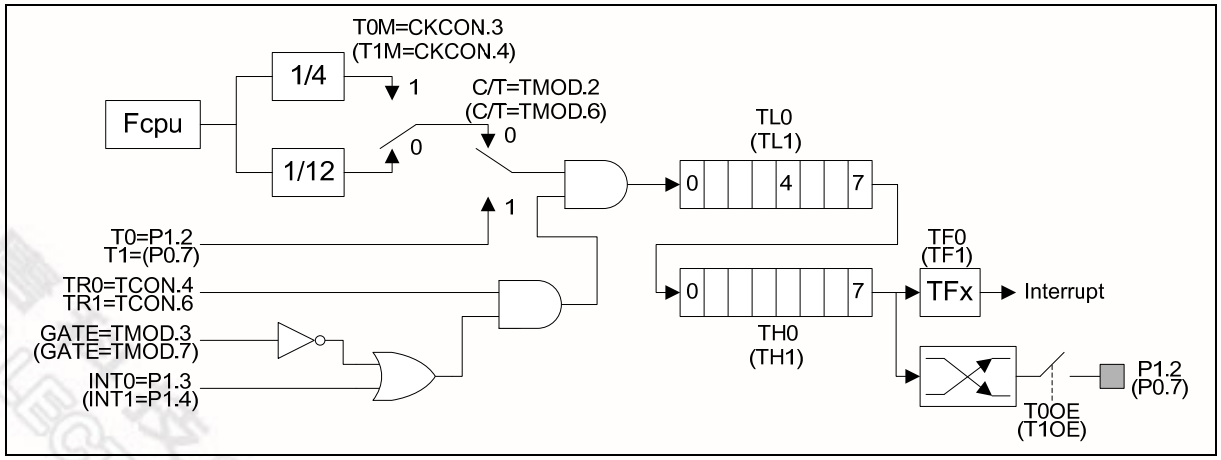

Figure 13-2: Timer/Counters 0 & 1 in Mode 1

16 SERIAL PORT (UART)

Serial port in the N79E825 series is a full duplex port. The N79E825 series provide the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode the N79E825 series generate the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the N79E825 series whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is Transmitted/Received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and the N79E825 series.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the N79E825 series and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide–by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter.

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

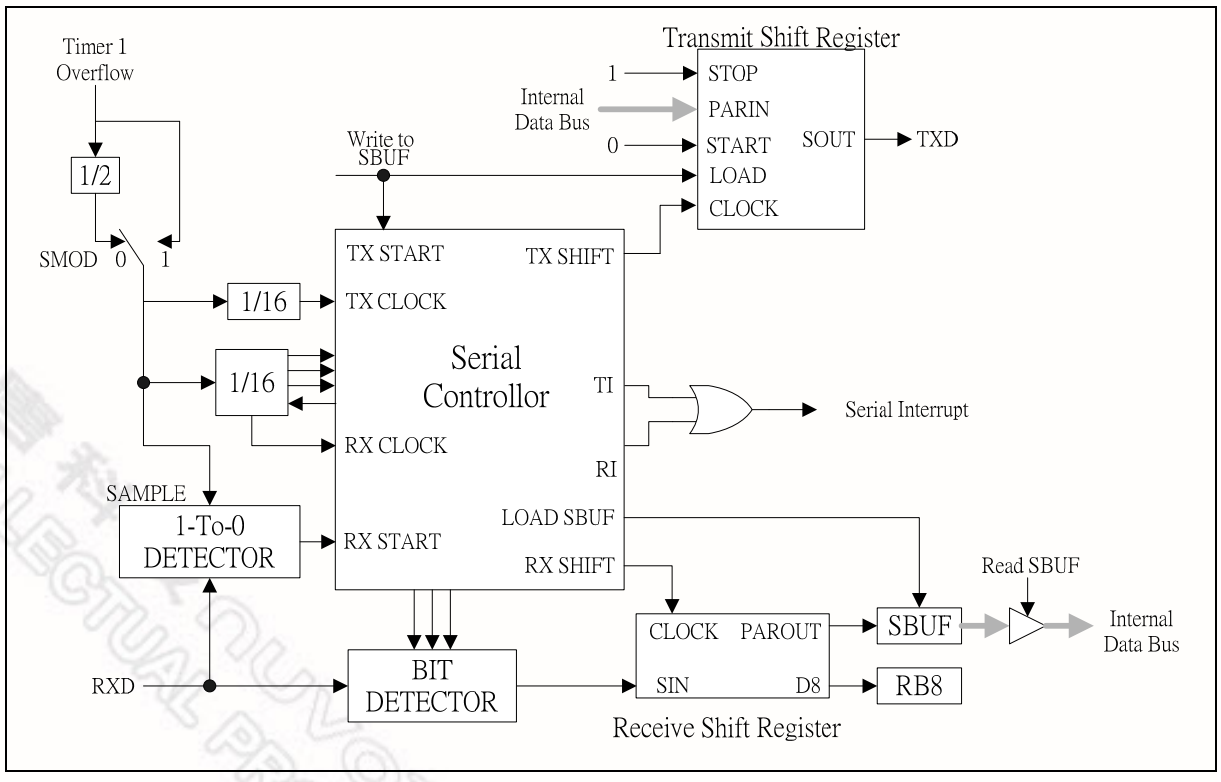

Figure 16-2: Serial Port Mode 1

The “weak” pull-up is turned on when the input port pin is logic “1” level or itself is logic “1”, and it provides the most source current for a quasi-bidirectional pin that output is “1” or port latch is logic “0”’.

The “very weak” pull-up is turned on when the port latch is logic “1”. If port latch is logic “0”, it will be turned off. The very weak pull-up is support a very small current that will pull the pin high if it is left floating. And the quasi-bidirectional port configuration is shown as below figure.

If port pin is low, it can drives large sink current for output, and it is similar with push-pull and open drain on sink current output.

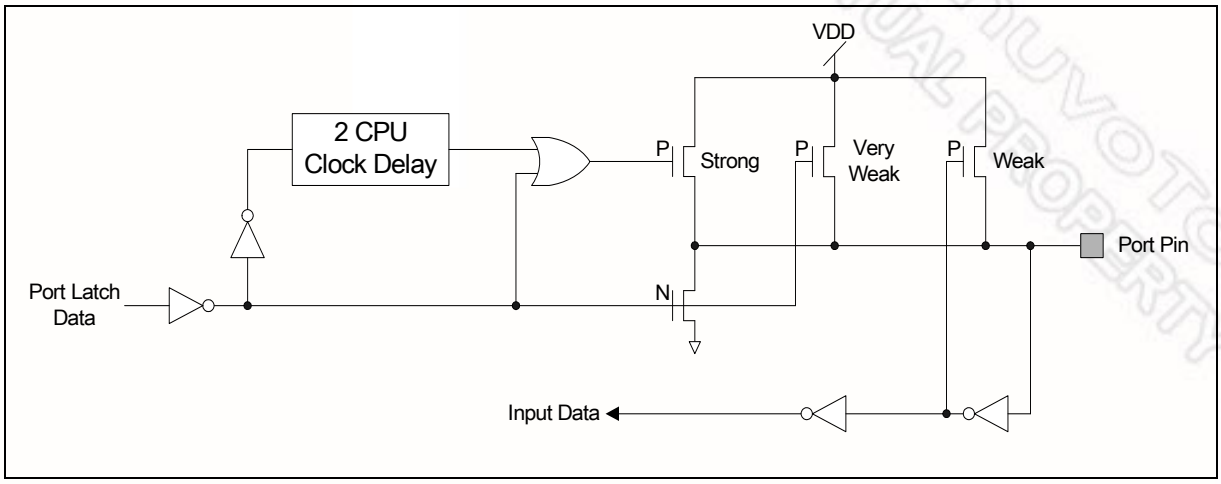

Figure 20-2: Quasi-Bidirectional Output

20.2 Open Drain Output Configuration

To configure this mode is turned off all pull-ups. If used similar as a logic output, the port must has an external pull-up resister. The open drain port configuration is shown as below.

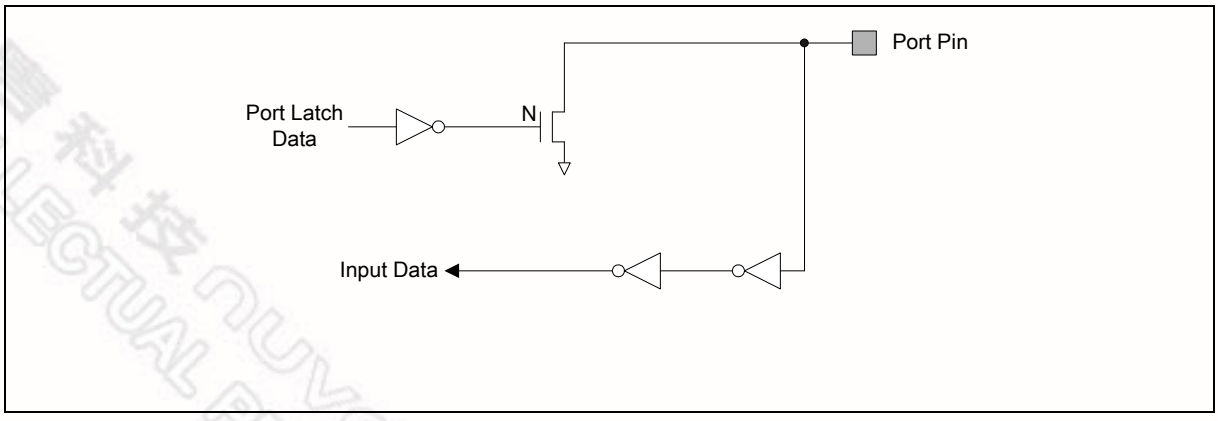

Figure 20-3: Open Drain Output

22 POWER MONITORING FUNCTION

Power-On Detect and Brownout are two additional power monitoring functions implemented in N79E825 series to prevent incorrect operation during power up and power drop or loss.

22.1 Power On Detect

The Power–On Detect function is a designed to detect power up after power voltage reaches to a level where Brownout Detect can work. After power on detect, the POR (PCON.4) will be set to “1” to indicate an initial power up condition. The POR flag will be cleared by software.

22.2 Brownout Detect

The Brownout Detect function is detect power voltage is drops to brownout voltage level, and allows preventing some process work or indicate power warming. The N79E825 series have two brownout voltage levels to select by BOV (CONFIG1.4). If BOV =0 that brownout voltage level is 3.8V, If BOV = 1 that brownout voltage level is 2.5V. When the Brownout voltage is drop to select level, the brownout detector will detect and keeps this active until VDD is returns to above brownout Detect voltage. The Brownout Detect block is as follow.

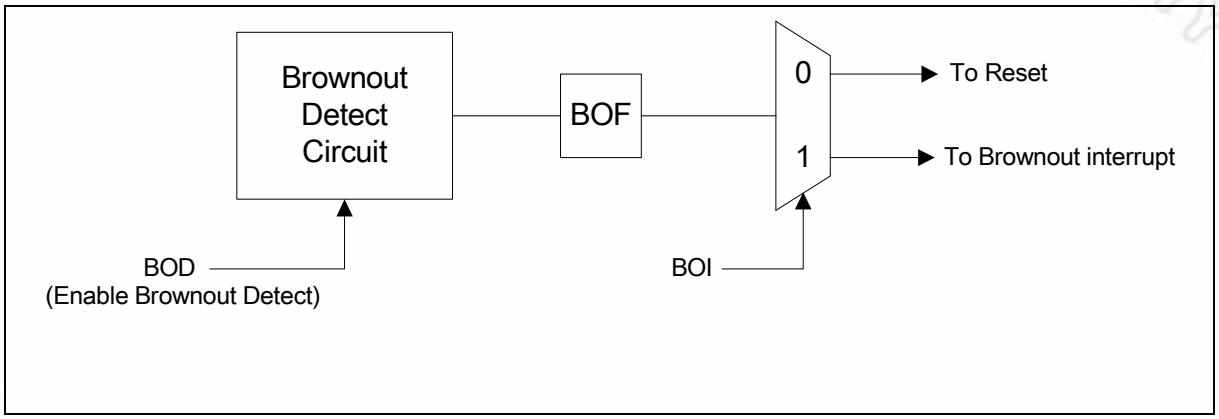

Figure 22-1: Brownout Detect Block

When Brownout Detect is enabled by BOD (AUXR1.6), the BOF (PCON.5) flag will be set and brownout reset will occur. If BOI (AUXR1.5) is set to “1”, the brownout detect will cause interrupt via the EA (IE.7) and EBO (IE.5) bits is set. BOF is cleared by software.

In order to guarantee a correct detection of Brownout, The VDD fall time must be slower than 50mV/us, and rise time is slower than 2mV/us to ensure a proper reset.

The N79E825 series devices support brake function which can be activated by software or external pin (P0.2). The Brake function is controlled by the PWMCON2 register. The setting and details description of software brake and external pin brake can be found at the brake condition table at the SFR section.

As for external brake, the user program can poll the brake flag (BKF) or enable PWM's brake interrupt to determine when the external Brake Pin is asserted and causes a brake to occur. The brake pin (P0.2) can be set to trigger the brake function by either low or high level, by clearing or setting the PWMCON2.6 (BKPS) bit respectively. The details description of varies brake functions can be found in the brake condition table.

Since the Brake Pin being asserted will automatically clear the Run bit of PWMCON1.7 and BKF (PWMCON3.0) flag will be set, the user program can poll this bit or enable PWM's brake interrupt to determine when the Brake Pin causes a brake to occur. The other method for detecting a brake caused by the Brake Pin would be to tie the Brake Pin to one of the external interrupt pins. This latter approach is needed if the Brake signal is of insufficient length to ensure that it can be captured by a polling routine. When, after being asserted, the condition causing the brake is removed, the PWM outputs go to whatever state that had immediately prior to the brake. This means that in order to go from brake being asserted to having the PWM run without going through an indeterminate state, care must be taken. If the Brake Pin causes brake to be asserted, the following prototype code will allow the PWM to go from brake and then run smoothly after brake is released.

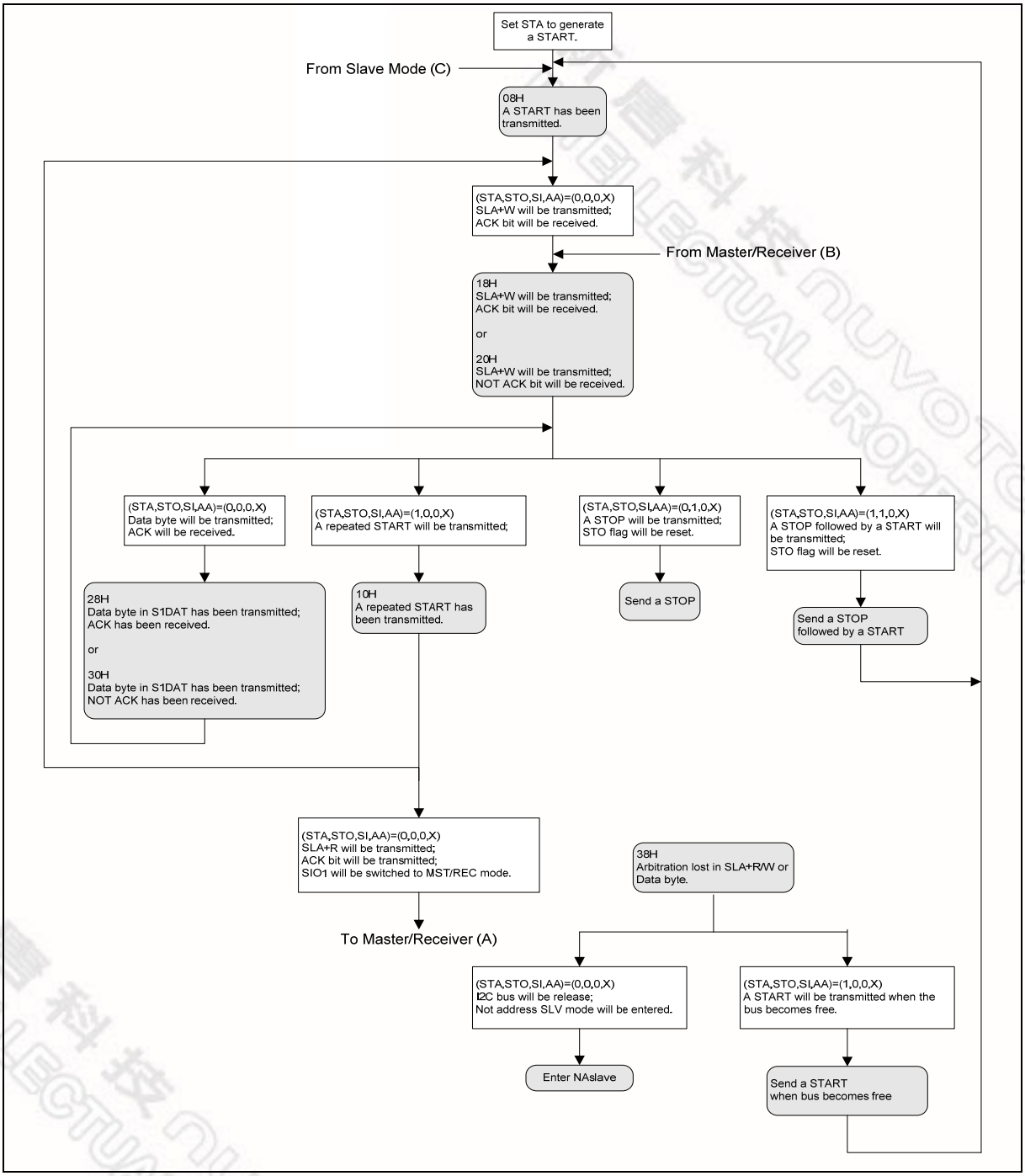

Figure 25-4: Master Transmitter Mode

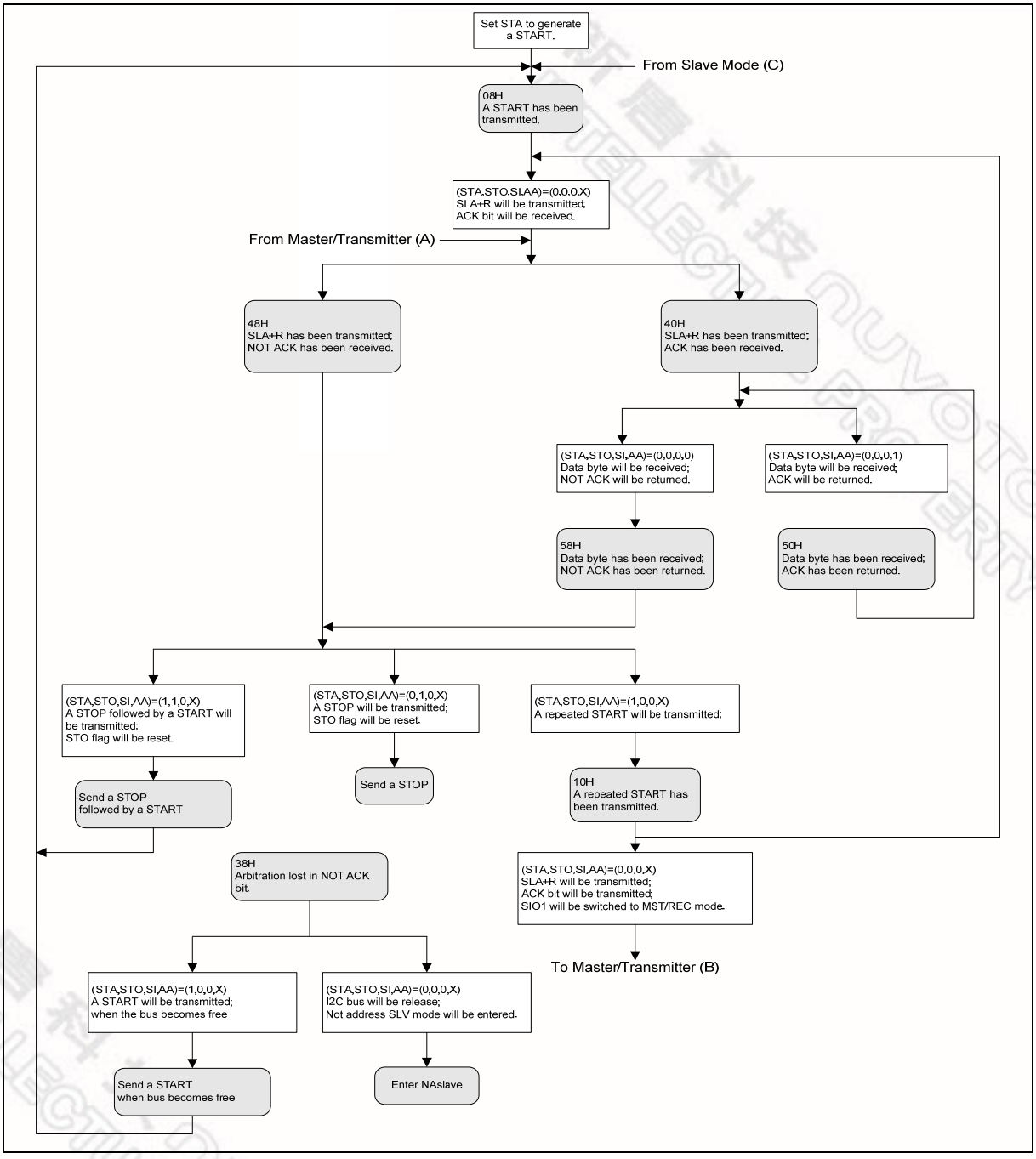

Figure 25-5: Master Receiver Mode

27 CONFIG BITS

The N79E825 series have two CONFIG bits (CONFIG1, CONFIG2) that must be define at power up and can not be set after the program start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG2) and those operations on it are described below. The data of these bytes may be read by the MOVC instruction at the addresses.

27.1 CONFIG1

CONFIG 1 :

7	6	5	4	3	2	1	0	
-	RPD	PRHI	BOV	-	-	Fosc1	Fosc0	CONFIG Bit

RPD: Reset Pin Disable Bit.
PRHI: Port Reset High or Low Bit.
BOV: Brownout voltage select Bit.
Fosc1: CPU oscillator type select Bit 1.
Fosc0: CPU oscillator type select Bit 0.

CONFIG Register 1

BIT	NAME	FUNCTION
7	-	Reserved.
6	RPD	Reset Pin Disable bit: 0: Enable Reset function of Pin 1.5. 1: Disable Reset function of Pin 1.5, and it to be used as an input port pin.
5	PRHI	Port Reset High or Low bit: 0: Port reset to low state. 1: Port reset to high state.
4	BOV	Brownout Voltage Select bit: 0: Brownout detect voltage is 3.8V. 1: Brownout detect voltage is 2.5V.