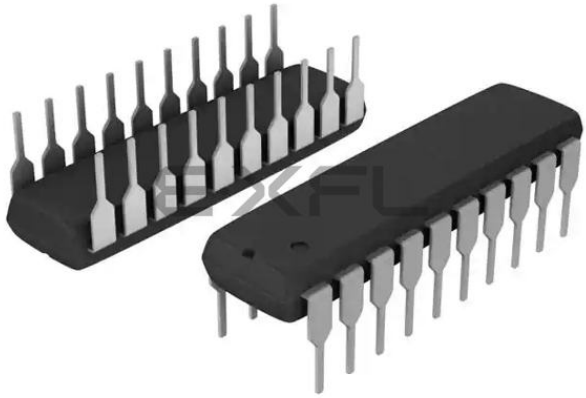


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n79e823adg

SYMBOL	DEFINITION	ADDRESS	MSB LSB BIT_ADDRESS, SYMBOL								RESET
IP1	Interrupt priority 1	F8H	(FF) -	(FE) -	(FD) PPWM	(FC) PWDI	(FB) PC2	(FA) PC1	(F9) PKB	(F8) PI2	xx000000B
IP1H	Interrupt high priority 1	F7H	-	-	PPWMH	PWDIH	PC2H	PC1H	PKBH	PI2H	xx000000B
P0IDS	Port 0 Digital Input Disable	F6H									00000000B
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	00000000B
EIE	Interrupt enable 1	E8H	(EF) -	(EE) -	(ED) EPWM	(EC) EWDI	(EB) EC2	(EA) EC1	(E9) EKB	(E8) EI2C	xx000000B
ADCH	ADC converter result	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	xxxxxxxxB
ADCCON	ADC control register	E1H	ADC.1	ADC.0	ADCEX	ADCI	ADCS	RCCLK	AADR1	AADR0	xx000x00B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	00000000B
PWMCON2	PWM control register 2	DFH	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B	00000000B
PWM3L	PWM 3 low bits register	DEH	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0	00000000B
PWM2L	PWM 2 low bits register	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	00000000B
PWMCON1	PWM control register 1	DCH	PWMRUN	load	CF	CLRPWM	PWM3I	PWM2I	PWM1I	PWM0I	00000000B
PWM1L	PWM 1 low bits register	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	00000000B
PWM0L	PWM 0 low bits register	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	00000000B
PWMPL	PWM counter low register	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	00000000B
WDCON	Watch-Dog control	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	0x000000B
PWMCON3	PWM control register 3	D7H	-	-	-	-	-	-	-	BKF	xxxxxxx0B
PWM3H	PWM 3 high bits register	D6H	-	-	-	-	-	-	PWM3.9	PWM3.8	xxxxxx00B
PWM2H	PWM 2 high bits register	D5H	-	-	-	-	-	-	PWM2.9	PWM2.8	xxxxxx00B
PWM1H	PWM 1 high bits register	D3H	-	-	-	-	-	-	PWM1.9	PWM1.8	xxxxxx00B
PWM0H	PWM 0 high bits register	D2H	-	-	-	-	-	-	PWM0.9	PWM0.8	xxxxxx00B
PWMPH	PWM counter high register	D1H	-	-	-	-	-	-	PWMP0.9	PWMP0.8	xxxxxx00B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	00000000B
NVMDATA	NVM Data	CFH									00000000B
NVMCON	NVM Control	CEH	EER	EWR	-	-	-	-	-	-	00000000B
TA	Timed Access Protection	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	11111111B
NVMADDR	NVM address	C6H									00000000B
I2ADDR	I2C address1	C1H	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxxxxx0B
I2CON	I2C Control register	C0H	(C7) -	(C6) ENS1	(C5) STA	(C4) STO	(C3) SI	(C2) AA	(C1) -	(C0) -	x00000xxB
I2TIMER	I2C Timer Counter register	BFH	-	-	-	-	-	ENTI	DIV4	TIF	00000000B
I2CLK	I2C Clock Rate	BEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	00000000B
I2STATUS		BDH									1111000B
I2DAT		BCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxxxxxxB
SADEN	Slave address mask	B9H									00000000B
IP0	Interrupt priority	B8H	(BF) -	(BE) PADC	(BD) PBO	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x0000000B
IP0H	Interrupt high priority	B7H	-	PADCH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H	x0000000B
P2M2	Port 2 output mode 2	B6H	-	-	-	-	-	-	P2M2.1	P2M2.0	xxxxxx00B
P2M1	Port 2 output mode 1	B5H	P2S	P1S	P0S	ENCLK	T1OE	T0OE	P2M1.1	P2M1.0	00000000B
P1M2	Port 1 output mode 2	B4H	P1M2.7	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	00000000B
P1M1	Port 1 output mode 1	B3H	P1M1.7	P1M1.6	-	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	00000000B
P0M2	Port 0 output mode 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	00000000B
P0M1	Port 0 output mode 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	00000000B

Continued

BIT	NAME	FUNCTION
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

Continued .

BIT	NAME	FUNCTION
2	OE2	Output enable: 1: The comparator output is connected to the CMP2 pin if the comparator is enabled (CE2 = 1). This output is asynchronous to the CPU clock.
1	CO2	Comparator output: Synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CE2 = 0).
0	CMF2	Comparator interrupt flag: This bit is set by hardware whenever the comparator output CO2 changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CE2 = 0).

PORT 0 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0

Mnemonic: P0M1 Address: B1h

BIT	NAME	FUNCTION
7-0	P0M1.[7:0]	To control the output configuration of P0 bits [7:0]

PORT 0 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0

Mnemonic: P0M2 Address: B2h

BIT	NAME	FUNCTION
7-0	P0M2.[7:0]	To control the output configuration of P0 bits [7:0]

PORT 1 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P1M1.7	P1M1.6	-	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0

Mnemonic: P1M1 Address: B3h

BIT	NAME	FUNCTION
7-0	P1M1.[7:0]	To control the output configuration of P1 bits [7:0]

PORT 1 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P1M2.7	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0

Mnemonic: P1M2 Address: B4h

PWM 1 HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM1.9	PWM1.8

Mnemonic: PWM1H Address: D3h

BIT	NAME	FUNCTION
7~2	-	Reserved.
1~0	PWM1.[9:8]	The PWM 1 High Bits Register bit 9~8.

PWM 2 HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM2.9	PWM2.8

Mnemonic: PWM2H Address: D5h

BIT	NAME	FUNCTION
7~2	-	Reserved.
1~0	PWM2.[9:8]	The PWM 2 High Bits Register bit 9~8.

PWM 3 HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM3.9	PWM3.8

Mnemonic: PWM3H Address: D6h

BIT	NAME	FUNCTION
7~2	-	Reserved.
1~0	PWM3.[9:8]	The PWM 3 High Bits Register bit 9~8.

PWM CONTROL REGISTER 3

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	BKF

Mnemonic: PWMCON3 Address: D7h

BIT	NAME	FUNCTION
7-6	-	Reserved.
0	BKF	The external brake pin Flag. 0: The PWM is not brake. 1: The PWM is brake by external brake pin. It will be cleared by software.

WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	WDRUN	POR	WD1	WD0	WDIF	WTRF	EWRST	WDCLR

Mnemonic: WDCON Address: D8h

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>7</td><td>WDRUN</td><td>0: The Watchdog is stopped.
1: The Watchdog is running.</td></tr>
<tr><td>6</td><td>-</td><td>Reserved.</td></tr>
<tr><td>5</td><td>WD1</td><td rowspan="2">Watchdog Timer Time-out Select bits. These bits determine the time-out period of the watchdog timer. The reset time-out period is 512 clocks longer than the watchdog time-out.

<table>
<tr><th>WD1</th><th>WD0</th><th>Interrupt time-out</th><th>Reset time-out</th></tr>
<tr><td>0</td><td>0</td><td>2^{17}</td><td>2^{17} + 512</td></tr>
<tr><td>0</td><td>1</td><td>2^{20}</td><td>2^{20} + 512</td></tr>
<tr><td>1</td><td>0</td><td>2^{23}</td><td>2^{23} + 512</td></tr>
<tr><td>1</td><td>1</td><td>2^{26}</td><td>2^{26} + 512</td></tr>
</table></td></tr>
<tr><td>4</td><td>WD0</td></tr>
<tr><td>3</td><td>WDIF</td><td>Watchdog Timer Interrupt Flag
0: If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
1: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred.</td></tr>
<tr><td>2</td><td>WTRF</td><td>Watchdog Timer Reset Flag
1: Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWRST = 0, the watchdog timer will have no affect on this bit.</td></tr>
<tr><td>1</td><td>EWRST</td><td>0: Disable Watchdog Timer Reset.
1: Enable Watchdog Timer Reset.</td></tr>
<tr><td>0</td><td>WDCLR</td><td>Reset Watchdog Timer
This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWRST before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWRST is set. This bit is self-clearing by hardware.</td></tr>
</table>

The WDCON SFR is set to 0x000000B on a reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by an external reset. EWRST (WDCON.1) is set to 0 on a Power-on reset, reset pin reset, and Watch Dog Timer reset.

All the bits in this SFR have unrestricted read access. WDRUN, WD0, WD1, EWRST, WDIF and WDCLR require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

EXTENDED INTERRUPT PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	-	PPWM	PWDI	PC2	PC1	PKB	PI2

Mnemonic: IP1 Address: F8h

BIT	NAME	FUNCTION
7	-	Reserved.
6	-	Reserved.
5	PPWM	1: To set interrupt priority of PWM's external brake is higher priority level.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3	PC2	1: To set interrupt priority of Comparator 2 is higher priority level.
2	PC1	1: To set interrupt priority of Comparator 1 is higher priority level.
1	PKB	1: To set interrupt priority of Keypad is higher priority level.
0	PI2	1: To set interrupt priority of I2C is higher priority level.

Continued

OP-CODE	HEX CODE	BYTES	N79E825 SERIES MACHINE CYCLE	N79E825 SERIES CLOCK CYCLES	8032 CLOCK CYCLES	N79E825 SERIES VS. 8032 SPEED RATIO
SJMP rel	80	2	3	12	24	2
JZ rel	60	2	3	12	24	2
JNZ rel	70	2	3	12	24	2
JC rel	40	2	3	12	24	2
JNC rel	50	2	3	12	24	2
JB bit, rel	20	3	4	16	24	1.5
JNB bit, rel	30	3	4	16	24	1.5
JBC bit, rel	10	3	4	16	24	1.5
CJNE A, direct, rel	B5	3	4	16	24	1.5
CJNE A, #data, rel	B4	3	4	16	24	1.5
CJNE @R0, #data, rel	B6	3	4	16	24	1.5
CJNE @R1, #data, rel	B7	3	4	16	24	1.5
CJNE R0, #data, rel	B8	3	4	16	24	1.5
CJNE R1, #data, rel	B9	3	4	16	24	1.5
CJNE R2, #data, rel	BA	3	4	16	24	1.5
CJNE R3, #data, rel	BB	3	4	16	24	1.5
CJNE R4, #data, rel	BC	3	4	16	24	1.5
CJNE R5, #data, rel	BD	3	4	16	24	1.5
CJNE R6, #data, rel	BE	3	4	16	24	1.5
CJNE R7, #data, rel	BF	3	4	16	24	1.5
DJNZ R0, rel	D8	2	3	12	24	2
DJNZ R1, rel	D9	2	3	12	24	2
DJNZ R5, rel	DD	2	3	12	24	2
DJNZ R2, rel	DA	2	3	12	24	2
DJNZ R3, rel	DB	2	3	12	24	2
DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5

Table 9-1: Instruction Set for N79E825/824

10 POWER MANAGEMENT

The N79E825 series has several features that help the user to control the power consumption of the device. These modes are discussed in the next two sections.

10.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer, I2C, PWM and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle Mode.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a low on the external /RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held low for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the N79E825 series are exiting from an Idle Mode with a reset, the instruction following the one which put the device into Idle Mode is not executed. So there is no danger of unexpected writes.

10.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The port pins output the values held by their respective SFRs.

The N79E825 series will exit the Power Down mode with a reset or by an external interrupt pin enabled as level detected. An external reset can be used to exit the Power down state. The low on /RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode when its clock source is external OSC or crystal.

The sources that can wake up from the power down mode are external interrupts, keyboard interrupt (KBI), brownout reset (BOR), and comparator interrupt (CMF1, CMF2).

The N79E825 series can be waken up from the Power Down mode by forcing an external interrupt pin activation, provided the corresponding interrupt is enabled, while the global enable (EA) bit is set. If these conditions are met, then either a low-level or a falling-edge at external interrupt pin will re-start the oscillator. The device will then execute the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there. During Power down mode, if AUXR1.LPBOV = 1 and AUXR1.BOD = 0, the internal RC clock will be enabled

12 INTERRUPTS

The N79E825 series have four priority level interrupts structure with 13 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

12.1 Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

The Serial block can generate interrupt on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits by software.

All the bits that generate interrupts can be set or reset by software, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all interrupts.

The ADC can generate interrupt after finished ADC converter. There is one interrupt source, which is obtained by the ADCI bit in the ADCCON SFR. This bit is not automatically cleared by the hardware, and the user will have to clear this bit using software.

The two comparators can generate interrupt after comparator output has toggle occurs by CMF1 and CMF2. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

The I2C function can generate interrupt, if EI2C and EA bits are enabled, when SI Flag is set due to a new I2C status code is generated, SI flag is generated by hardware and must be cleared by software.

The PWM function can generate interrupt by BKF flag, after external brake pin has brake occurred. This bit will be cleared by software.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.
2. The current polling cycle is the last machine cycle of the instruction currently being execute.
3. The current instruction does not involve a write to IE, EIE, IP0, IP0H, IP1 or IPH1 registers and is

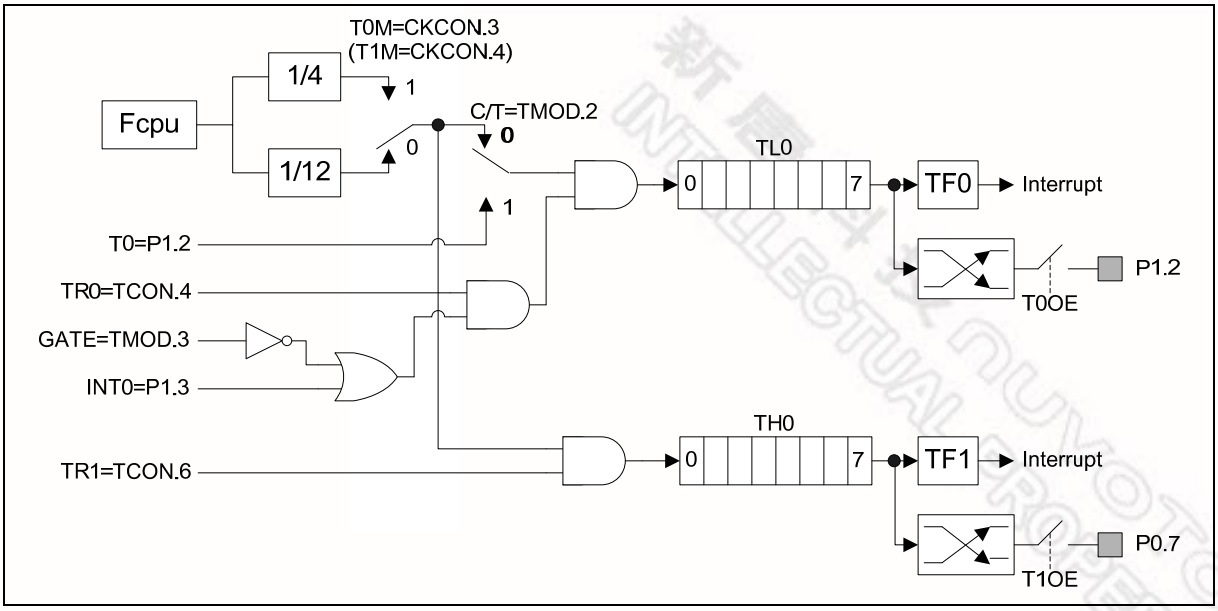


Figure 13-4: Timer/Counter Mode 3

Example 5: Invalid Access

```
MOV     TA, #0AAh       ;3 M/C
NOP                     ;1 M/C
MOV     TA, #055h       ;3 M/C
SETB    EWT             ;2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycles window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

23 PULSE-WIDTH-MODULATED (PWM) OUTPUTS

The N79E825 series have four Pulse Width Modulated (PWM) channels, and the PWM outputs are PWM0 (P0.1), PWM1 (P1.6), PWM2 (P1.7) and PWM3 (P0.0). The initial PWM outputs level correspondingly depend on the PRHI level set prior to the chip reset. When PRHI set to high, PWM output will initialize to high after chip reset; if PRHI set to low, PWM output will be initialize to low after chip reset.

The N79E825 series support 10-bits down counter with cpu clock as its input. The PWM counter clock, has the same frequency as the clock source $F_{CPU} = F_{OSC}$. When the counter reaches underflow it will automatic reloaded from counter register. The PWM frequency is given by: $f_{PWM} = F_{CPU} / (PWMP+1)$, where PWMP is 10-bits register of PWMPH.1, PWMPH.0 and PWMPL.7~PWMPL.0.

The counter register will be loaded with the PWMP register value when PWMRUN, load and CF are equal to 1; the load bit will be automatically cleared to zero on the next clock cycle, and at the same time the counter register value will be loaded to the 10 bits down counter. CF flag is 10-bits down counter reaches underflow, the CF flag will be cleared by software.

The pulse width of each PWM output is determined by the Compare registers of PWM0L through PWM3L and PWM0H through PWM3H. When PWM compare register is greater than 10-bits counter register, the PWM output is low. Load bit has to be set to 1 for alteration of PWMn width. After the new values are written to the PWMn registers, and if load bit is set to 1, the new PWMn values will be loaded to the PWMn registers upon the next underflow. The PWM output high pulses width is given by:

t_{HI} = (PWMP – PWMn+1). *Notice, if compare register is set to 000H, the PWMn output will stay at high, and if compare register is set to 3FFH, the PWMn output will stuck at low until there is a change in the compare register.*

The N79E825 series devices support brake function which can be activated by software or external pin (P0.2). The Brake function is controlled by the PWMCON2 register. The setting and details description of software brake and external pin brake can be found at the brake condition table at the SFR section.

As for external brake, the user program can poll the brake flag (BKF) or enable PWM's brake interrupt to determine when the external Brake Pin is asserted and causes a brake to occur. The brake pin (P0.2) can be set to trigger the brake function by either low or high level, by clearing or setting the PWMCON2.6 (BKPS) bit respectively. The details description of varies brake functions can be found in the brake condition table.

Since the Brake Pin being asserted will automatically clear the Run bit of PWMCON1.7 and BKF (PWMCON3.0) flag will be set, the user program can poll this bit or enable PWM's brake interrupt to determine when the Brake Pin causes a brake to occur. The other method for detecting a brake caused by the Brake Pin would be to tie the Brake Pin to one of the external interrupt pins. This latter approach is needed if the Brake signal is of insufficient length to ensure that it can be captured by a polling routine. When, after being asserted, the condition causing the brake is removed, the PWM outputs go to whatever state that had immediately prior to the brake. This means that in order to go from brake being asserted to having the PWM run without going through an indeterminate state, care must be taken. If the Brake Pin causes brake to be asserted, the following prototype code will allow the PWM to go from brake and then run smoothly after brake is released.

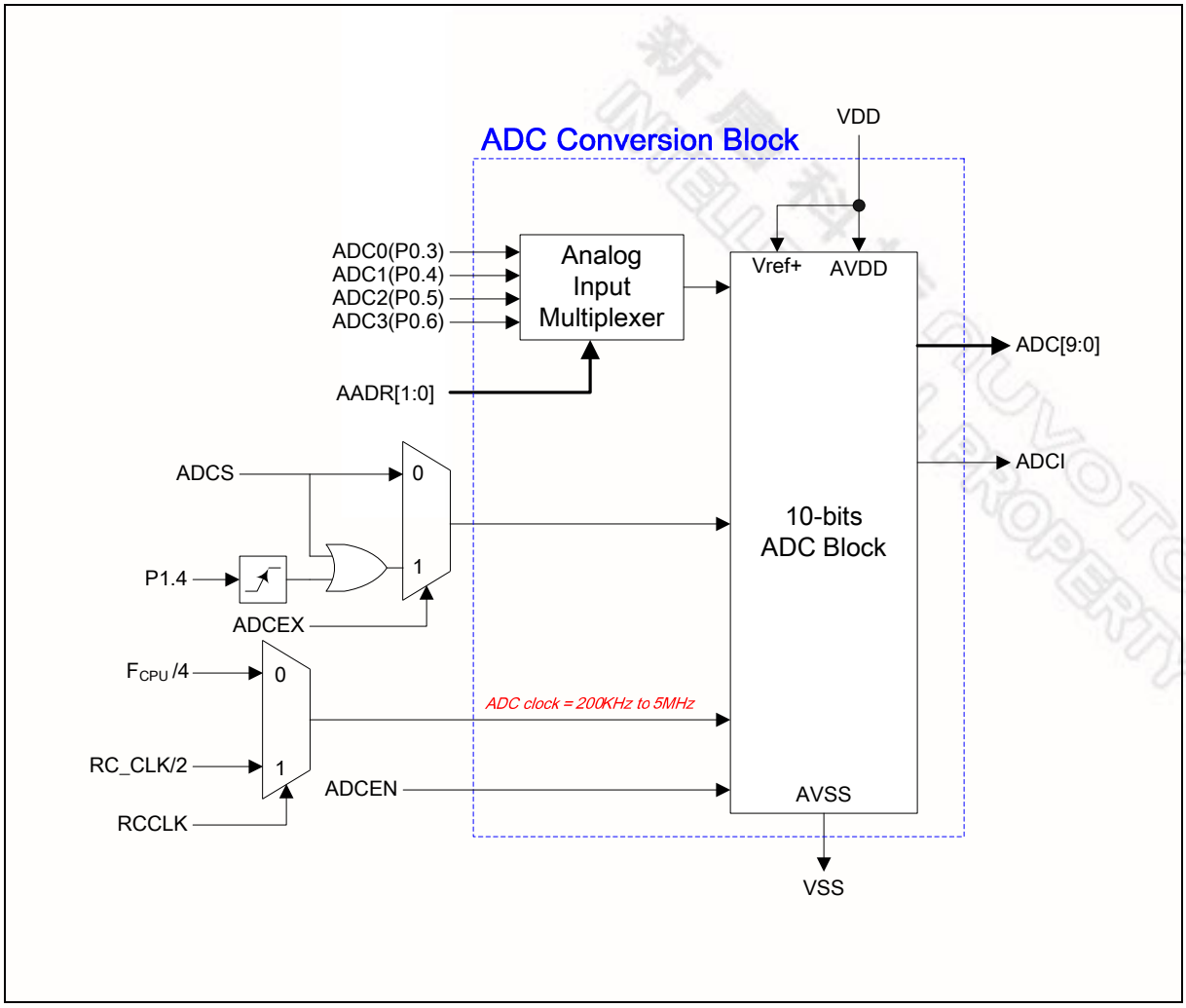


Figure 24-2: The ADC Block Diagram

26 ICP(IN-CIRCUIT PROGRAM) FLASH PROGRAM

The contexts of flash in N79E825 series are empty by default. User must program the flash EPROM by external Writer device or by ICP (In-Circuit Program) tool.

In the ICP tool, the user must take note of ICP's program pins used in system board. In some application circuits, the pins are located at P1.5, P0.4 and P0.5, as below figure. During ICP programming, P1.5 must be set to high voltage (~10.5V), and keeping this voltage to update code, data and/or configure CONFIG bits. After programming completion, the high voltage of P1.5 should be released. So, it is highly recommended user power off then power on after ICP programming has completed on the system board.

Upon entry into ICP program mode, all pin will be set to quasi-bidirectional mode, and output to level "1".

The N79E825 series support programming of Flash EPROM (**16K/8K/4K/2K** bytes AP Flash EPROM) and NVM data memory (**256** bytes). User has the option to program the AP flash and NVM either individually or both.

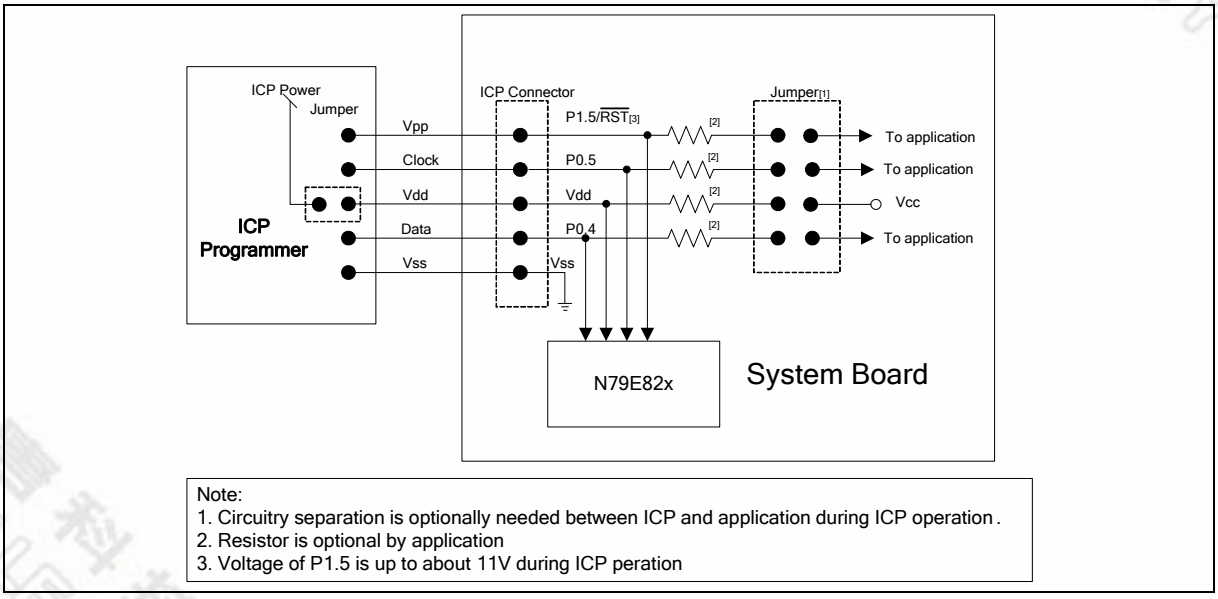


Figure 26-1: Application Circuit of ICP

Note: 1. When using ICP to upgrade code, the P1.5, P0.4 and P0.5 must be taken within design system board.

2. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.

3. It is recommended that user performs erase function and programming configure bits continuously without any interruption.

28 ELECTRICAL CHARACTERISTICS

28.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Operating Temperature	TA	-40	+85	°C
Storage Temperature	Tst	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current suck by a I/O pin			25	mA
Maximum Current sourced by a I/O pin			25	mA
Maximum Current suck by total I/O pins			75	mA
Maximum Current sourced by total I/O pins			75	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability

DC ELECTRICAL CHARACTERISTICS, continued

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4	V	V_{DD} = 3.0V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2	V	V_{DD} = 3.0V
Input High Voltage P0, P1, P2 (TTL input)	V_{IH1}	2.4	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.0	-	V_{DD} +0.2	V	V_{DD} = 3.0V
Negative going threshold (Schmitt input)	V_{ILS}	-0.5	-	$0.3V_{DD}$	V	
Positive going threshold (Schmitt input)	V_{IHS}	$0.7V_{DD}$	-	V_{DD}+0.5	V	
Hysteresis voltage	V_{HY}		$0.2V_{DD}$		V	
Source Current P0, P1, P2 (Quasi-bidirectional Mode)	I_{sr1}	-180	-230	-360	uA	V_{DD} = 4.5V, V_S = 2.4V
Sink Current P0, P1, P2 (Quasi-bidirectional Mode)	I_{SK2}	13	23	24	mA	V_{DD} = 4.5V, V_S = 0.45V
Output Low Voltage P0, P1, P2 (PUSH-PULL Mode)	V_{OL1}	-	0.5	0.9	V	V_{DD} = 4.5V, I_{OL} = 20 mA
		-	0.1	0.4	V	V_{DD} = 2.7V, I_{OL} = 3.2 mA
Output High Voltage P0, P1, P2 (PUSH-PULL Mode)	V_{OH}	2.4	3.4	-	V	V_{DD} = 4.5V, I_{OH} = -16mA
		1.9	2.4	-	V	V_{DD} = 2.7V, I_{OH} = -3.2mA
Brownout voltage with BOV=1	$V_{BO2.5}$	2.4	-	2.7	V	TA = -0 to 70°C
Brownout voltage with BOV=0	$V_{BO3.8}$	3.5	-	4.0	V	TA = -0 to 70°C
Brown-Out Current			1		mA	5.0V/20MHz XTAL P1.5 (RST) tie to VDD
Brown-Out Current + Power saving			90		μA	5.0V/20MHz XTAL P1.5 (RST) tie to VDD
Comparator Reference Voltage	Vref	1.02	1.20	1.31	V	

Notes: *1. /RST pin is a Schmitt trigger input.

28.6 EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	12.5	-	-	nS	
Clock Low Time	t_{CLCX}	12.5	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

28.7 AC SPECIFICATION

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	20	MHz

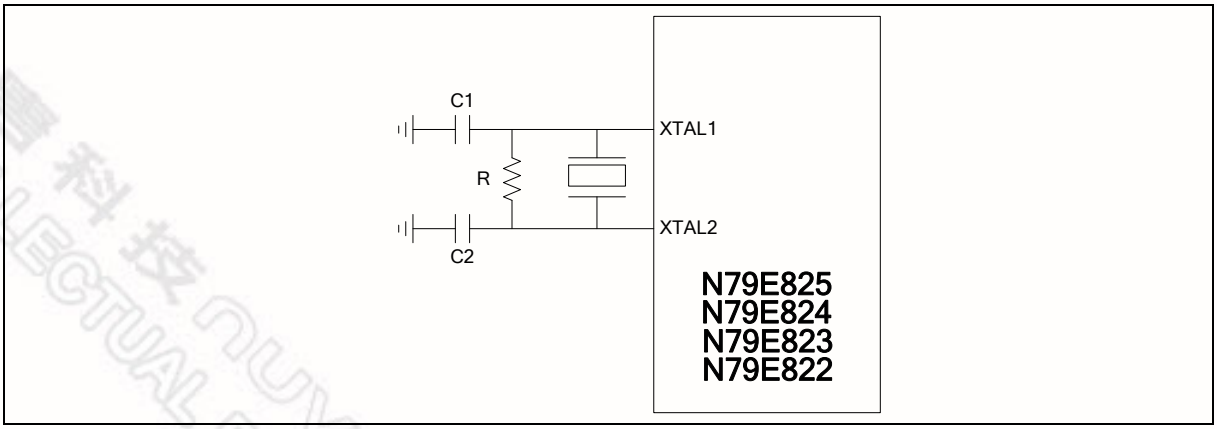
28.8 Internal RC OSC Specification

Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
On-chip RC oscillator	-	± 50%	-	%	V_{DD}=2.7V~5.5V, TA = -40°C ~85°C

28.9 TYPICAL APPLICATION CIRCUITS

CRYSTAL	C1	C2	R
4MHz ~ 20 MHz	without	without	without

The above table shows the reference values for crystal applications.



30 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Dec. 03, 2009	-	Initial Issued
A2	Aug. 05, 2010	Page 124	Modify SSOP20 Package.