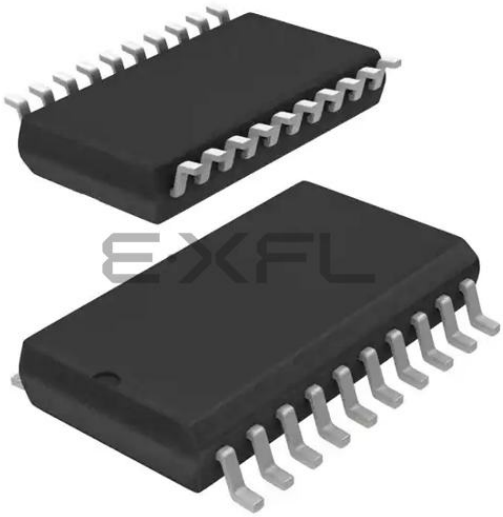
Nuvoton Technology Corporation - N79E825ASG Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n79e825asg

2 FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller up to 20MHz when V_{DD}=4.5V to 5.5V, 12MHz when V_{DD}=2.7V to 5.5V
- **16K/8K/4K/2K** bytes of AP Flash EPROM, with ICP and external writer programmable mode.
- **256** bytes of on-chip RAM.
- **256** bytes NVM Data Flash EPROM for customer data storage used and 10K writer cycles; Data Flash program/erase V_{DD}=3.0V to 5.5V
- Instruction-set compatible with MCS-51.
- Built-in internal RC oscillator (about 6MHz)
- Two 8-bit bi-directional and one 2-bit bi-directional ports.
- Two 16-bit timer/counters.
- 13 interrupts source with four levels of priority.
- One enhanced full duplex serial port with framing error detection and automatic address recognition.
- The 4 outputs mode and TTL/Schmitt trigger selectable Port.
- Programmable Watchdog Timer.
- Four-channel 10-bit PWM (Pulse Width Modulator).
- Four-channel multiplexed with 10-bits A/D convert.
- One I2C communication port (Master / Slave).
- Eight keypad interrupt inputs.
- Two analog comparators.
- Configurable on-chip oscillator.
- LED drive capability (20mA) on all port pins.
- Brownout voltage detect interrupt and reset.
- Development Tools:
  - JTAG ICE(In Circuit Emulation) tool
  - ICP(In Circuit Programming) writer
- Packages:

N79E825ADG ---- PDIP20
N79E825ASG ---- SOP20
N79E825ARG ---- SSOP20
N79E824ADG ---- PDIP20
N79E824ASG ---- SOP20
N79E824ARG ---- SSOP20
N79E823ADG ---- PDIP20
N79E823ASG ---- SOP20
N79E823ARG ---- SSOP20
N79E822ADG ---- PDIP20

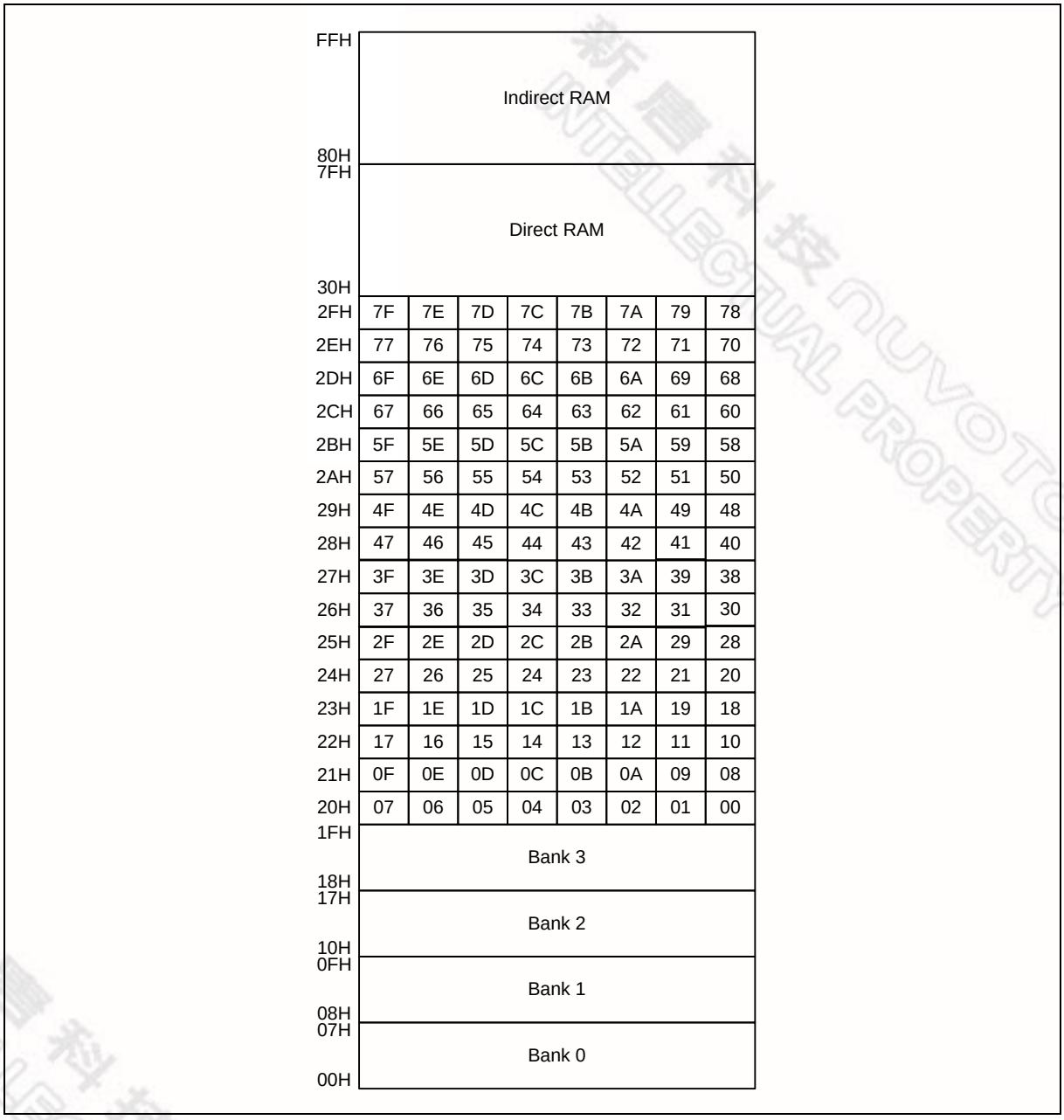

Figure 7-3: Scratch pad RAM

8 SPECIAL FUNCTION REGISTERS

The N79E825 series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The N79E825 series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

F8	IP1							
F0	B						P0ID	IP1H
E8	EIE							
E0	ACC	ADCCON	ADCH					
D8	WDCON	PWMPL	PWM0L	PWM1L	PWMCON1	PWM2L	PWM3L	PWMCON2
D0	PSW	PWMPH	PWM0H	PWM1H		PWM2H	PWM3H	PWMCON3
C8							NVMCON	NVMDAT
C0	I2CON	I2ADDR					NVMADDR	TA
B8	IP0	SADEN			I2DAT	I2STATUS	I2CLK	I2TIMER
B0		P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H
A8	IE	SADDR			CMP1	CMP2		
A0	P2	KBI	AUXR1					
98	SCON	SBUF						
90	P1					DIVM		
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH				PCON

Table 8-1: Special Function Register Location Table

Note: 1. The SFRs in the column with dark borders are bit-addressable

2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.

Continued .

BIT	NAME	FUNCTION
3	KBI.3	1: Enable P0.3 as a cause of a Keyboard interrupt.
2	KBI.2	1: Enable P0.2 as a cause of a Keyboard interrupt.
1	KBI.1	1: Enable P0.1 as a cause of a Keyboard interrupt.
0	KBI.0	1: Enable P0.0 as a cause of a Keyboard interrupt.

AUX FUNCTION REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	KBF	BOD	BOI	LPBOV	SRST	ADCEN	0	DPS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	KBF	Keyboard Interrupt Flag: 1: When any pin of port 0 that is enabled for the Keyboard Interrupt function goes low. Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.
5	BOI	Brown Out Interrupt: 0: Disable Brownout Detect Interrupt function and it will cause chip reset when BOF is set. 1: This prevents Brownout Detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOV	Low Power Brown Out Detect control: 0: When BOD is enable, the Brown Out detect is always turned on by normal run or Power Down mode. 1: When BOD is enable, the Brown Out detect circuit is turned on by Power Down mode. This control can help save 15/16 of the Brownout circuit power. When uC is in Power Down mode, the BOD will enable internal RC OSC (2MHz~0.5MHZ)
3	SRST	Software reset: 1: reset the chip as if a hardware reset occurred.
2	ADCEN	0: Disable ADC circuit. 1: Enable ADC circuit.
1	0	Reserved.
0	DPS	Dual Data Pointer Select 0: To select DPTR of standard 8051. 1: To select DPTR1

INTERRUPT ENABLE

I2C ADDRESS REGISTER

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	GC

Mnemonic: I2ADDR Address: C1h

BIT	NAME	FUNCTION
7~1	I2ADDR.[7:1]	I2C Address register: The 8051 uC can read from and write to this 8-bit, directly addressable SFR. The content of this register is irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own address. The I2C hardware will react if either of the address is matched.
0	GC	General Call Function. 0: Disable General Call Function. 1: Enable General Call Function.

NVM ADDRESS

Bit:	7	6	5	4	3	2	1	0
	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0

Mnemonic: NVMADDR Address: C6h

BIT	NAME	FUNCTION
7~0	NVMADDR.[7:0]	The NVM address: The register indicates NVM data memory of low byte address on On-Chip code memory space.

TIMED ACCESS

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

BIT	NAME	FUNCTION
7-0	TA.[7:0]	The Timed Access register: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

NVM CONTROL

Bit:	7	6	5	4	3	2	1	0
	EER	EWR	-	-	-	-	-	-

Mnemonic: NVMCON Address: CEh

```
TA      REG     C7H
WDCON   REG     D8H
MOV     TA, #AAH            ; To access protected bits
MOV     TA, #55H
SETB    WDCON.0             ; Reset watchdog timer
ORL     WDCON, #00110000B   ; Select 26 bits watchdog timer
MOV     TA, #AAH
MOV     TA, #55H
ORL     WDCON, #00000010B   ; Enable watchdog
```

PWMP COUNTER LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWMP.7	PWMP.6	PWMP.5	PWP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.1

Mnemonic: PWMPL Address: D9h

BIT	NAME	FUNCTION
7~0	PWMP.[7:0]	PWM Counter Low Bits Register.

PWM0 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.1

Mnemonic: PWM0L Address: DAh

BIT	NAME	FUNCTION
7~0	PWM0.[7:0]	PWM 0 Low Bits Register.

PWM1 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Mnemonic: PWM1L Address: DBh

BIT	NAME	FUNCTION
7~0	PWM1.[7:0]	PWM 1 Low Bits Register.

PWM CONTROL REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	Load	CF	CLRPWM	PWM3I	PWM2I	PWM1I	PWM0I

Mnemonic: PWMCON1 Address: DCh

BIT	NAME	FUNCTION
7	PWMRUN	0: The PWM is not running. 1: The PWM counter is running.
6	Load	0: The registers value of PWMP and PWMn are never loaded to counter and Comparator registers. 1: The PWMP and PWMn registers load value to counter and compare registers at the counter underflow. This bit is auto cleared by hardware at next clock cycle.
5	CF	0: The 10-bit counter down count is not underflow. 1: The 10-bit counter down count is underflow. This bit is Software clear.
4	CLRPWM	1: Clear 10-bit PWM counter to 000H. This bit is auto cleared by hardware.
3	PWM3I	0: PWM3 out is non-inverted. 1: PWM3 output is inverted.
2	PWM2I	0: PWM2 out is non-inverted. 1: PWM2 output is inverted.
1	PWM1I	0: PWM1 out is non-inverted. 1: PWM1 output is inverted.
0	PWM0I	0: PWM0 out is non-inverted. 1: PWM0 output is inverted.

PWM2 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2L Address: DDh

BIT	NAME	FUNCTION
7~0	PWM2.[7:0]	PWM 2 Low Bits Register.

PWM3 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0

Mnemonic: PWM3L Address: DEh

BIT	NAME	FUNCTION
7~0	PWM3.[7:0]	PWM 3 Low Bits Register.

PWM CONTROL REGISTER 2

Bit:	7	6	5	4	3	2	1	0
	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B

Mnemonic: PWMCON2 Address: DFh

BIT	NAME	FUNCTION
7-0	ACC.[7:0]	The A or ACC register is the standard 8052 accumulator

ADC CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	ADC.1	ADC.0	ADCEX	ADCI	ADCS	RCCLK	AADR1	AADR0

Mnemonic: ADCCON Address: E1h

BIT	NAME	FUNCTION
7	ADC.1	The ADC conversion result.
6	ADC.0	The ADC conversion result.
5	ADCEX	Enable STADC-triggered conversion 0: Conversion can only be started by software (i.e., by setting ADCS). 1: Conversion can be started by software or by a rising edge on STADC (pin P1.4).
4	ADCI	ADC Interrupt flag: This flag is set when the result of an A/D conversion is ready. This generates an ADC interrupt, if it is enabled. The flag may be cleared by the ISR. While this flag is 1, the ADC cannot start a new conversion. ADCI can not be set by software.
3	ADCS	ADC Start and Status: Set this bit to start an A/D conversion. It may also be set by STADC if ADCEX is 1. This signal remains high while the ADC is busy and is reset right after ADCI is set. Notes: 1. It is recommended to clear ADCI ***before*** ADCS is set. However, if ADCI is cleared and ADCS is set at the same time, a new A/D conversion may start on the same channel. 2. Software clearing of ADCS will abort conversion in progress. 3. ADC cannot start a new conversion while ADCS or ADCI is high.
2	RCCLK	0: The CPU clock is used as ADC clock. 1: The internal RC clock is used as ADC clock.
1	AADR1	The ADC input select. See table below.
0	AADR0	The ADC input select. See table below.

The ADCI and ADCS control the ADC conversion as below:

ADCI	ADCS	ADC STATUS
0	0	ADC not busy; A conversion can be started.
0	1	ADC busy; Start of a new conversion is blocked.
1	0	Conversion completed; Start of a new conversion requires ADCI = 0.
1	1	This is an internal temporary state that user can ignore it.

ADDC A, @R1	37	1	1	4	12	3

Continued

OP-CODE	HEX CODE	BYTES	N79E825 SERIES MACHINE CYCLE	N79E825 SERIES CLOCK CYCLES	8032 CLOCK CYCLES	N79E825 SERIES VS. 8032 SPEED RATIO
XCH A, R2	CA	1	1	4	12	3
XCH A, R3	CB	1	1	4	12	3
XCH A, R4	CC	1	1	4	12	3
XCH A, R5	CD	1	1	4	12	3
XCH A, R6	CE	1	1	4	12	3
XCH A, R7	CF	1	1	4	12	3
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3
XCHD A, @R0	D6	1	1	4	12	3
XCHD A, @R1	D7	1	1	4	12	3
XCH A, direct	C5	2	2	8	12	1.5
CLR C	C3	1	1	4	12	3
CLR bit	C2	2	2	8	12	1.5
SETB C	D3	1	1	4	12	3
SETB bit	D2	2	2	8	12	1.5
CPL C	B3	1	1	4	12	3
CPL bit	B2	2	2	8	12	1.5
ANL C, bit	82	2	2	8	24	3
ANL C, /bit	B0	2	2	6	24	3
ORL C, bit	72	2	2	8	24	3
ORL C, /bit	A0	2	2	6	24	3
MOV C, bit	A2	2	2	8	12	1.5
MOV bit, C	92	2	2	8	24	3
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	3	12	24	2
LCALL addr16	12	3	4	16	24	1.5
RET	22	1	2	8	24	3
RETI	32	1	2	8	24	3
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	3	12	24	2
LJMP addr16	02	3	4	16	24	1.5
JMP @A+DPTR	73	1	2	6	24	3

SFR RESET VALUE

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
P0	1111 1111B	I2DAT	xxxx xxxxB
SP	0000 0111B	I2STATUS	0000 0xxxB
DPL	0000 0000B	I2TIMER	0000 0000B
DPH	0000 0000B	I2CLK	0000 0000B
PCON	00xx 0000B	I2CON	0000 0000B
TCON	0000 0000B	I2ADDR	xxxx xxxxB
TMOD	0000 0000B	TA	1111 1111B
TL0	0000 0000B	PSW	0000 0000B
TL1	0000 0000B	PWMP1	xxxx xx00B
TH0	0000 0000B	PWM0H	xxxx xx00B
TH1	0000 0000B	PWM1H	xxxx xx00B
CKCON	0000 0000B	PWM2H	xxxx xx00B
P1	1111 xx11B	PWM3H	xxxx xx00B
DIVM	0000 0000B	WDCON	0x00 0000B
SCON	0000 0000B	PWMP0	0000 0000B
SBUF	xxxx xxxxB	PWM0L	0000 0000B
P2	xxx xx11B	PWM1L	0000 0000B
KBI	0000 0000B	PWMCON1	0000 0000B
AUXR1	0000 0000B	PWM2L	0000 0000B
IE	0000 0000B	PWM3L	0000 0000B
SADDR	0000 0000B	PWMCON2	0000 0000B
CMP1	0000 0000B	PWMCON3	xxxxxxx0B
CMP2	0000 0000B	ACC	0000 0000B
P0M1	0000 0000B	ADCCON	xx00 0x00B
P0M2	0000 0000B	ADCH	xxxx xxxxB
P1M1	0000 0000B	EIE	xx000 000B
P1M2	0000 0000B	B	0000 0000B
P2M1	0000 0000B	P0IDS	0000 0000B
P2M2	xxxx xx00B	IPH	xx00 0000B
IP0H	x000 0000B	IP1	xx00 0000B
IP0	x000 0000B	NVMADDR	0000 0000B
SADEN	0000 0000B	NVMDAT	0000 0000B
		NVMCON	00xx xxxxB

Table 11-1: SFR Reset Value

13 PROGRAMMABLE TIMERS/COUNTERS

The N79E825 series have two 16-bit programmable timer/counters and one programmable Watchdog Timer. The Watchdog Timer is operationally quite different from the other two timers. It's timer/counters have additional timer 0 or timer 1 overflow toggle output enable feature as compare to conventional timer/counters. This timer overflow toggle output can be configured to automatically toggle T0 or T1 pin output whenever a timer overflow occurs.

13.1 Timer/Counters 0 & 1

The N79E825 series have two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 for Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/8 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

13.1.1 Time-Base Selection

The N79E825 series can operate like the standard 8051/52 family, counting at the rate of 1/12 of the clock speed, or in turbo mode, counting at the rate of 1/4 clock speed. The speed is controlled by the T0M and T1M bits in CKCON, and the default value is zero, which uses the standard 8051/52 speed.

13.1.2 Mode 0

In Mode 0, the timer/counter is a 13-bit counter. The 13-bit counter consists of THx (8 MSB) and the five lower bits of TLx (5 LSB). The upper three bits of TLx are ignored. The timer/counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. When $C/\overline{T}$ is 0, the timer/counter counts clock cycles; when $C/\overline{T}$ is 1, it counts falling edges on T0 (P1.2 for Timer 0) or T1 (P0.7 for Timer 1). For clock cycles, the time base may be 1/12 or 1/4 clock speed, and the falling edge of the clock increments the counter. When the 13-bit value moves from 1FFFh to 0000h, the timer overflow flag TFx is set, and an interrupt occurs if enabled. This is illustrated in next figure below.

In "Timer" mode, if output toggle enable bit of P2M1.T0OE or P2M1.T1OE is enabled, T0 or T1 output pin will toggle whenever a timer overflow occurs.

15.2 CLOCK CONTROL of Watchdog

WD1, WD0: WDCON.5, WDCON.4 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the watchdog timer. The reset time is 512 clocks longer than the interrupt time-out value.

The default Watchdog time-out is 2^{17} clocks, which is the shortest time-out period. The WDRUN, WD0, WD1, EWRST, WDIF and WDCLR bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the Watchdog Timer.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide–by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter.

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

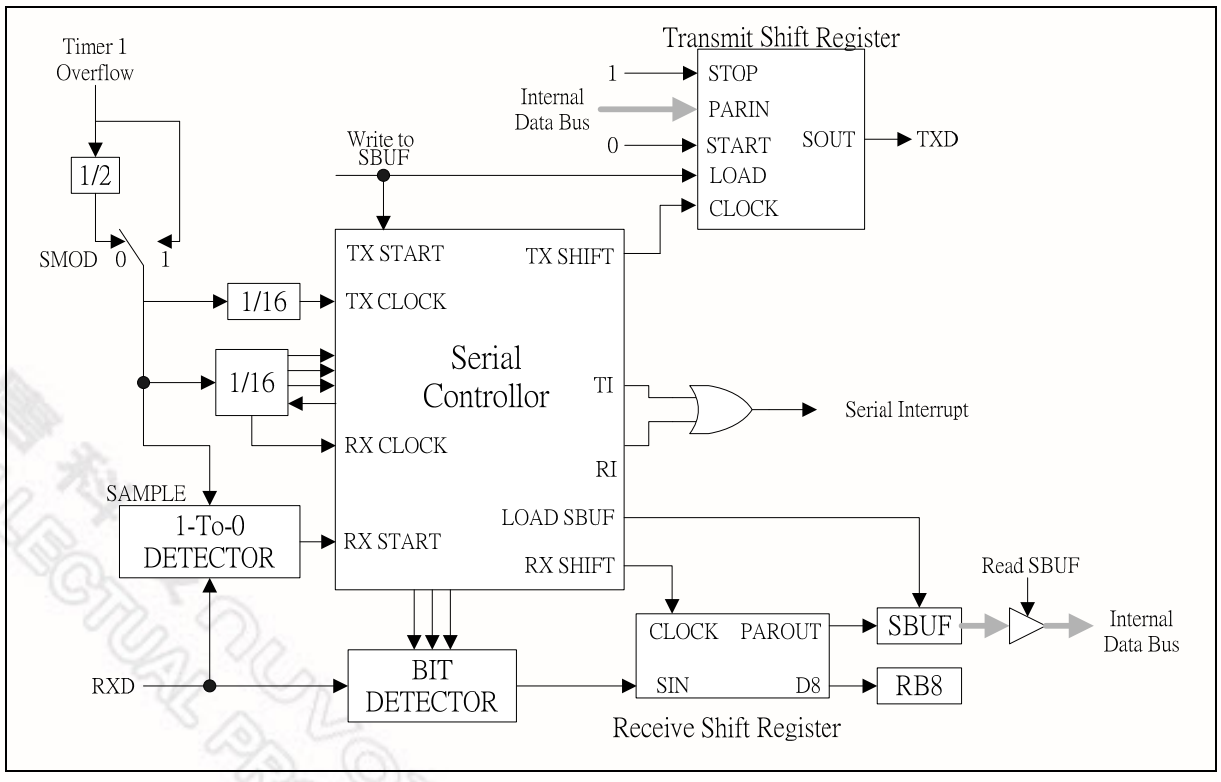

Figure 16-2: Serial Port Mode 1

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and

2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

16.4 MODE 3

This mode is similar to Mode 2 in all aspects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

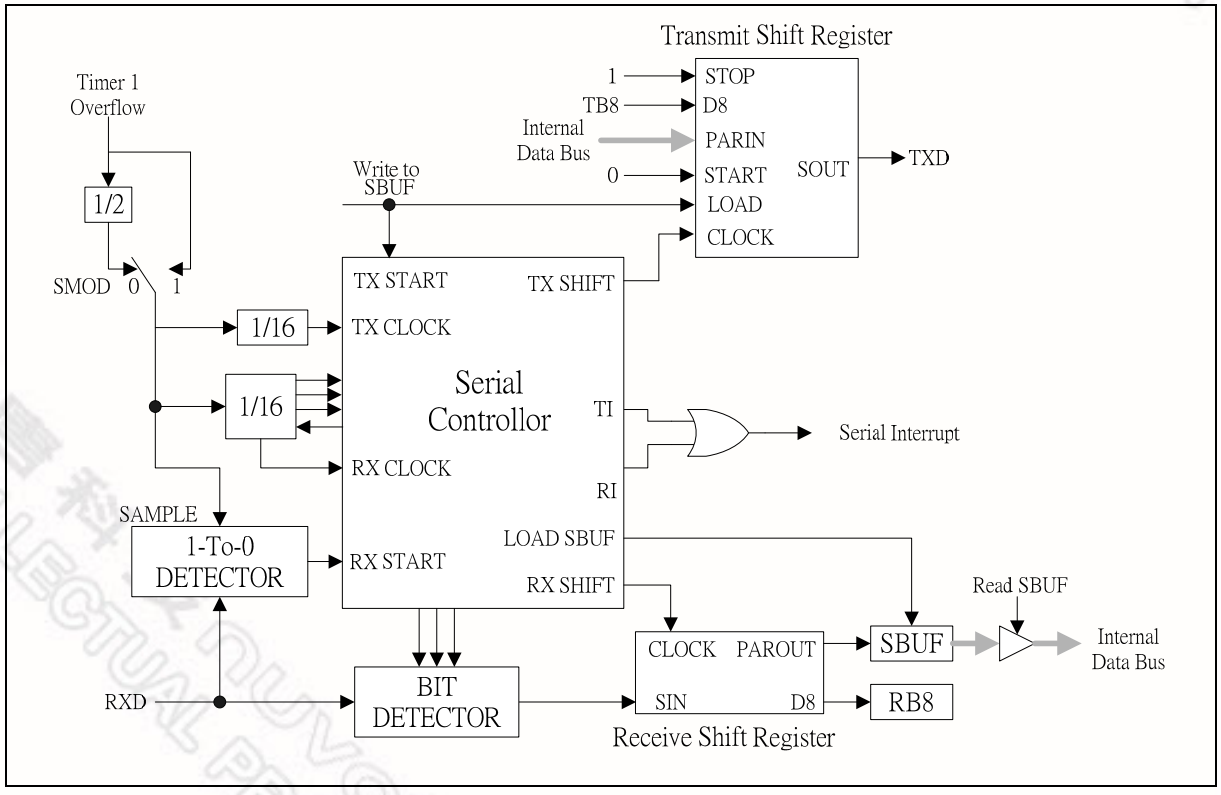

Figure 16-4: Serial Port Mode 3

20 I/O PORT CONFIGURATION

The N79E825 series have three I/O ports, port 0, port 1 and port 2. All pins of I/O ports can be configured to one of four types by software except P1.5 is only input pin. When P1.5 is configured reset pin by RPD=0 in the CONFIG 1 register, the N79E825 series can support 15 pins by use Crystal. If used on-chip RC oscillator the P1.5 is configured input pin, the N79E825 series can be supported up to 18 pins. The I/O ports configuration setting as below table.

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P2M1.PxS=0, TTL input P2M1.PxS=1, Schmitt input
1	1	Open Drain

Table 20-1: I/O port Configuration Table

All port pins can be determined to high or low after reset by configure PRHI bit in the CONFIG1 register. After reset, these pins are in quasi-bidirectional mode. The port pin of P1.5 only is a Schmitt trigger input.

Enabled toggle outputs from Timer 0 and Timer 1 by T0OE and T1OE on P2M1 register, the output frequency of Timer 0 or Timer 1 is by Timer overflow.

Each I/O port of the N79E825 series may be selected to use TTL level inputs or Schmitt inputs by P(n)S bit on P2M1 register, where n is 0, 1 or 2. When P(n)S is set to 1, Ports are selected Schmitt trigger inputs on Port(n). The P2.0 (XTAL2) can be configured clock output when used on-chip RC or external Oscillator is clock source, and the frequency of clock output is divided by 4 on on-chip RC clock or external Oscillator.

20.1 Quasi-Bidirectional Output Configuration

After chip was power on or reset, the all ports output are this mode, and output is common with the 8051. This mode can be used as both an input and output without the need to reconfigure the port.

When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

This mode has three pull-up resisters that are “strong” pull-up, “weak” pull-up and “very weak” pull-up. The “strong” pull-up is used fast transition from logic “0” change to logic “1”, and it is fast latch and transition. When port pins is occur from logic “0” to logic “1”, the strong pull-up will quickly turn on two CPU clocks to pull high then turn off.

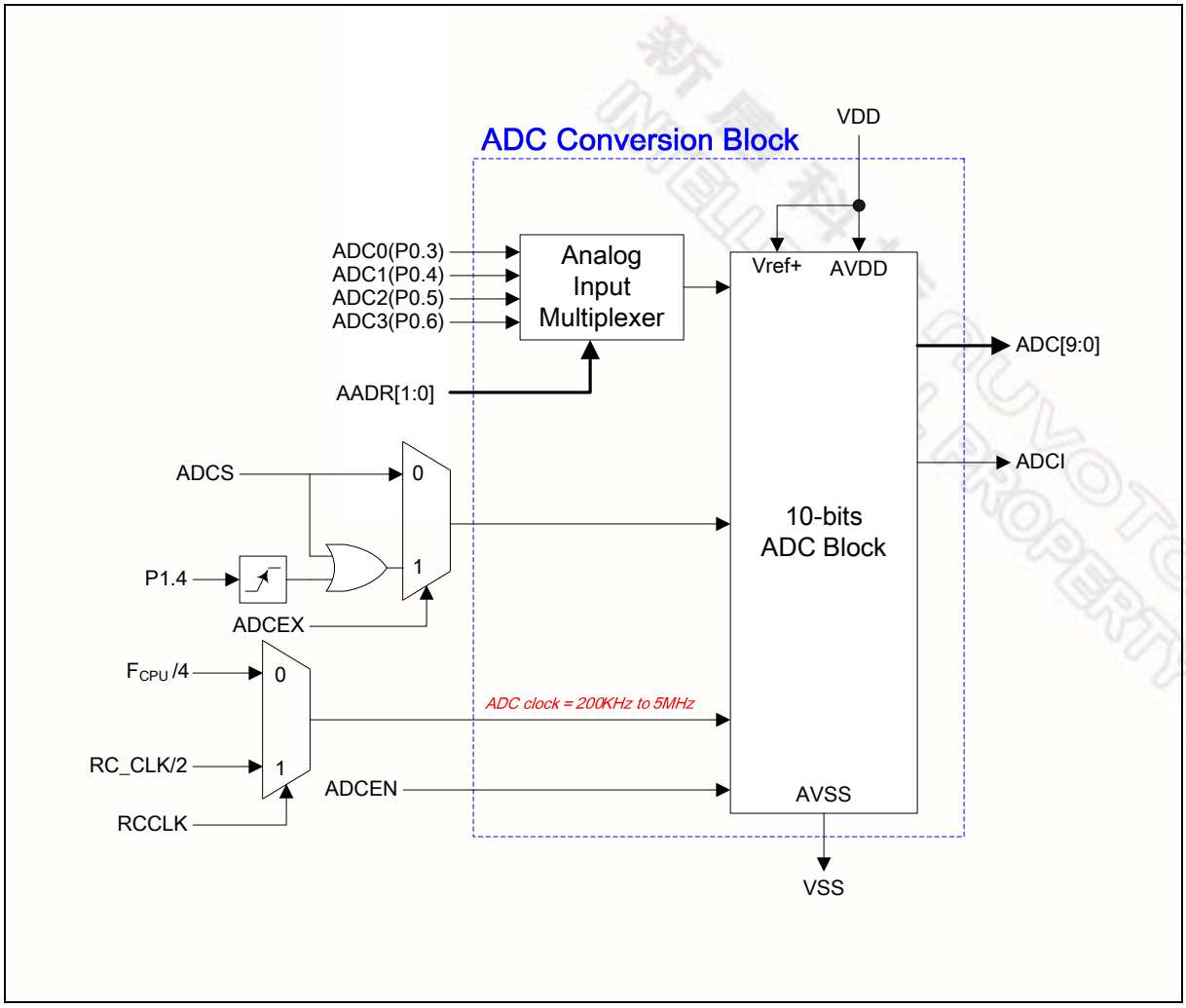

Figure 24-2: The ADC Block Diagram

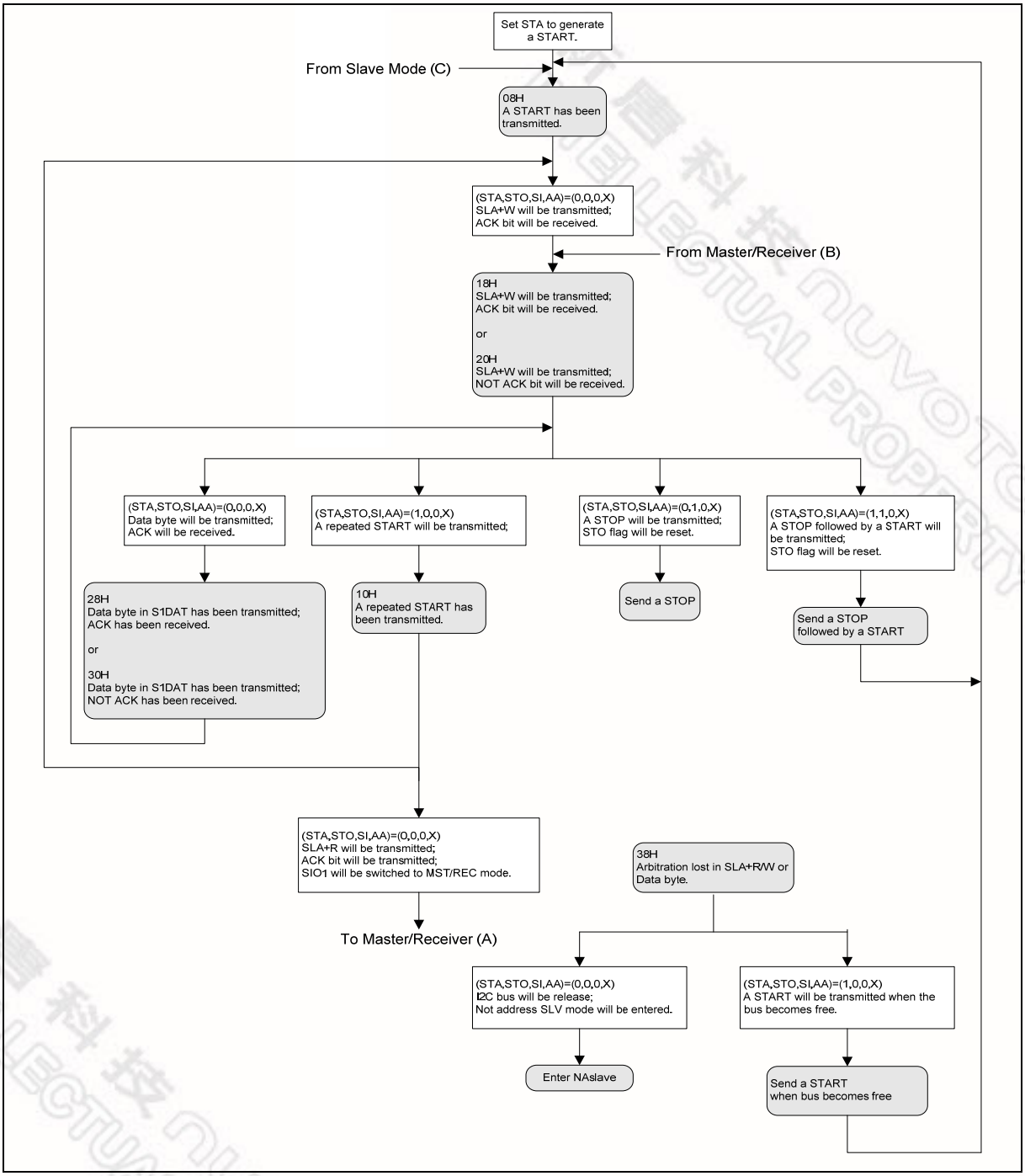

Figure 25-4: Master Transmitter Mode

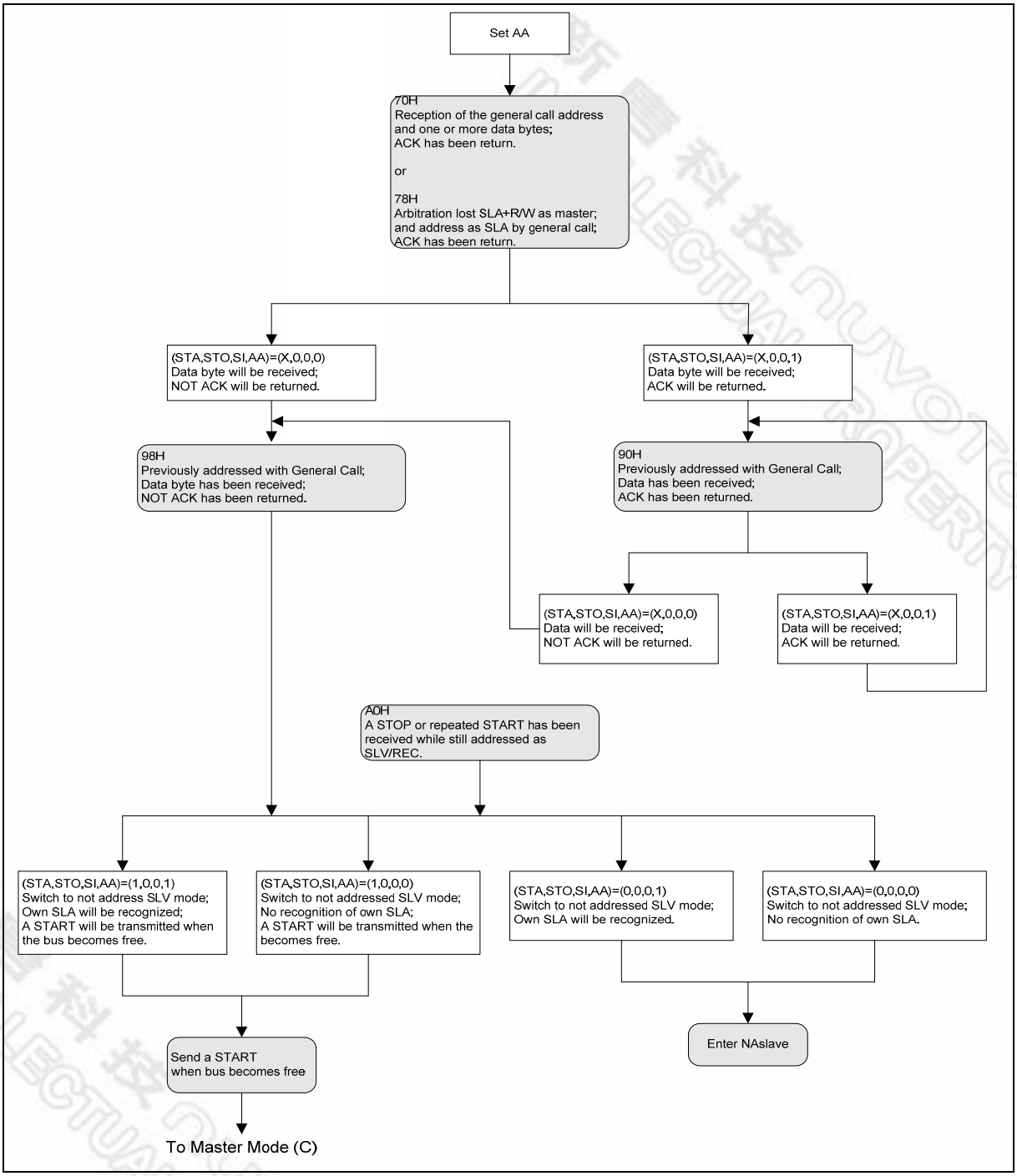

Figure 25-8:GC Mode

BIT 7	BIT 6	FUNCTION DESCRIPTION
1	1	Both security of **16KB/8KB/4KB/2KB** program code and **256** Bytes data area are unlocked. They can be erased, programmed or read by Writer or ICP.
0	1	The **16KB/8KB/4KB/2KB** program code area is locked. It can't be read by Writer or ICP.
1	0	Don't support (Invalid).
0	0	Both security of **16KB/8KB/4KB/2KB** program code and **256** Bytes data area are locked. They can't be read by Writer or ICP.