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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini51fde

1 GENERAL DESCRIPTION

The NuMicro Mini51™ series 32-bit microcontroller is embedded with ARM® Cortex™-M0 core for industrial control and applications which require high performance, high integration, and low cost. The Cortex™-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NuMicro Mini51™ series can run up to 24 MHz and operate at 2.5V ~ 5.5V, -40℃ ~ 105℃, and thus can afford to support a variety of industrial control and applications which need high CPU performance. The NuMicro Mini51™ series offers 4K/8K/16K-bytes embedded program flash, size configurable data flash (shared with program flash), 2K-byte flash for the ISP, and 2K-byte SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NuMicro Mini51™ series in order to reduce component count, board space and system cost. These useful functions make the NuMicro Mini51™ series powerful for a wide range of applications.

Additionally, the NuMicro Mini51™ series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core running up to 24 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Built-in LDO for wide operating voltage ranged: 2.5 V to 5.5 V
- Memory
  - 4 KB/ 8 KB/ 16 KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2 KB Flash for loader (LDROM)
  - 2 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - 4 ~ 24 MHz external crystal input (HXT)
  - 32.768 kHz external crystal input (LXT) for Power-down wake-up and system operation clock
  - 22.1184 MHz internal oscillator (HIRC) (1% accuracy at 25°C, 5V)
    - Dynamically calibrating the HIRC OSC to 22.1184 MHz ±1% from -40°C to 105°C by external 32.768K crystal oscillator (LXT)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and Power-down wake-up
- I/O Port
  - Up to 30 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - Input-only with high impendence
    - Push-pull output
    - Open-drain output
    - Quasi-bidirectional
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - Configurable default I/O mode of all pins after POR
- Timer

- Provides two channel 32-bit timers. One 8-bit pre-scale counter with 24-bit up counter for each timer
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous operation modes
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
- Provides event counter function
- Supports wake-up from Idle or Power-down mode

- WDT (Watchdog Timer)
  - Multiple clock sources
  - Supports wake-up from Idle or Power-down mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Independent 16-bit PWM duty control units with maximum six outputs
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake protections
  - Supports duty, period, and fault break interrupts
  - Supports duty/period trigger ADC conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period
  - Provides interrupt accumulation function
- UART (Universal Asynchronous Receiver/Transmitters)
  - One UART device
  - Buffered receiver and transmitter, each with 16-byte FIFO
  - Optional flow control function (CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports RS-485 function
- SPI (Serial Peripheral Interface)
  - One SPI devices
  - Supports Master/Slave mode

- Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage level: 2.0V
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP (7x7), 33-pin QFN (5x5) , 33-pin QFN (4x4), 20-pin TSSOP

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro Mini51™ Series Selection Code

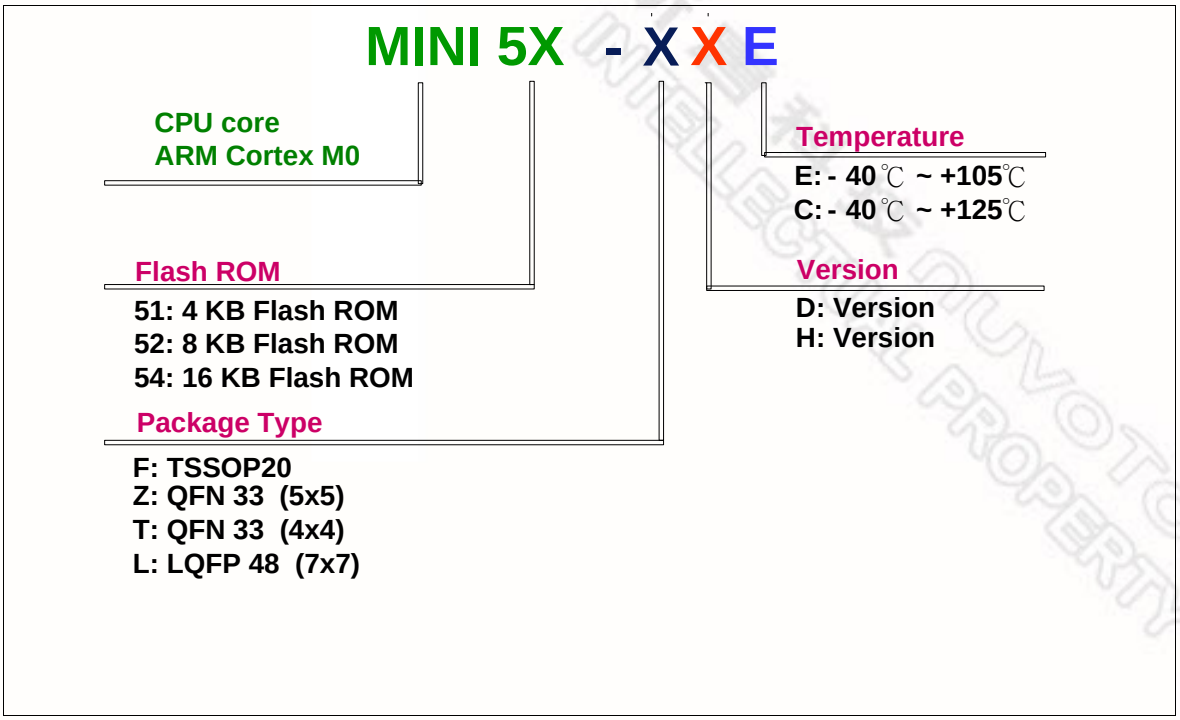


Figure 4.1-1 NuMicro Mini51™ Series Selection Code

4.3.2 QFN 33-pin

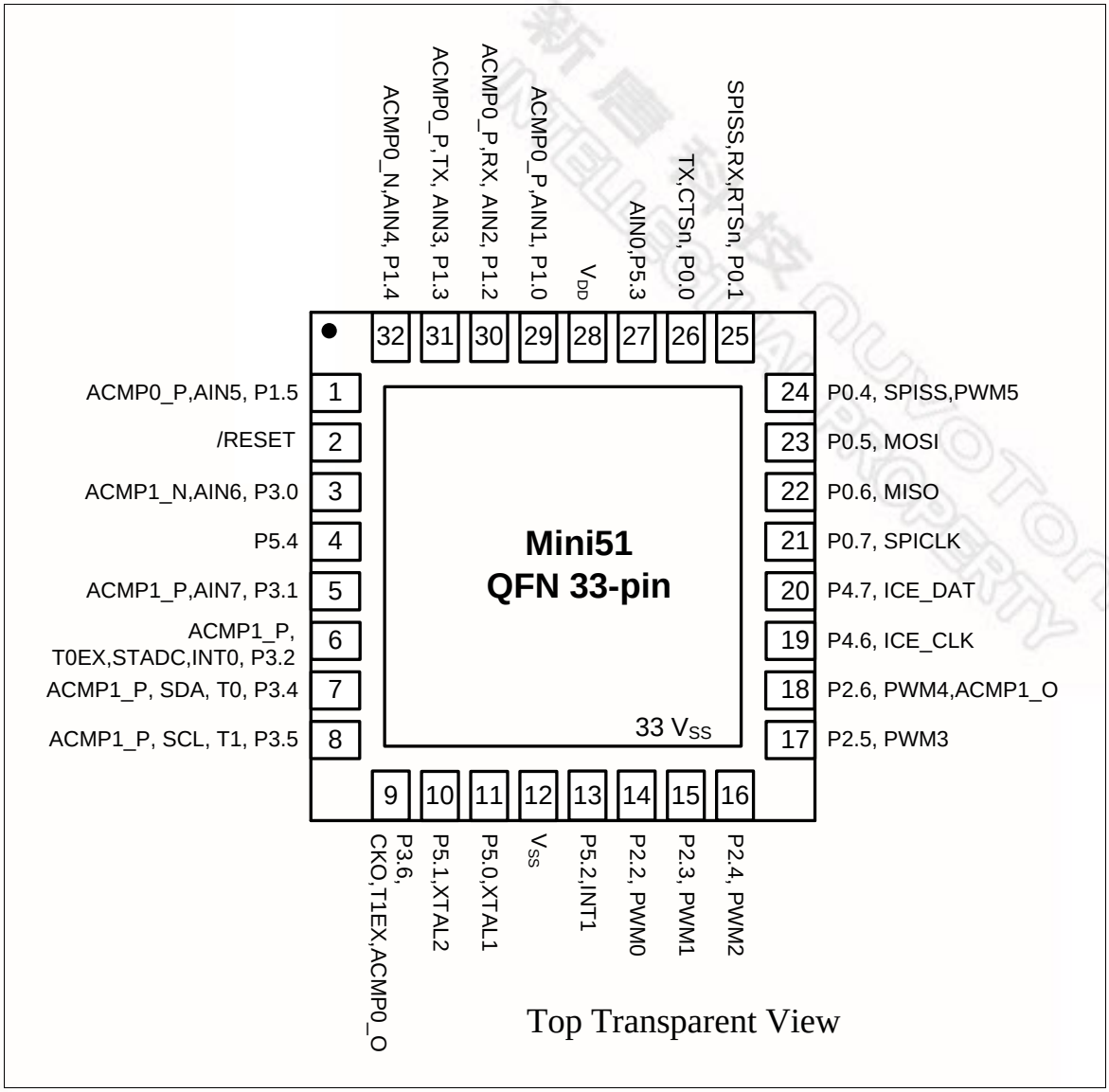


Figure 4.3-2 NuMicro Mini51™ Series QFN 33-pin Diagram

4.4 Pin Description

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
1	---	---	---	NC	**---**	Not connected
2	1	4	---	P1.5	**I/O**	General purpose digital I/O pin
				AIN5	**AI**	ADC analog input pin
				ACMP0_P	**AI**	Analog comparator positive input pin
3	2	5	5	/RESET	**I(ST)**	The Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. /RESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
4	3	---	---	P3.0	**I/O**	General purpose digital I/O pin
				AIN6	**AI**	ADC analog input pin
				ACMP1_N	**AI**	Analog comparator negative input pin
5	---	---	---	AV_{SS}	**AP**	Ground pin for analog circuit
6	4	---	---	P5.4	**I/O**	General purpose digital I/O pin
7	5	---	---	P3.1	**I/O**	General purpose digital I/O pin
				AIN7	**AI**	ADC analog input pin
				ACMP1_P	**AI**	Analog comparator positive input pin
8	6	6	6	P3.2	**I/O**	General purpose digital I/O pin
				INT0	**I**	External interrupt 0 input pin
				STADC	**I**	ADC external trigger input pin
				T0EX	**I**	Timer 0 external capture/reset trigger input pin
				ACMP1_P	**AI**	Analog comparator positive input pin
9	7	7	7	P3.4	**I/O**	General purpose digital I/O pin
				T0	**I/O**	Timer 0 external event counter input pin
				SDA	**I/O**	I^2C data I/O pin
				ACMP1_P	**AI**	Analog comparator positive input pin
10	8	8	8	P3.5	**I/O**	General purpose digital I/O pin
				T1	**I/O**	Timer 1 external event counter input pin
				SCL	**I/O**	I^2C clock I/O pin
				ACMP1_P	**AI**	Analog comparator positive input pin
11	---	---	---	NC	**---**	Not connected.
12	---	---	---	NC	**---**	Not connected.
13	---	--	--	NC	**---**	Not connected.

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
				RX	**I**	UART data receiver input pin.
				ACMP0_P	**AI**	Analog comparator positive input pin.
46	31	2	3	P1.3	**I/O**	General purpose digital I/O pin.
				AIN3	**AI**	ADC analog input pin.
				TX	**O**	UART transmitter output pin.
				ACMP0_P	**AI**	Analog comparator positive input pin.
47	32	3	4	P1.4	**I/O**	General purpose digital I/O pin.
				AIN4	**I/O**	PWM5: PWM output/Capture input.
				ACMP0_N	**AI**	Analog comparator negative input pin.
48	---	--	--	NC	**---**	Not connected.

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

6.4 Clock Controller

6.4.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex™-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 3 sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT) or 32.768 kHz (LXT) external low speed crystal oscillator
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

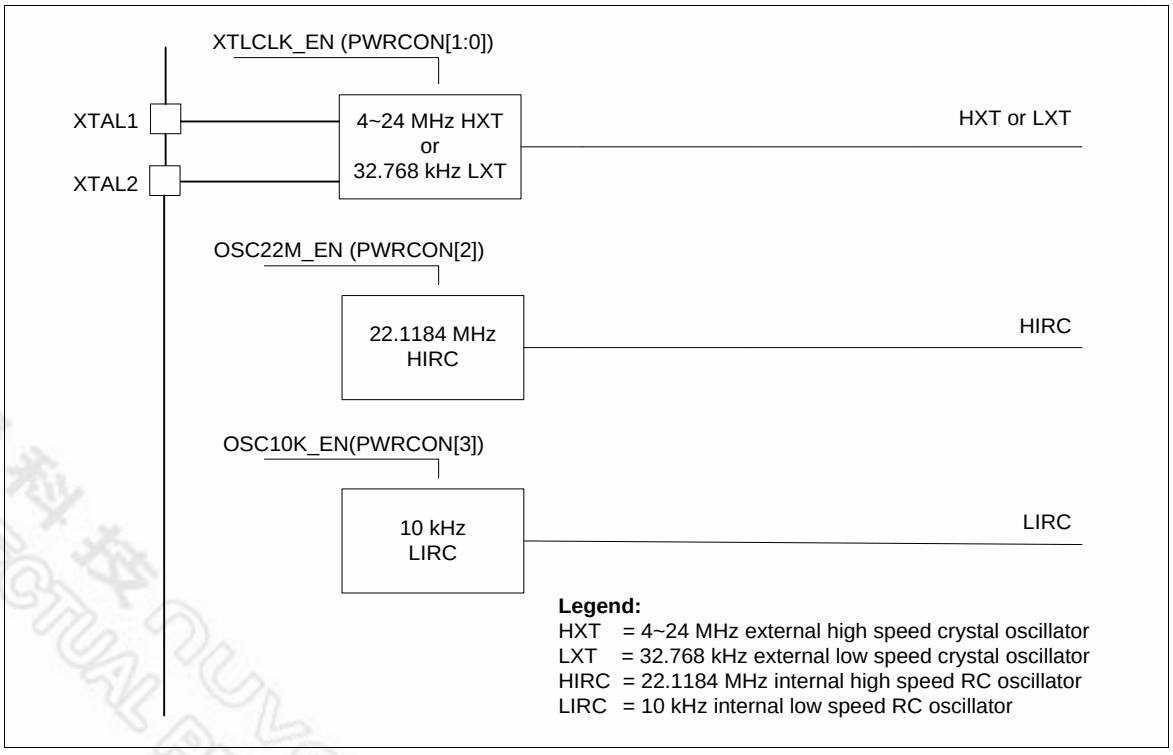


Figure 6.4-1 Clock Generator Block Diagram

6.4.2 System Clock and SysTick Clock

The system clock has three clock sources which are generated from clock generator block. The clock source switches depending on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown below.

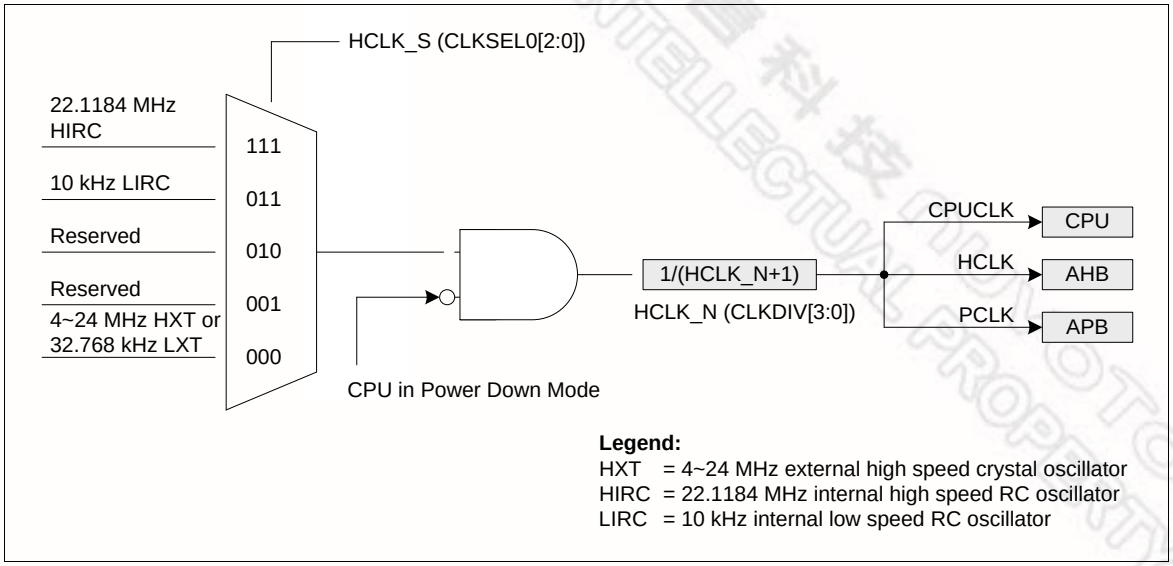


Figure 6.4-2 System Clock Block Diagram

The clock source of SysTick in Cortex™-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switches depending on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown below.

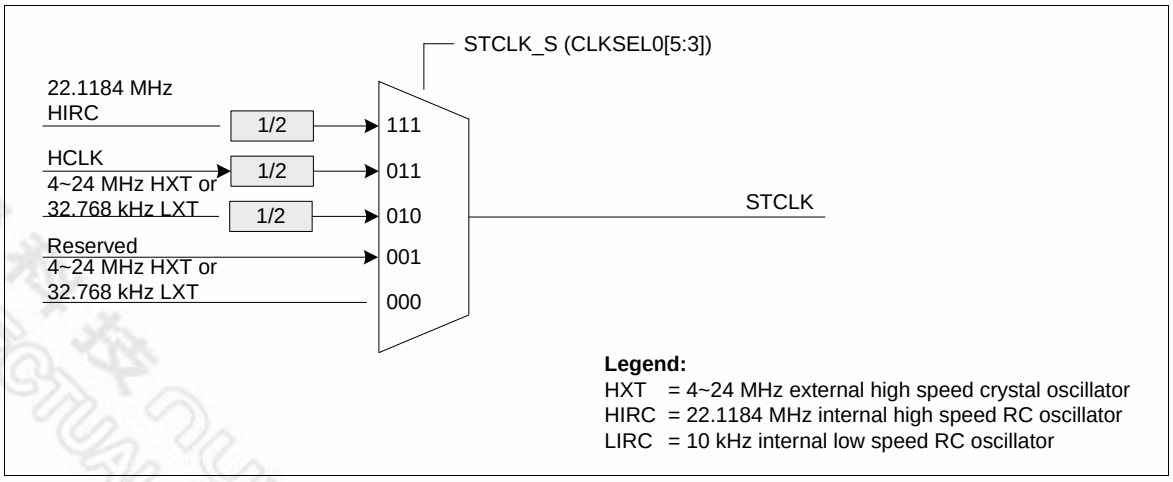


Figure 6.4-3 SysTick Clock Control Block Diagram

6.4.3 ISP Clock Source Selection

The clock source of ISP is from AHB clock (HCLK). Please refer to the register AHBCLK.

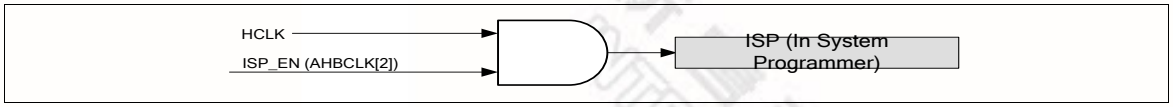


Figure 6.4-4 AHB Clock Source for HCLK

6.4.4 Module Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals. Please refer to the CLKSEL1 and APBCLK register description in section **Error! Reference source not found.**.

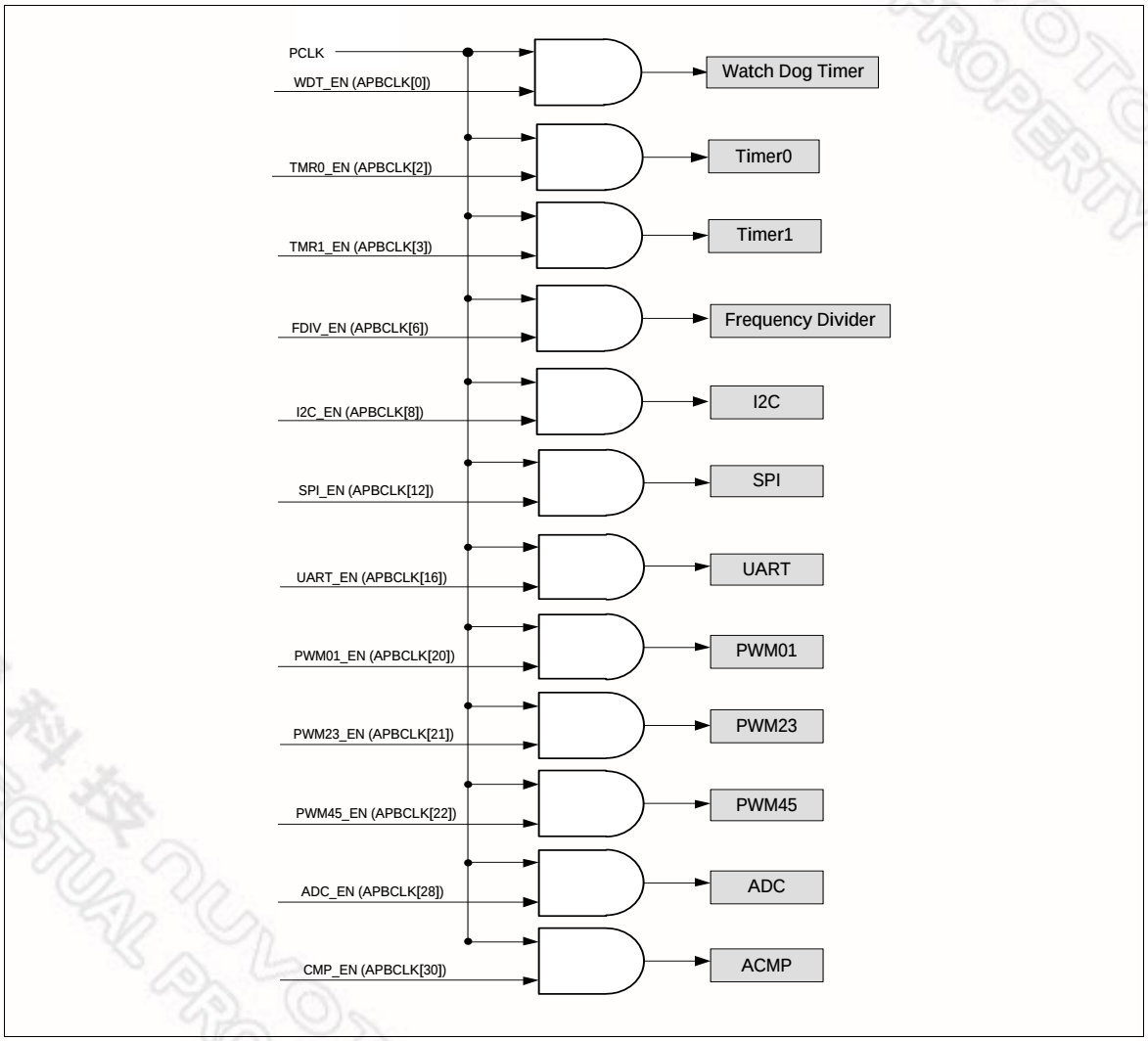


Figure 6.4-5 Peripherals Clock Source Selection for PCLK

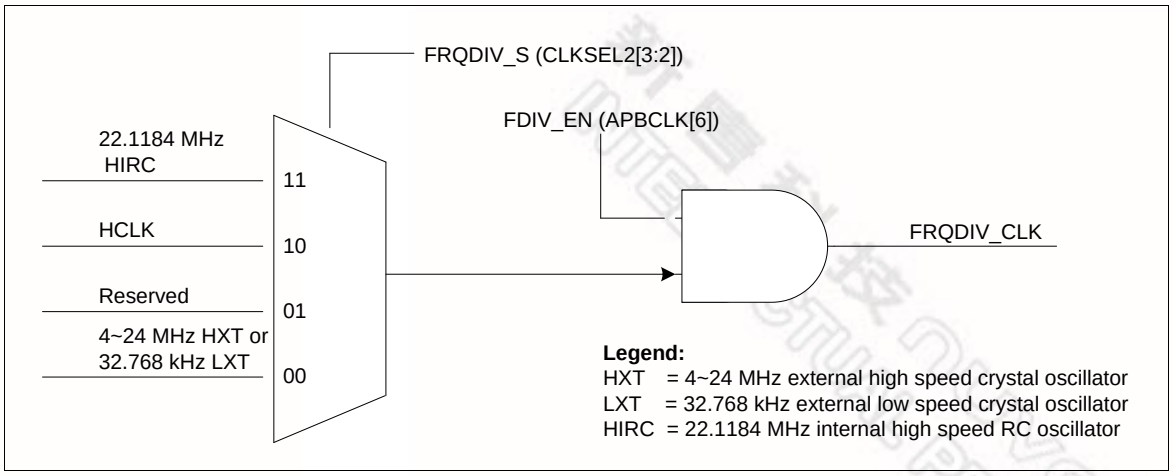


Figure 6.4-6 Clock Source of Frequency Divider

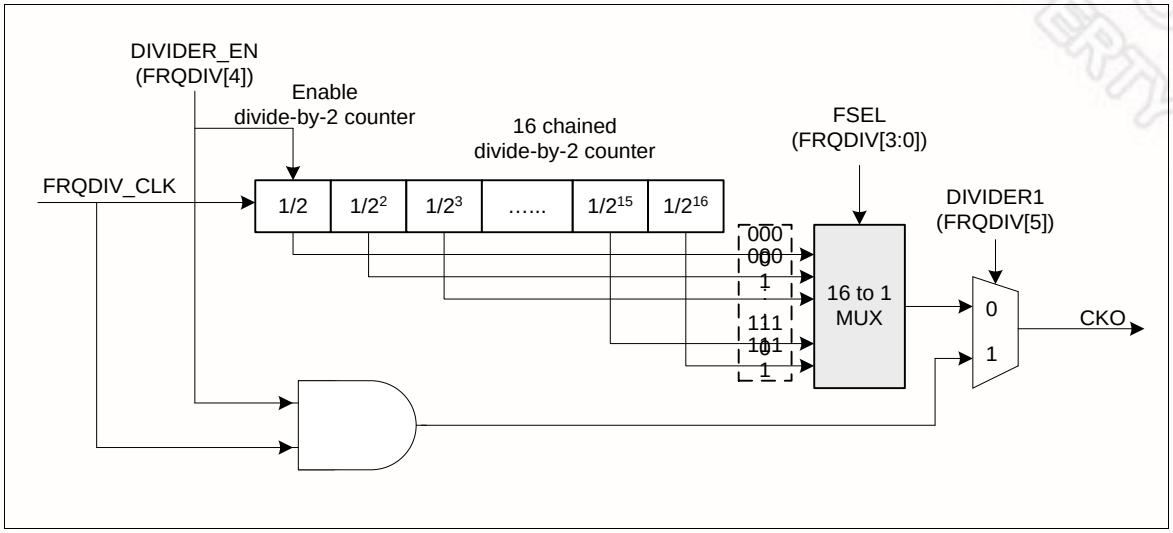


Figure 6.4-7 Block Diagram of Frequency Divider

6.7 Flash Memory Controller (FMC)

6.7.1 Overview

The NuMicro Mini51™ series is equipped with 4K/8K/16K bytes on chip embedded flash memory for application program (APROM) that can be updated through ISP procedure. In-System-Programming (ISP) and In-Application-Programming (IAP) enable user to update program memory when chip is soldered on PCB. After chip power on Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro Mini51™ series also provides Data Flash region that is shared with APROM and its start address is configurable and defined by user in CONFIG1.

6.7.2 Features

- Running up to 24 MHz with zero wait state for discontinuous address read access
- 4/8/16 Kbytes application program memory (APROM)
- 2 Kbytes in system programming (ISP) loader program memory (LDROM)
- Programmable data flash start address
- All embedded flash memory supports 512 bytes page erase
- In System Program (ISP)/In Application Program (IAP) to update on chip flash memory

6.12 Timer Controller (TMR)

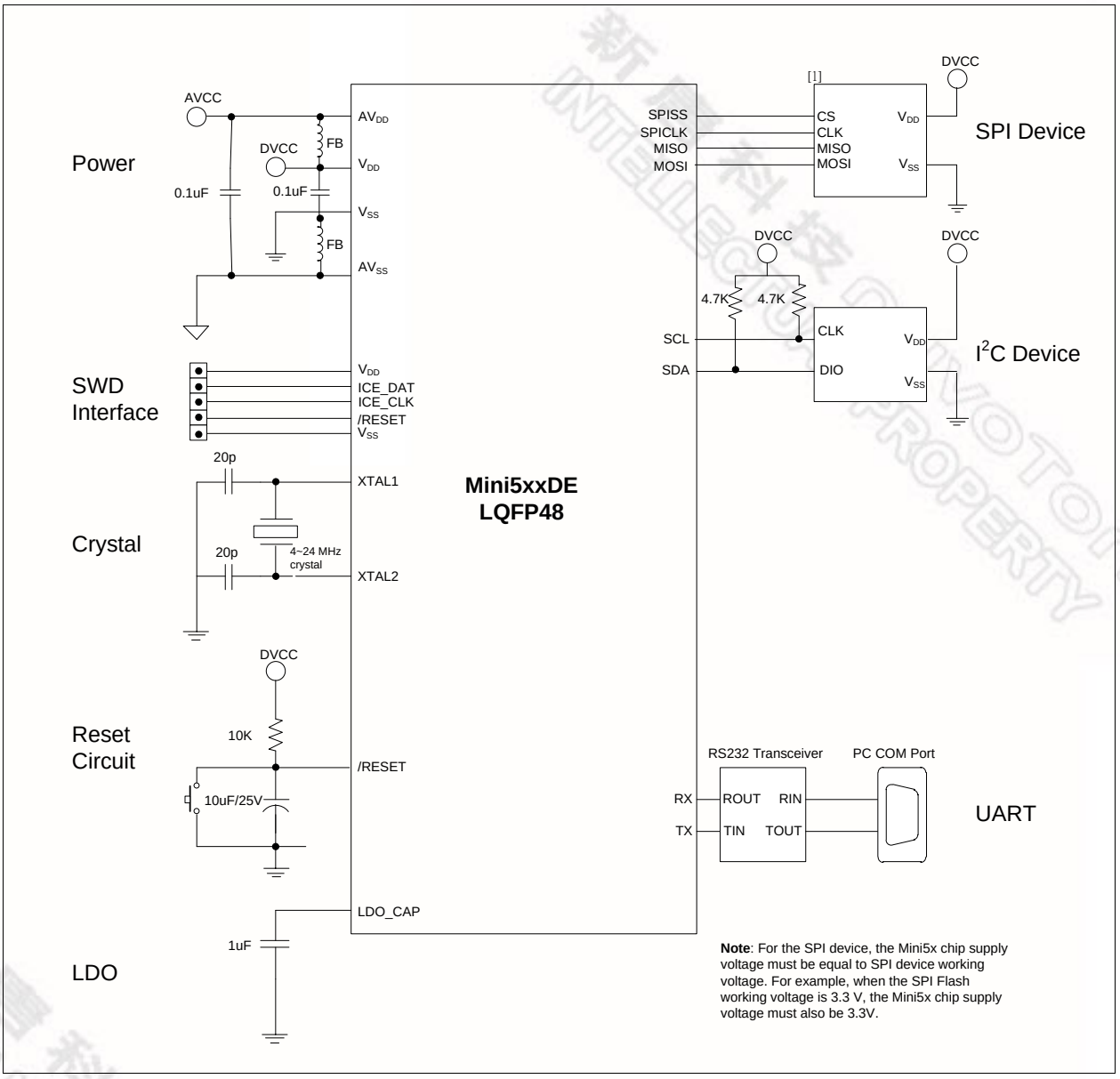
6.12.1 Overview

The Timer Controller includes two 32-bit timers, TIMER0 ~ TIMER1, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.12.2 Features

- Two sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each channel (TMR0_CLK, TMR1_CLK)
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}); T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external pin (T0, T1)
- 24-bit capture value is readable through TCAP (Timer Capture Data Register)
- Supports external capture pin (T0EX, T1EX) for interval measurement
- Supports internal signal (CPO0, CPO1) for interval measurement
- Supports external capture pin (T0EX, T1EX) to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

8 APPLICATION CIRCUIT



I_{IDLE2}	Operating Current Idle Mode HCLK=22.1184 MHz	-	4.9	-	mA	V_{DD} 5.5V; HXT 24 MHz; HIRC Disabled; All digital modules Disabled
I_{IDLE3}		-	5.1	-	mA	V_{DD} 3.3V; HXT 24 MHz; HIRC Disable; All digital modules Enabled
I_{IDLE4}		-	2.9	-	mA	V_{DD} 5.5V; HXT 24 MHz; HIRC Disabled; All digital modules Disabled
I_{IDLE5}		-	4.1	-	mA	V_{DD} 5.5V; HXT Disabled; HIRC Enabled; All digital modules Enabled
I_{IDLE6}		-	2.0	-	mA	. V_{DD} 5.5V; HXT Disabled; HIRC Enabled; All digital modules Disabled
I_{IDLE7}		-	4.1	-	mA	V_{DD} 3.3V; HXT Disabled; HIRC Enabled; All digital modules Enabled
I_{IDLE8}		-	1.9	-	mA	V_{DD} 3.3V; HXT Disabled; HIRC Enabled; All digital modules Disabled

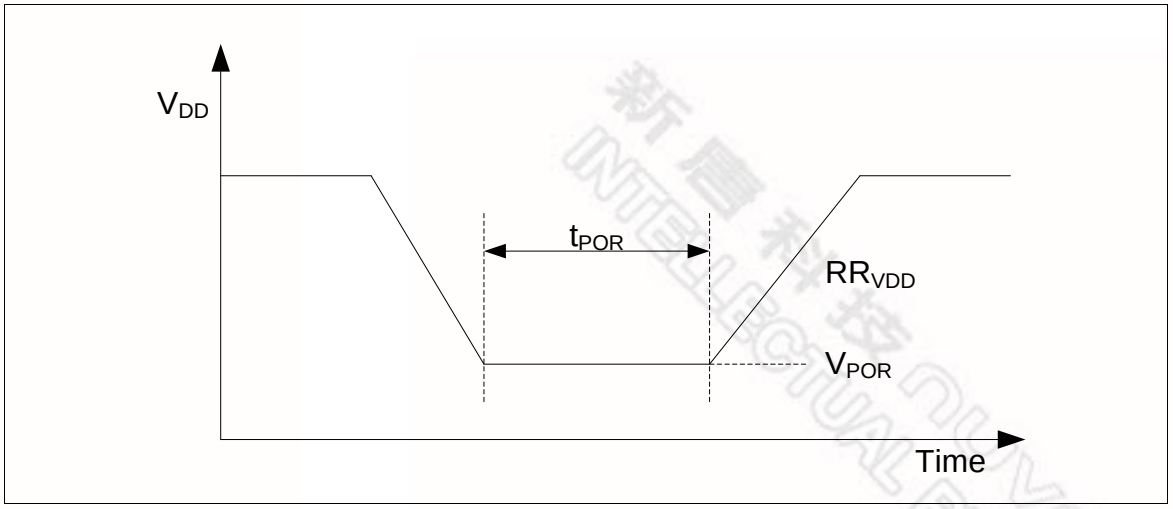
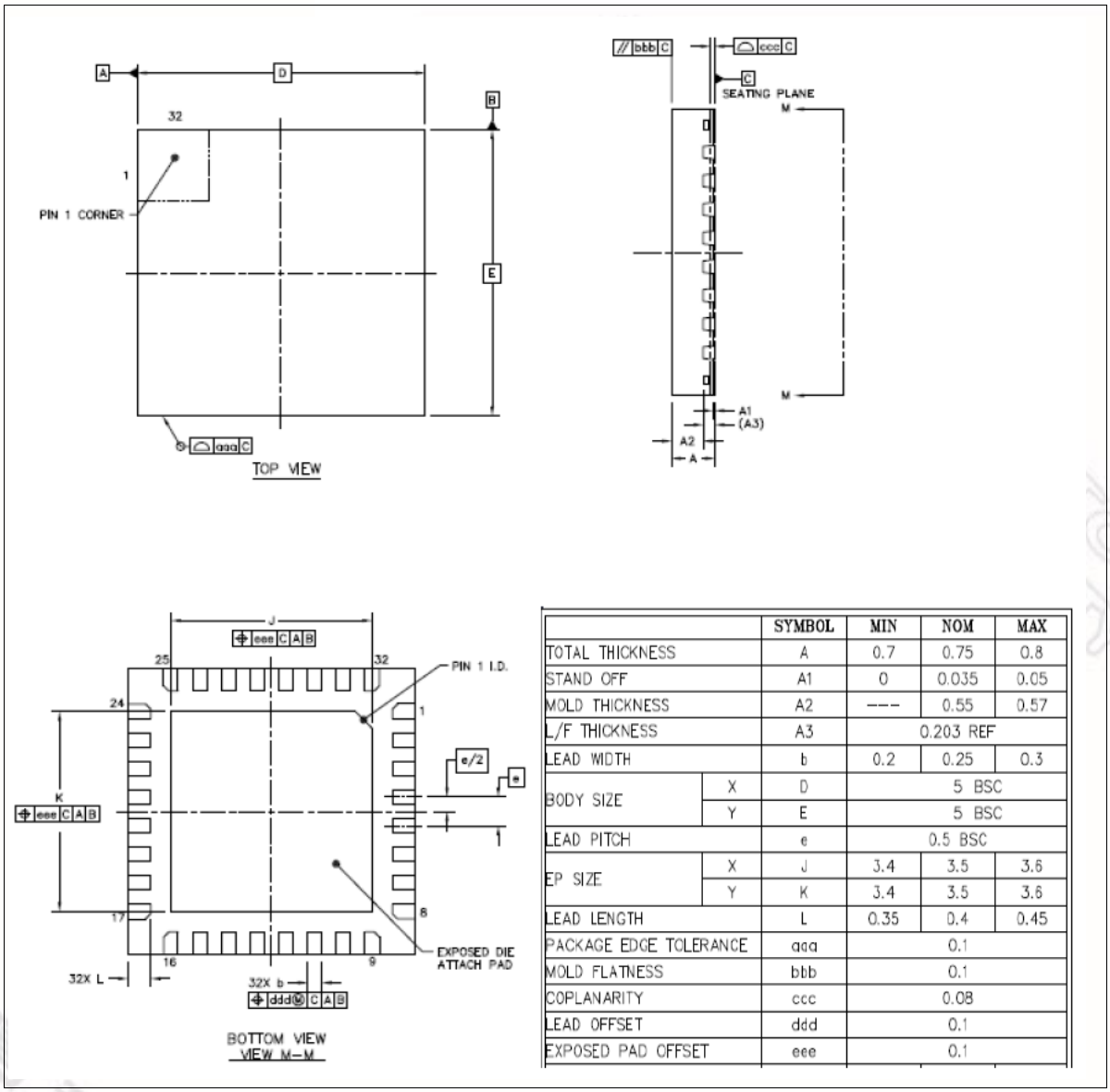


Figure 9-2Power-up Ramp Condition

9.4.6 Comparator

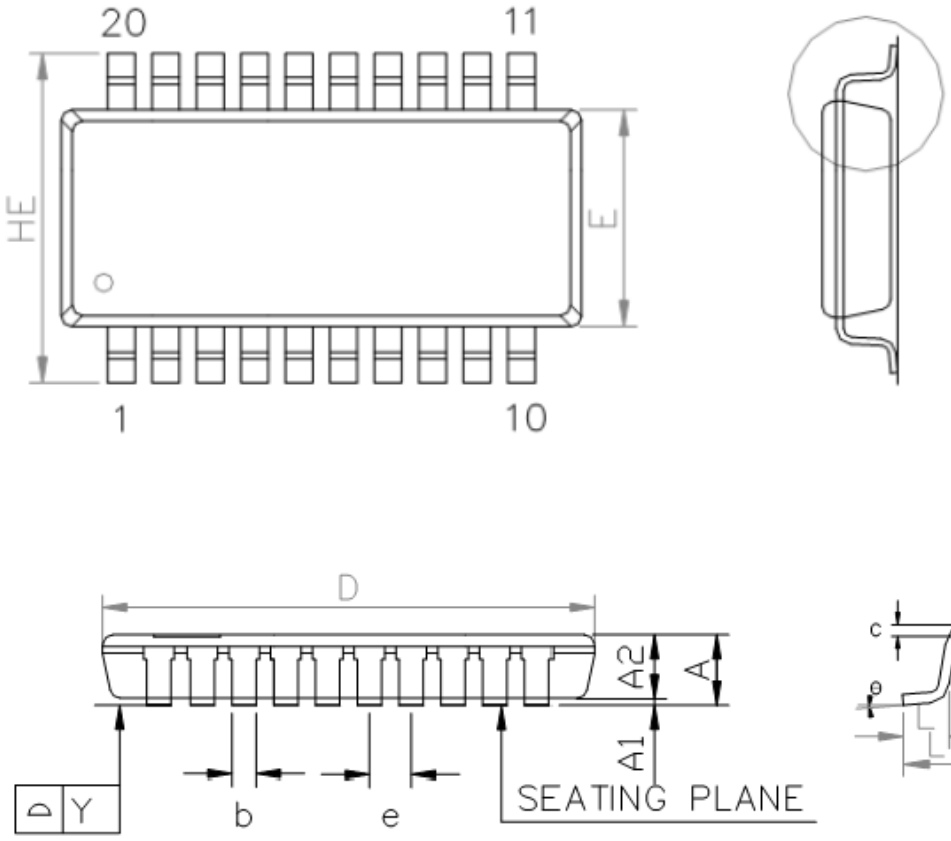
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.5	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	40	80	μA	AV_{DD}=5V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	AV_{DD} -0.1	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD}– 0.1	V	-
-	DC Gain	40	70	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{COM}=1.2 V, V_{DIFF}=0.1 V
V_{HYS}	Hysteresis	-	±30	±60	mV	V_{COM}=1.2 V
T_{STB}	Stable time	-	-	1	μs	

10.3 33-pin QFN (5 mm x 5 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

10.4 20-pin TSSOP



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	—	0.30	0.007	—	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	—	0.20	0.004	—	0.008
θ	0°	—	8°	0°	—	8°
Y	0.10 BASIC			0.004 BASIC		

11 REVISION HISTORY

Revision	Date	Description
1.00	Oct. 18, 2013	Preliminary version
1.01	May 20, 2014	Supported the Mini54FHC for NuMicro Mini51 series.