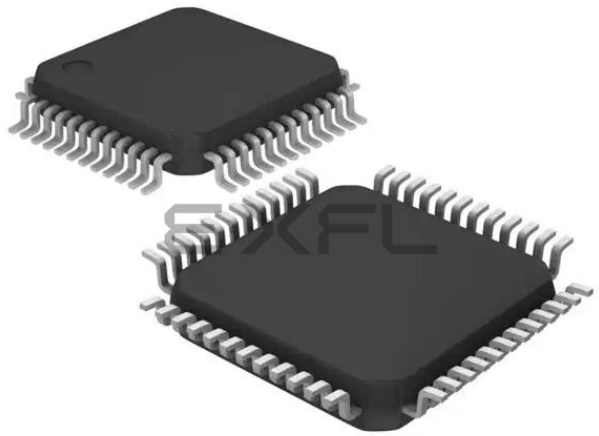

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini51lde

Table of Contents

1 GENERAL DESCRIPTION 7
2 FEATURES 8
3 ABBREVIATIONS 12
4 PARTS INFORMATION LIST AND PIN CONFIGURATION 13
4.1 NuMicro Mini51™ Series Selection Code 13
4.2 NuMicro Mini51™ Series Product Selection Guide 14
4.3 PIN CONFIGURATION 15
4.3.1 LQFP 48-pin 15
4.3.2 QFN 33-pin 16
4.3.3 TSSOP 20-pin 17
4.3.4 Mini54FHC (TSSOP20-pin) 17
4.4 Pin Description 18
5 BLOCK DIAGRAM 22
5.1 NuMicro Mini51™ Block Diagram 22
6 Functional Description 23
6.1 Memory Organization 23
6.1.1 Overview 23
6.1.2 System Memory Map 23
6.2 Nested Vectored Interrupt Controller (NVIC) 24
6.2.1 Overview 24
6.2.2 Features 24
6.2.3 Exception Model and System Interrupt Map 25
6.2.4 Vector Table 26
6.2.5 Operation Description 27
6.3 System Manager 28
6.3.1 Overview 28
6.3.2 System Reset 28
6.3.3 System Power Architecture 28
6.3.4 Whole System Memory Mapping 30
6.4 Clock Controller 31
6.4.1 Overview 31
6.4.2 System Clock and SysTick Clock 32
6.4.3 ISP Clock Source Selection 33

- Provides two channel 32-bit timers. One 8-bit pre-scale counter with 24-bit up counter for each timer
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous operation modes
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
- Provides event counter function
- Supports wake-up from Idle or Power-down mode

- WDT (Watchdog Timer)
  - Multiple clock sources
  - Supports wake-up from Idle or Power-down mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Independent 16-bit PWM duty control units with maximum six outputs
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake protections
  - Supports duty, period, and fault break interrupts
  - Supports duty/period trigger ADC conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period
  - Provides interrupt accumulation function
- UART (Universal Asynchronous Receiver/Transmitters)
  - One UART device
  - Buffered receiver and transmitter, each with 16-byte FIFO
  - Optional flow control function (CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports RS-485 function
- SPI (Serial Peripheral Interface)
  - One SPI devices
  - Supports Master/Slave mode

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro Mini51™ Series Selection Code

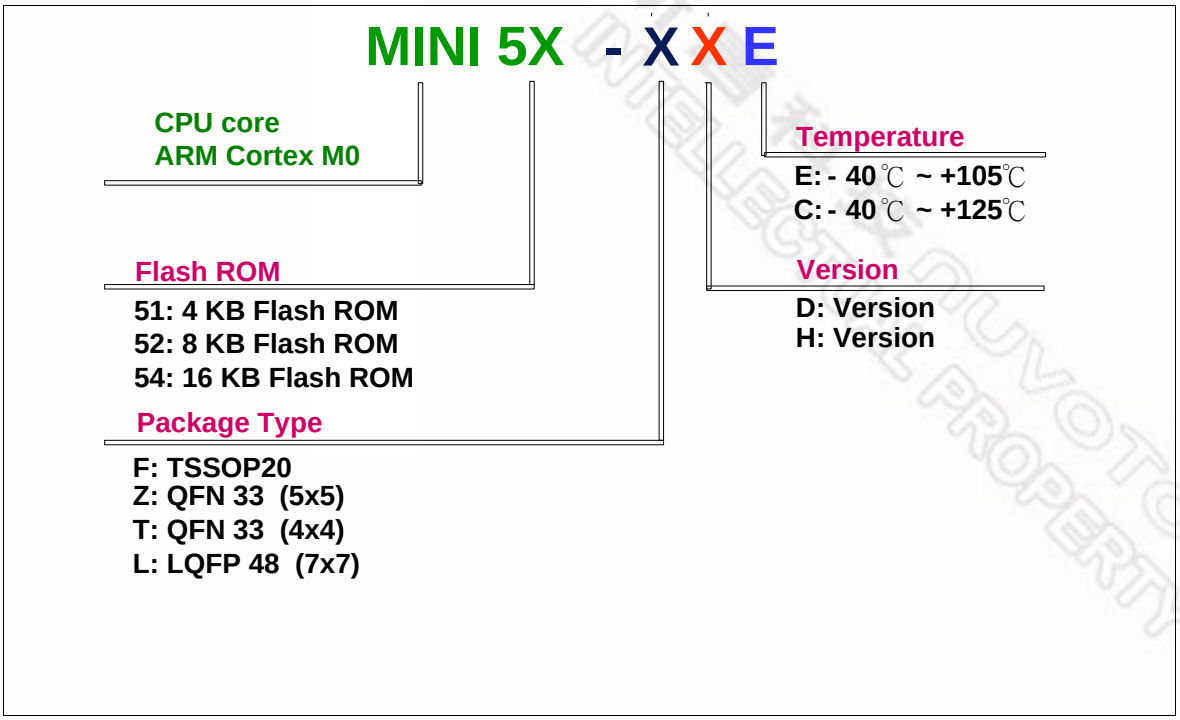


Figure 4.1-1 NuMicro Mini51™ Series Selection Code

4.2 NuMicro Mini51™ Series Product Selection Guide

Part No.	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP IAP	IRC 22.1184 MHz	Package
							UART	SPI	I²C						
MINI51FDE	4 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI51LDE	4 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI51ZDE	4 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI51TDE	4 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
MINI52FDE	8 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI52LDE	8 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI52ZDE	8 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI52TDE	8 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
MINI54FDE	16 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI54LDE	16 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI54ZDE	16 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI54TDE	16 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
*MINI54FHC	16 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	6	3x10-bit	v	v	TSSOP20

Table 4.2-1NuMicro Mini51™ Series Product Selection Guide

* Mini54FHC is a special part number, not pin to pin compatible to others Mini51series part number.

4.3 PIN CONFIGURATION

4.3.1 LQFP 48-pin

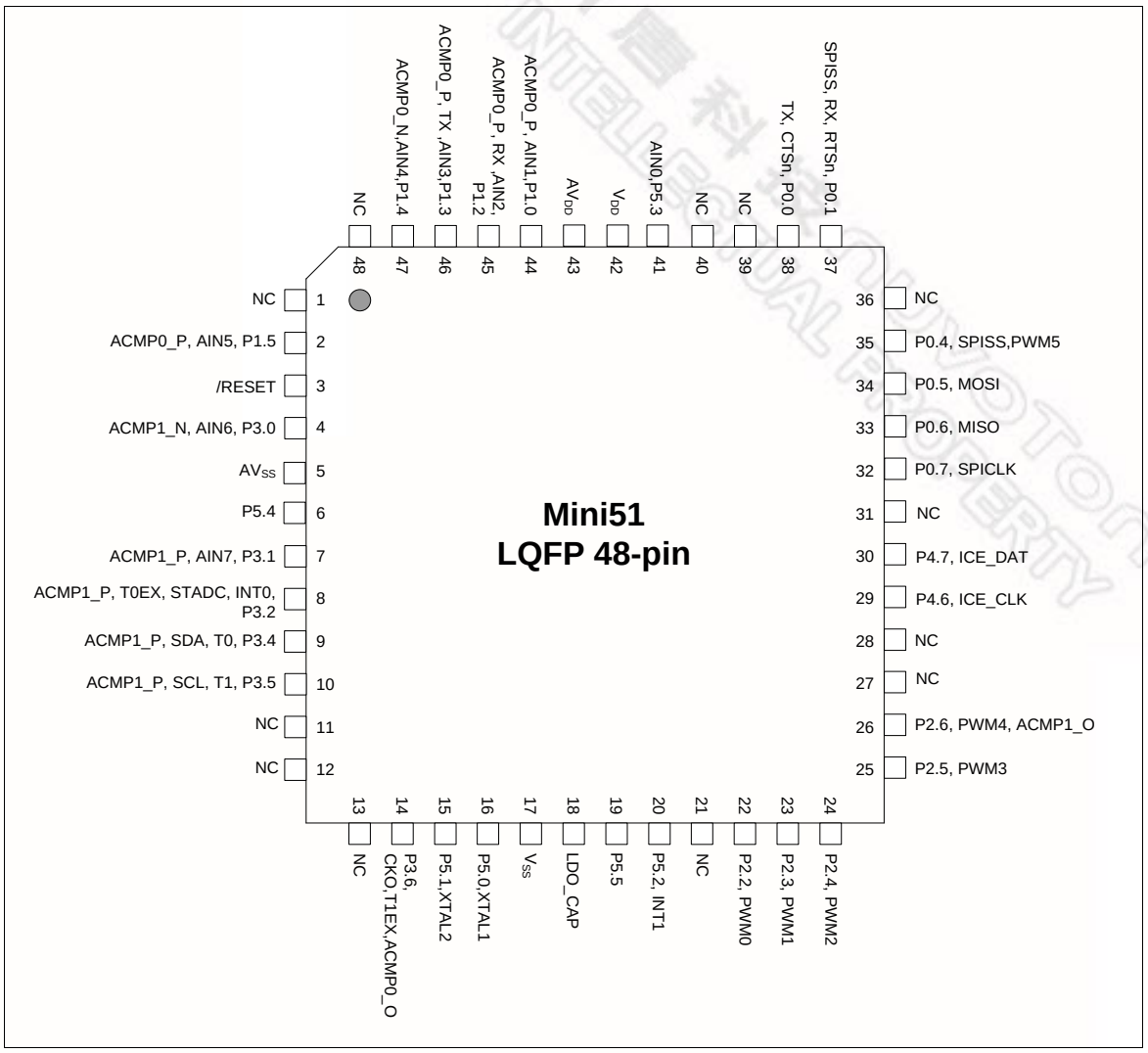


Figure 4.3-1 NuMicro Mini51™ Series LQFP 48-pin Diagram

4.3.3 TSSOP 20-pin

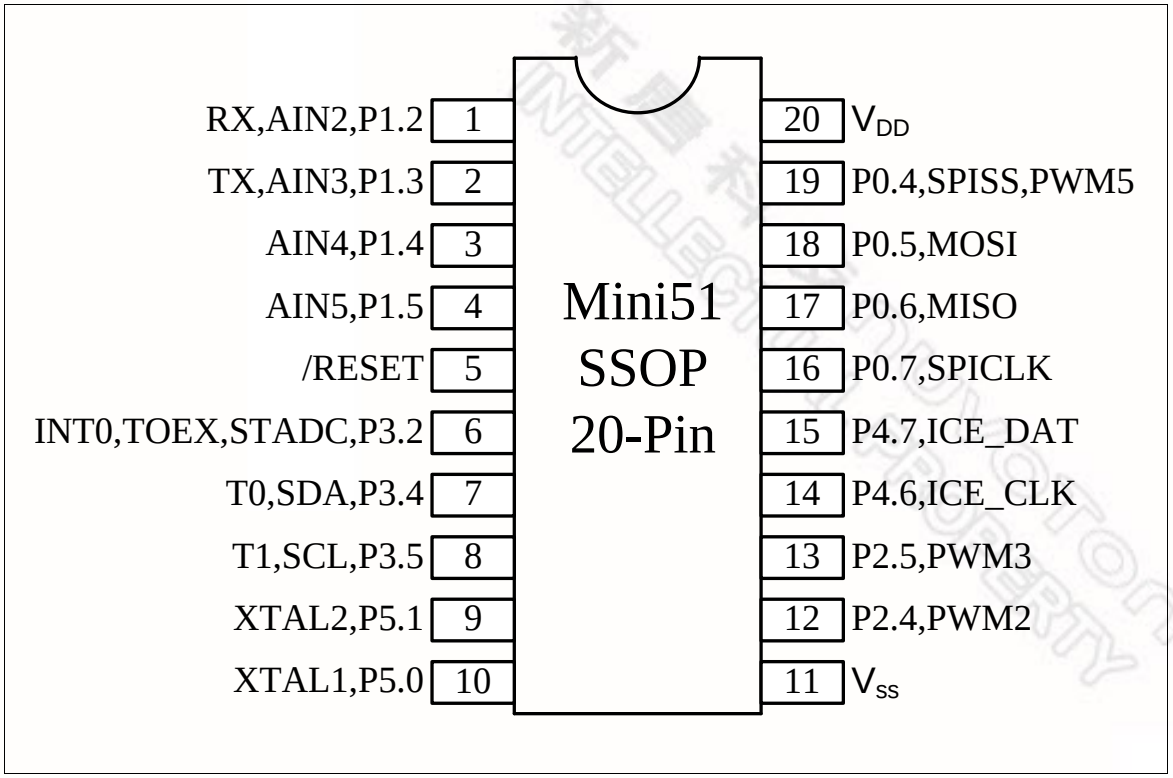


Figure 4.3-3 NuMicro Mini51™ Series TSSOP 20-pin Diagram

4.3.4 Mini54FHC (TSSOP20-pin)

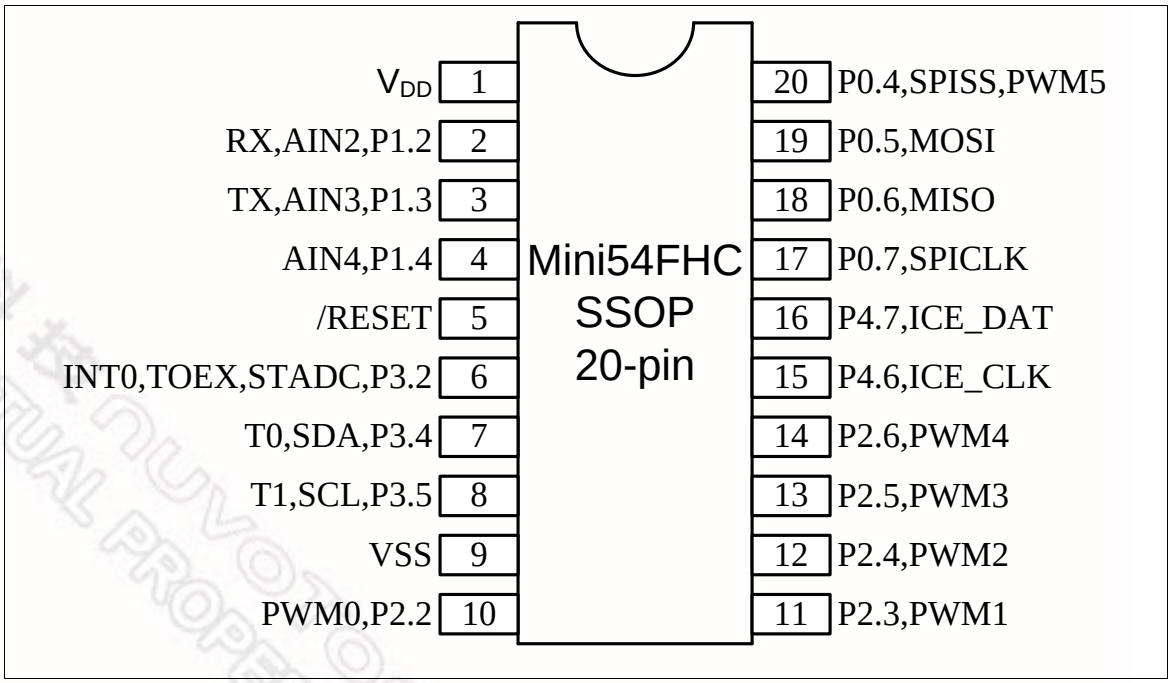


Figure 4.3-4 NuMicro Mini51™ Series TSSOP 20-pin Diagram

4.4 Pin Description

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
1	---	---	---	NC	**---**	Not connected
2	1	4	---	P1.5	**I/O**	General purpose digital I/O pin
				AIN5	**AI**	ADC analog input pin
				ACMP0_P	**AI**	Analog comparator positive input pin
3	2	5	5	/RESET	**I(ST)**	The Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. /RESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
4	3	---	---	P3.0	**I/O**	General purpose digital I/O pin
				AIN6	**AI**	ADC analog input pin
				ACMP1_N	**AI**	Analog comparator negative input pin
5	---	---	---	AV_{SS}	**AP**	Ground pin for analog circuit
6	4	---	---	P5.4	**I/O**	General purpose digital I/O pin
7	5	---	---	P3.1	**I/O**	General purpose digital I/O pin
				AIN7	**AI**	ADC analog input pin
				ACMP1_P	**AI**	Analog comparator positive input pin
8	6	6	6	P3.2	**I/O**	General purpose digital I/O pin
				INT0	**I**	External interrupt 0 input pin
				STADC	**I**	ADC external trigger input pin
				T0EX	**I**	Timer 0 external capture/reset trigger input pin
				ACMP1_P	**AI**	Analog comparator positive input pin
9	7	7	7	P3.4	**I/O**	General purpose digital I/O pin
				T0	**I/O**	Timer 0 external event counter input pin
				SDA	**I/O**	I^2C data I/O pin
				ACMP1_P	**AI**	Analog comparator positive input pin
10	8	8	8	P3.5	**I/O**	General purpose digital I/O pin
				T1	**I/O**	Timer 1 external event counter input pin
				SCL	**I/O**	I^2C clock I/O pin
				ACMP1_P	**AI**	Analog comparator positive input pin
11	---	---	---	NC	**---**	Not connected.
12	---	---	---	NC	**---**	Not connected.
13	---	--	--	NC	**---**	Not connected.

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
				ICE_CLK	**I**	Serial wired debugger clock pin.
30	20	15	16	P4.7	**I/O**	General purpose digital I/O pin.
				ICE_DAT	**I/O**	Serial wired debugger data pin.
31	---	---	---	NC	**---**	Not connected.
32	21	16	17	P0.7	**I/O**	General purpose digital I/O pin.
				SPICLK	**I/O**	SPI serial clock pin.
33	22	17	18	P0.6	**I/O**	General purpose digital I/O pin.
				MISO	**I/O**	SPI MISO (master in/slave out) pin.
34	23	18	19	P0.5	**I/O**	General purpose digital I/O pin.
				MOSI	**O**	SPI MOSI (master out/slave in) pin.
35	24	19	20	P0.4	**I/O**	General purpose digital I/O pin.
				SPISS	**I/O**	SPI slave select pin.
				PWM5	**O**	PWM5 output of PWM unit.
36	---	---	---	NC	**---**	Not connected.
37	25	---	---	P0.1	**I/O**	General purpose digital I/O pin.
				RTSn	**O**	UART RTS pin.
				RX	**I**	UART data receiver input pin.
				SPISS	**I/O**	SPI slave select pin.
38	26	---	---	P0.0	**I/O**	General purpose digital I/O pin.
				CTSn	**I**	UART CTS pin.
				TX	**O**	UART transmitter output pin.
39	---	---	---	NC	**---**	Not connected.
40	---	---	---	NC	**---**	Not connected.
41	27	---	---	P5.3	**I/O**	General purpose digital I/O pin.
				AIN0	**AI**	ADC analog input pin.
42	28	20	1	V_{DD}	**P**	Power supply for digital circuit.
43				AV_{DD}	**P**	Power supply for analog circuit.
44	29	---	---	P1.0	**I/O**	General purpose digital I/O pin.
				AIN1	**AI**	ADC analog input pin.
				ACMP0_P	**AI**	Analog comparator positive input pin.
45	30	1	2	P1.2	**I/O**	General purpose digital I/O pin.
				AIN2	**AI**	ADC analog input pin.

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
29	13	-	-	-	
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	-	-	-	
32	16	**GP5_INT**	GPIO	External signal interrupt from GPIO group P5 except P5.2	Yes
33	17	**HIRC_TRIM_INT**	HIRC	HIRC trim interrupt	No
34	18	**I2C_INT**	I^2C	I^2C interrupt	Yes
35 ~ 40	19 ~ 24	-	-	-	
41	25	**ACMP_INT**	ACMP	Analog Comparator 0 or Comparator 1 interrupt	Yes
42 ~ 43	26 ~ 27	-	-	-	
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	-	-	-	

Table 6.2-2 System Interrupt Map Vector Table

6.2.4 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table based address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with the exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer Value
Exception Number * 0x04	Exception Entry Pointer using that Exception Number

Table 6.2-3 Vector Table Format

6.3 System Manager

6.3.1 Overview

System management includes the following sections:

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.3.2 System Reset

The system reset can be included by one of the following listed events. For these reset events flags can be read by RSTSRC register.

- Power-On Reset (POR)
- Low level on the Reset Pin (/RESET)
- Watchdog Timer Time-out Reset (WDT)
- Brown-out Detector Reset (BOD)
- Cortex™-M0 MCU Reset
- CPU Reset

6.3.3 System Power Architecture

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. AV_{DD} must be equal to V_{DD} to avoid leakage current.
- Digital power from V_{DD} and V_{SS} supplies power to the I/O pins and internal regulator which provides a fixed 1.8V power for digital operation.
- Build-in a capacitor for internal voltage regulator

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level as the digital power (V_{DD}). The following figure shows the power distribution of the Mini51™DE series.

	Ext. CLK (HXT Or LXT)	HIRC	LIRC	PCLK
WDT	Yes	No	Yes	Yes
Timer0	Yes	Yes	Yes	Yes
Timer1	Yes	Yes	Yes	Yes
I²C	No	No	No	Yes
SPI	No	No	No	Yes
UART	Yes	Yes	No	No
PWM	No	No	No	Yes
ADC	Yes	Yes	No	Yes
ACMP	No	No	No	Yes

Table 6.4-1 Peripheral Clock Source Selection Table

6.4.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripheral clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator (LIRC) clock
- 32.768 kHz external low speed crystal oscillator (LXT) clock (If PD_32K = 1 and XTLCLK_EN[1:0] = 10)
- Peripherals Clock (When 10 kHz low speed oscillator is adopted as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

6.4.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\boldsymbol{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

if DIVIDER1(FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CKO pin directly.

- Two Interrupt source types:
  - Synchronously requested at PWM frequency when down counter comparison matched (edge- and center-aligned mode) or underflow (edge-aligned mode)
  - Requested when external fault brake asserted
    - BKP0: EINT0 or CPO1
    - BKP1: EINT1 or CPO0

- The PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register.
- Supports independently rising CMR matching (in Center-aligned mode), CNR matching (in Center-aligned mode), falling CMR matching, period matching to trigger ADC conversion
- Timer comparing matching event trigger PWM to do phase change in BLDC application
- Supports ACMP output event trigger PWM to force PWM output at most one period low, this feature is usually for step motor control
- Provides interrupt accumulation function

6.11 Serial Peripheral Interface (SPI)

6.11.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. The SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. SPI controller can be configured as a master or a slave device.

6.11.2 Features

- Supports Master or Slave mode operation
- Configurable transfer bit length
- Provides four 32-bit FIFO buffers
- Supports MSB first or LSB first transfer
- Supports byte reorder function
- Supports byte or word suspend mode
- Supports Slave 3-wire mode

6.14 Watchdog Timer (WDT)

6.14.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.14.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

7 ARM® CORTEX™-M0 CORE

7.1 Overview

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset and can be entered as a result of an exception return. The following figure shows the functional controller of the processor.

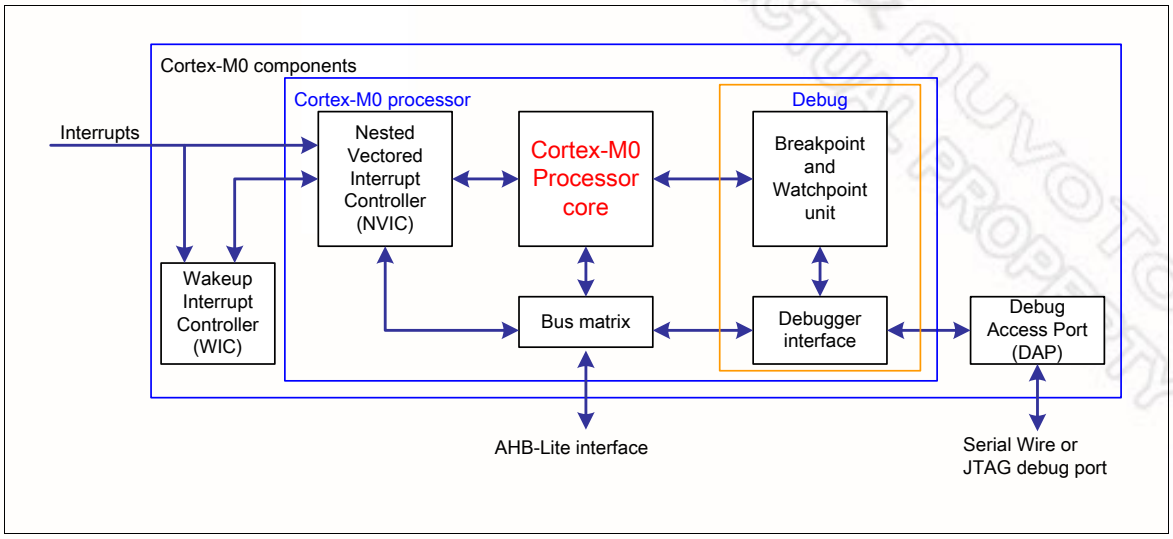


Figure 7.1-1 Functional Block Diagram

7.2 Features

- A low gate count processor
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model:

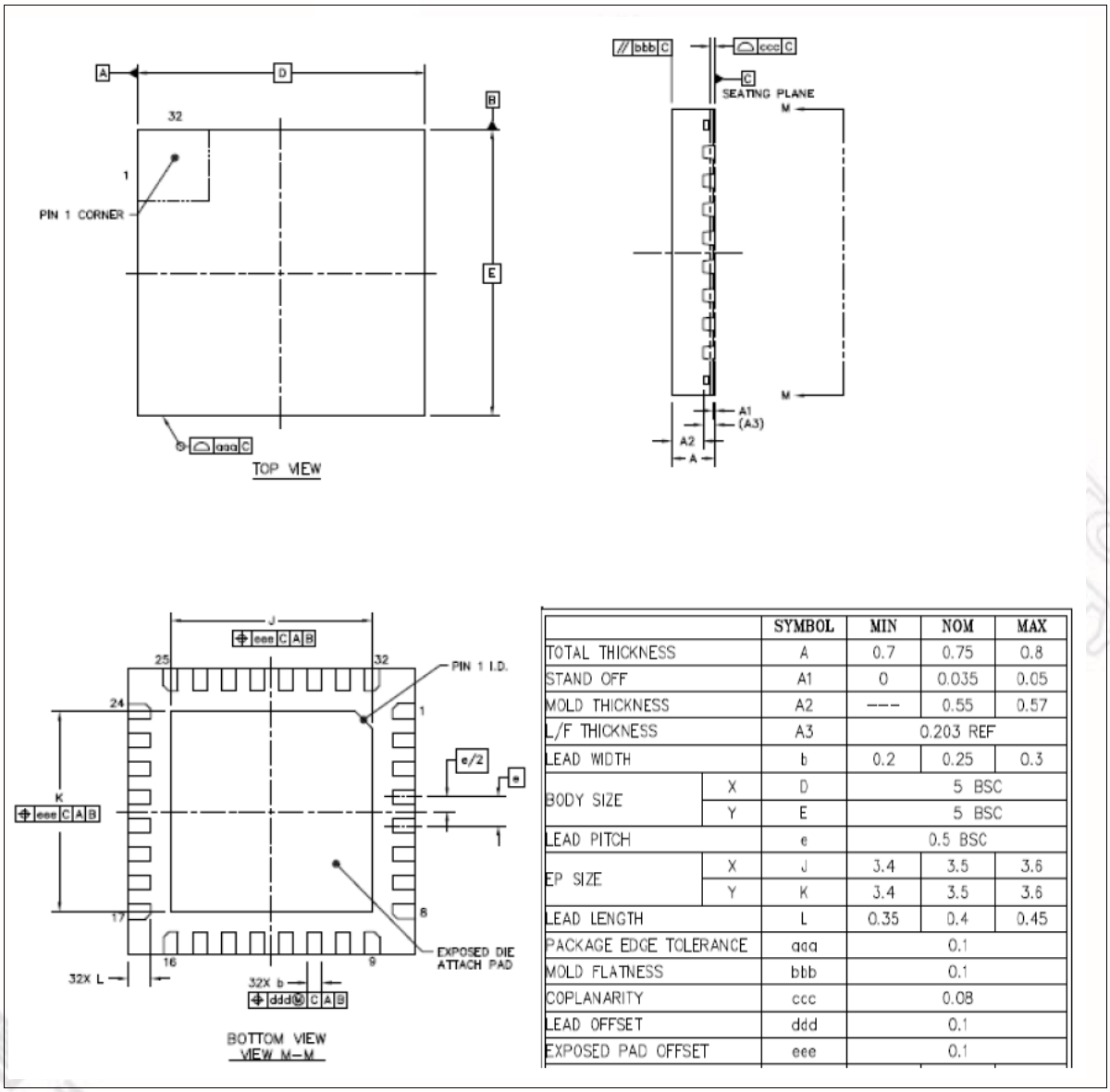
    This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power Idle mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC

I_{DD2}	Operating Current Normal Run Mode HCLK =22.1184 MHz while(1){} Executed from Flash	-	7.0	-	mA	V_{DD} 5.5V HXT 24 MHz HIRC Disabled All digital modules Disabled
I_{DD3}		-	7.1	-	mA	V_{DD} 3.3V HXT 24 MHz HIRC Disable All digital modules Enabled
I_{DD4}		-	5.0	-	mA	V_{DD} 3.3 V HXT 24 MHz HIRC Disabled All digital modules Disabled
I_{DD5}		-	6.1	-	mA	V_{DD} 5.5V HXT Disabled HIRC Enabled All digital modules Enabled
I_{DD6}		-	3.9	-	mA	. V_{DD} 5.5V HXT Disabled HIRC Enabled All digital modules Disabled
I_{DD7}		-	6.0	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled All digital modules Enabled
I_{DD8}		-	3.9	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled All digital modules Disabled

I_{IDLE16}	Operating Current Idle Mode at 10 kHz	-	1.1	-	mA	V_{DD} 3.3 V; HXT 4 MHz; HIRC Disabled; All digital modules Disabled
I_{IDLE17}		-	225	-	µA	V_{DD} 5.5 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Enabled; Only enable modules which support 10 kHz LIRC clock source
I_{IDLE18}		-	225	-	µA	V_{DD} 5.5 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Disabled
I_{IDLE19}		-	200	-	µA	V_{DD} 3.3 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Enabled; Only enable modules which support 10 kHz LIRC clock source
I_{IDLE20}		-	200	-	µA	V_{DD} 3.3 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Disabled
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)	-	10	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.
I_{PWD2}		-	9	-	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off.
I_{IL}	Logic 0 Input Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-	-70	-75	µA	V_{DD} = 5.5 V, V_{IN} = 0V

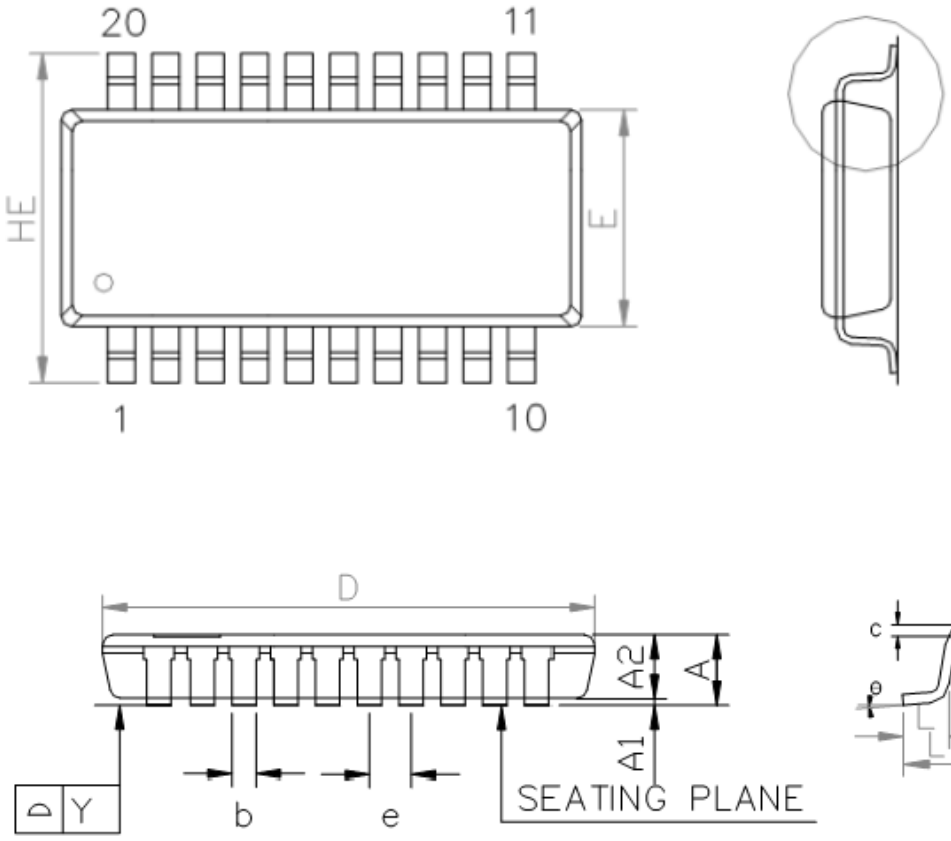
I_{TL}	Logic 1 to 0 Transition Current P0/1/2/3/4/5 (Quasi-bidirectional Mode) [*3]	-	-690	-750	µA	V_{DD} = 5.5 V, V_{IN} = 2.0V
I_{LK}	Input Leakage Current P0/1/2/3/4/5	-1	-	+1	µA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage P0/1/2/3/4/5 (TTL Input)	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
V_{IH1}	Input High Voltage P0/1/2/3/4/5 (TTL Input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{IL3}	Input Low Voltage XTAL1[*2]	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 2.5 V
V_{IH3}	Input High Voltage XTAL1[*2]	3.5	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{ILS}	Negative-going Threshold (Schmitt Input), /RESET	-0.3	-	0.2V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), /RESET	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
R_{RST}	Internal /RESETPin Pull-up Resistor	40		150	kΩ	V_{DD} = 2.5 V ~ 5.5V
V_{ILS}	Negative-going Threshold (Schmitt input), P0/1/2/3/4/5	-0.3	-	0.3V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt input), P0/1/2/3/4/5	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
I_{SR11}	Source Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-300	-400	-	µA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR12}		-50	-80	-	µA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR13}		-40	-73	-	µA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SR21}	Source Current P0/1/2/3/4/5 (Push-pull Mode)	-20	-26	-	mA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR22}		-3	-5	-	mA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR23}		-2.5	-5	-	mA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SK11}	Sink Current P0/1/2/3/4/5 (Quasi-bidirectional, Open-	10	15	-	mA	V_{DD} = 4.5 V, V_S = 0.45 V
I_{SK12}		6	9	-	mA	V_{DD} = 2.7 V, V_S = 0.45 V

10.3 33-pin QFN (5 mm x 5 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

10.4 20-pin TSSOP



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	—	0.30	0.007	—	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	—	0.20	0.004	—	0.008
θ	0°	—	8°	0°	—	8°
Y	0.10 BASIC			0.004 BASIC		