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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini52fde

Table of Contents

- Provides two channel 32-bit timers. One 8-bit pre-scale counter with 24-bit up counter for each timer
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous operation modes
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
- Provides event counter function
- Supports wake-up from Idle or Power-down mode

- WDT (Watchdog Timer)
  - Multiple clock sources
  - Supports wake-up from Idle or Power-down mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Independent 16-bit PWM duty control units with maximum six outputs
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake protections
  - Supports duty, period, and fault break interrupts
  - Supports duty/period trigger ADC conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period
  - Provides interrupt accumulation function
- UART (Universal Asynchronous Receiver/Transmitters)
  - One UART device
  - Buffered receiver and transmitter, each with 16-byte FIFO
  - Optional flow control function (CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports RS-485 function
- SPI (Serial Peripheral Interface)
  - One SPI devices
  - Supports Master/Slave mode

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer

Table 4.1-1 List of Abbreviations

4.3 PIN CONFIGURATION

4.3.1 LQFP 48-pin

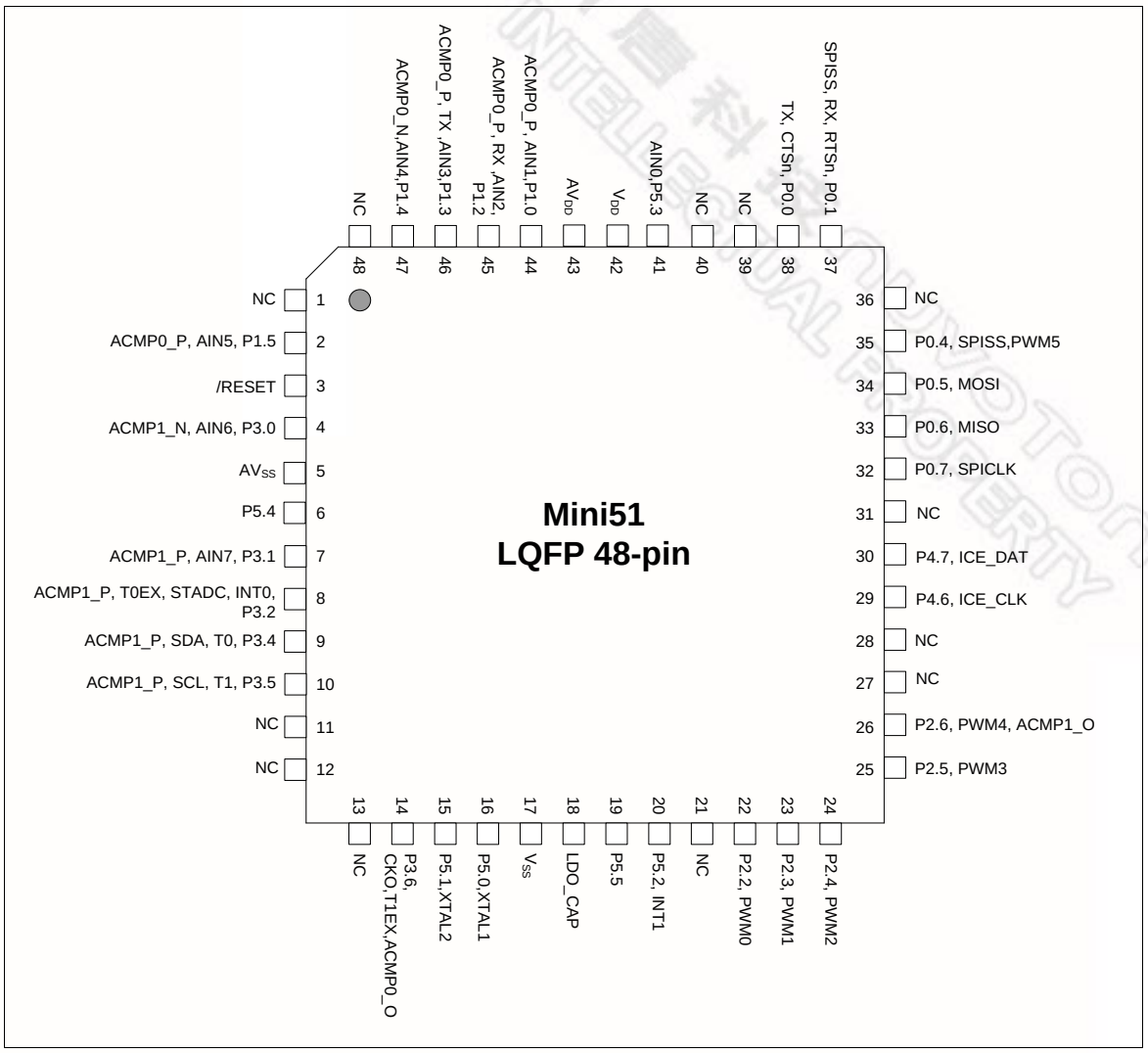


Figure 4.3-1 NuMicro Mini51™ Series LQFP 48-pin Diagram

4.3.3 TSSOP 20-pin

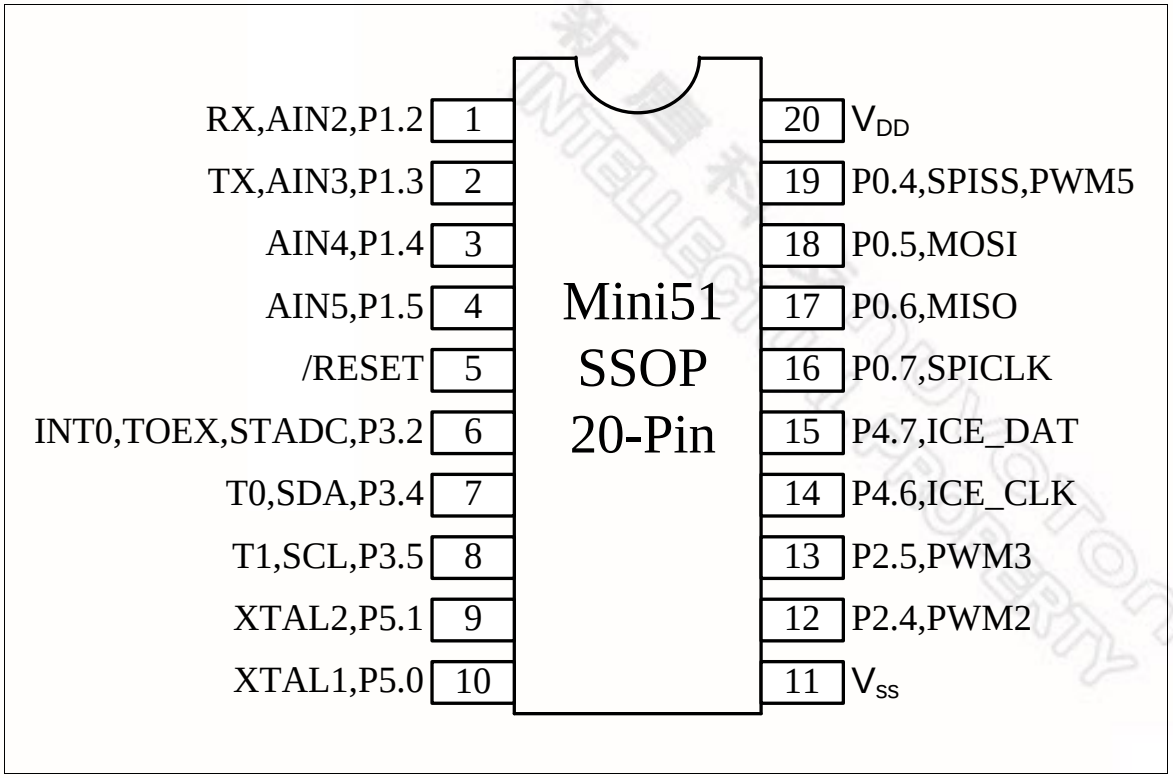


Figure 4.3-3 NuMicro Mini51™ Series TSSOP 20-pin Diagram

4.3.4 Mini54FHC (TSSOP20-pin)

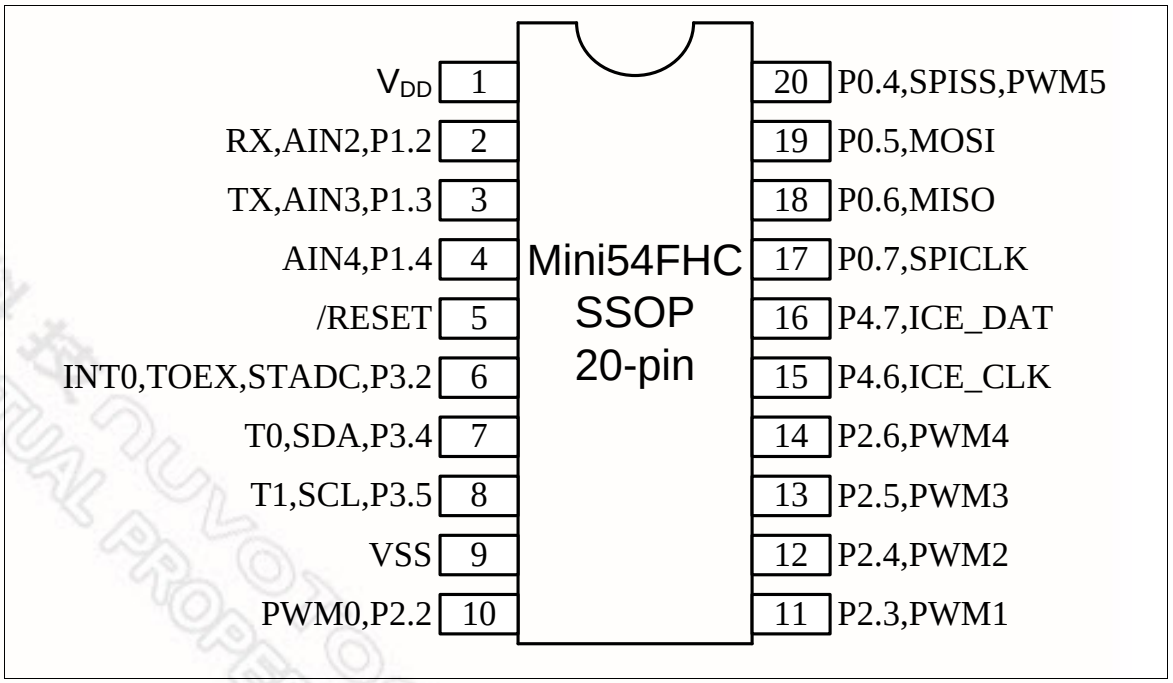


Figure 4.3-4 NuMicro Mini51™ Series TSSOP 20-pin Diagram

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
				RX	**I**	UART data receiver input pin.
				ACMP0_P	**AI**	Analog comparator positive input pin.
46	31	2	3	P1.3	**I/O**	General purpose digital I/O pin.
				AIN3	**AI**	ADC analog input pin.
				TX	**O**	UART transmitter output pin.
				ACMP0_P	**AI**	Analog comparator positive input pin.
47	32	3	4	P1.4	**I/O**	General purpose digital I/O pin.
				AIN4	**I/O**	PWM5: PWM output/Capture input.
				ACMP0_N	**AI**	Analog comparator negative input pin.
48	---	--	--	NC	**---**	Not connected.

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

5 BLOCK DIAGRAM

5.1 NuMicro Mini51™ Block Diagram

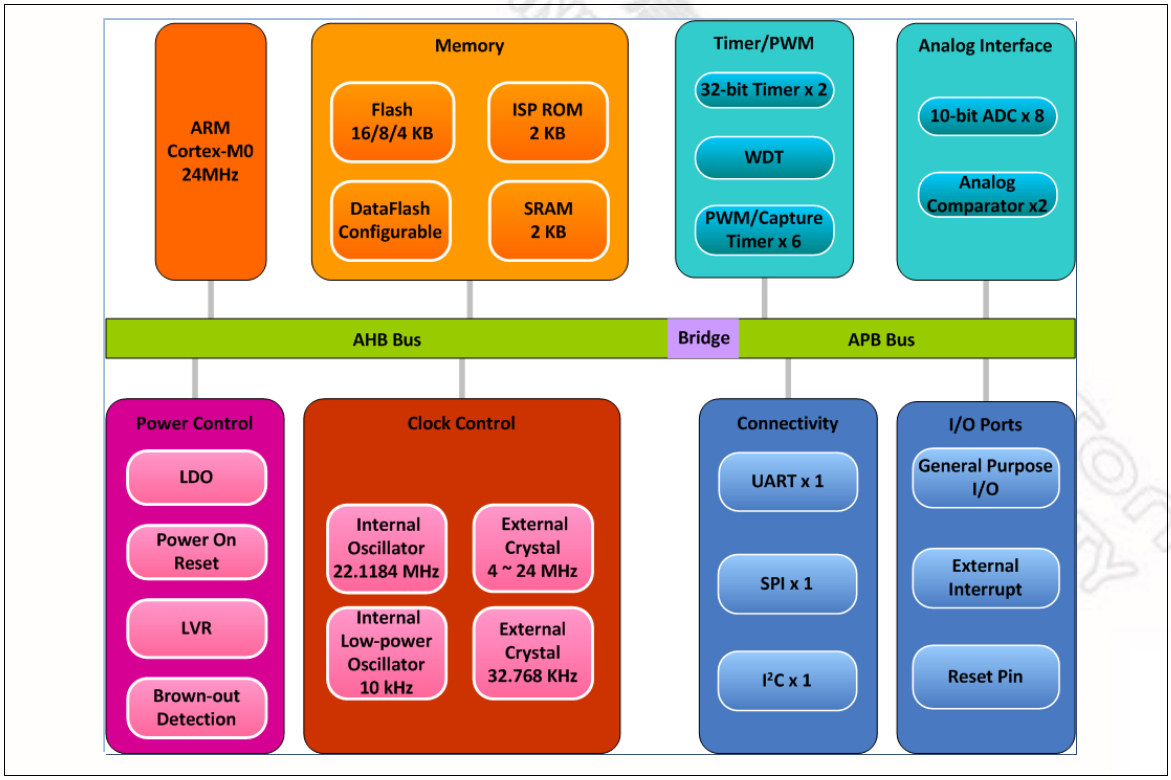


Figure 5.1-1 NuMicro Mini51™ Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Memory Organization

6.1.1 Overview

The NuMicro Mini51™ series provides 4G-byte addressing space. The addressing space assigned to each on-chip controllers is shown the following table. The detailed register definition, addressing space, and programming details will be described in the following sections for each on-chip peripheral. The NuMicro Mini51™ series only supports little-endian data format.

6.1.2 System Memory Map

The memory locations assigned to each on-chip controllers are shown in the following table.

Addressing Space	Token	Modules
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_3FFF	FLASH_BA	Flash Memory Space (16 KB)
0x2000_0000 – 0x2000_07FF	SRAM_BA	SRAM Memory Space (2 KB)
AHB Modules Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GP_BA	GPIO (P0~P5) Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB Modules Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C_BA	I^2C Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI_BA	SPI with Master/slave Function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM_BA	PWM Control Registers
0x4005_0000 – 0x4005_3FFF	UART_BA	UART Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
System Control Space (0xE000_E000 – 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	Nested Vectored Interrupt Control Registers
0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Block Registers

Table 6.1-1 Address Space Assignments for On-Chip Modules

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
29	13	-	-	-	
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	-	-	-	
32	16	**GP5_INT**	GPIO	External signal interrupt from GPIO group P5 except P5.2	Yes
33	17	**HIRC_TRIM_INT**	HIRC	HIRC trim interrupt	No
34	18	**I2C_INT**	I^2C	I^2C interrupt	Yes
35 ~ 40	19 ~ 24	-	-	-	
41	25	**ACMP_INT**	ACMP	Analog Comparator 0 or Comparator 1 interrupt	Yes
42 ~ 43	26 ~ 27	-	-	-	
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	-	-	-	

Table 6.2-2 System Interrupt Map Vector Table

6.2.4 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table based address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with the exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer Value
Exception Number * 0x04	Exception Entry Pointer using that Exception Number

Table 6.2-3 Vector Table Format

6.4.2 System Clock and SysTick Clock

The system clock has three clock sources which are generated from clock generator block. The clock source switches depending on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown below.

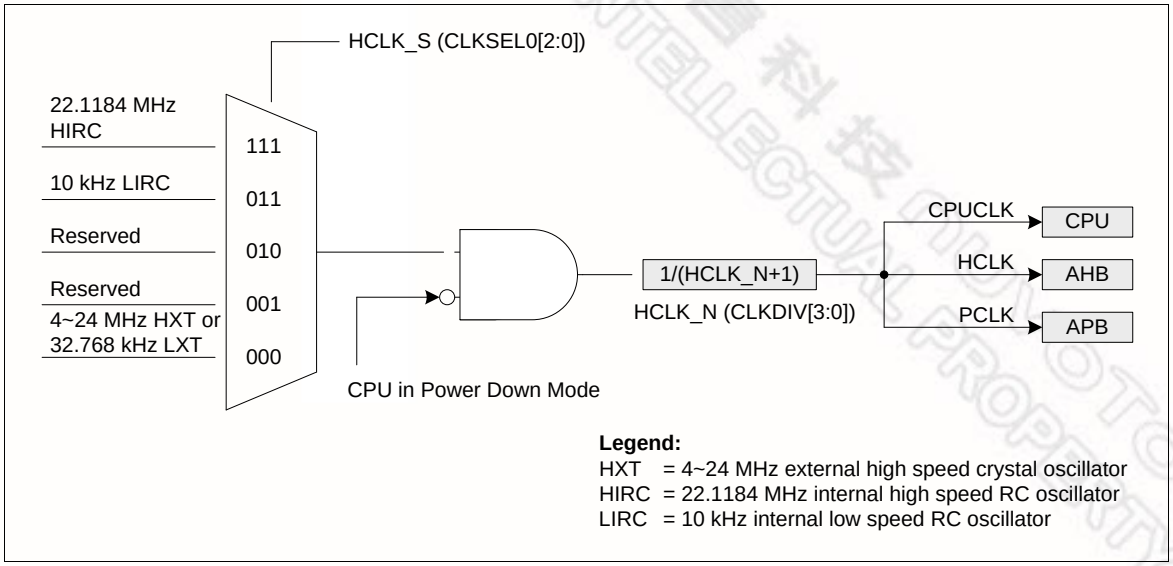


Figure 6.4-2 System Clock Block Diagram

The clock source of SysTick in Cortex™-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switches depending on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown below.

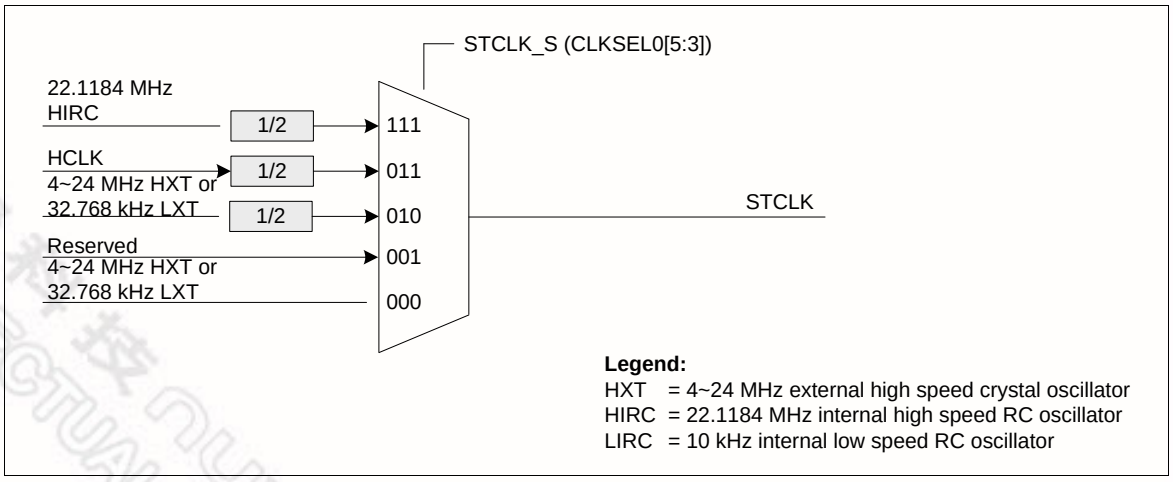


Figure 6.4-3 SysTick Clock Control Block Diagram

6.6 Analog-to-Digital Converter (ADC)

6.6.1 Overview

The NuMicro Mini51™ series contains one 10-bit successive approximation analog-to-digital converters (SAR A/D converter) with eight input channels. The A/D converters can be started by software, external pin (STADC/P3.2) or PWM trigger.

6.6.2 Features

- Analog input voltage range: 0 ~ Analog Supply Voltage from AV_{DD}
- 10-bit resolution and 8-bit accuracy is guaranteed
- Up to eight single-end analog input channels
- 300 KSPS (AV_{DD} 4.5V - 5.5V) and 200 KSPS (AV_{DD} 2.5V - 5.5V) conversion rate
- An A/D conversion is performed one time on a specified channel
- An A/D conversion can be started by:
  - Software write 1 to ADST bit
  - External pin STADC
  - PWM trigger with optional start delay period
- Each conversion result is held in data register with valid and overrun indicators
- Conversion results can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 2 input sources: External analog voltage and internal fixed band-gap voltage

6.8 General Purpose I/O (GPIO)

6.8.1 Overview

The NuMicro Mini51™ series have up to 30 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 30 pins are arranged in 6 ports named as P0, P1, P2, P3, P4 and P5. Each of the 30 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each pin can be configured by software individually as Input, Push-pull output, Open-drain output, or Quasi-bidirectional mode. For Quasi-bidirectional mode, each I/O pin is equipped with a very weak individual pull-up resistor about 110 kΩ ~ 300 kΩ for V_{DD} is from 5.0 V to 2.5 V.

6.8.2 Features

- Four I/O modes:
  - Input-only with high impendence
  - Push-pull output
  - Open-drain output
  - Quasi-bidirectional
- TTL/Schmitt trigger input mode selected by Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function
- High driver and high sink I/O mode support
- Configurable default I/O mode of all pins after reset by CIOINI (Config0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in Input tri-state mode after chip reset (default)

6.13 UART Controller (UART)

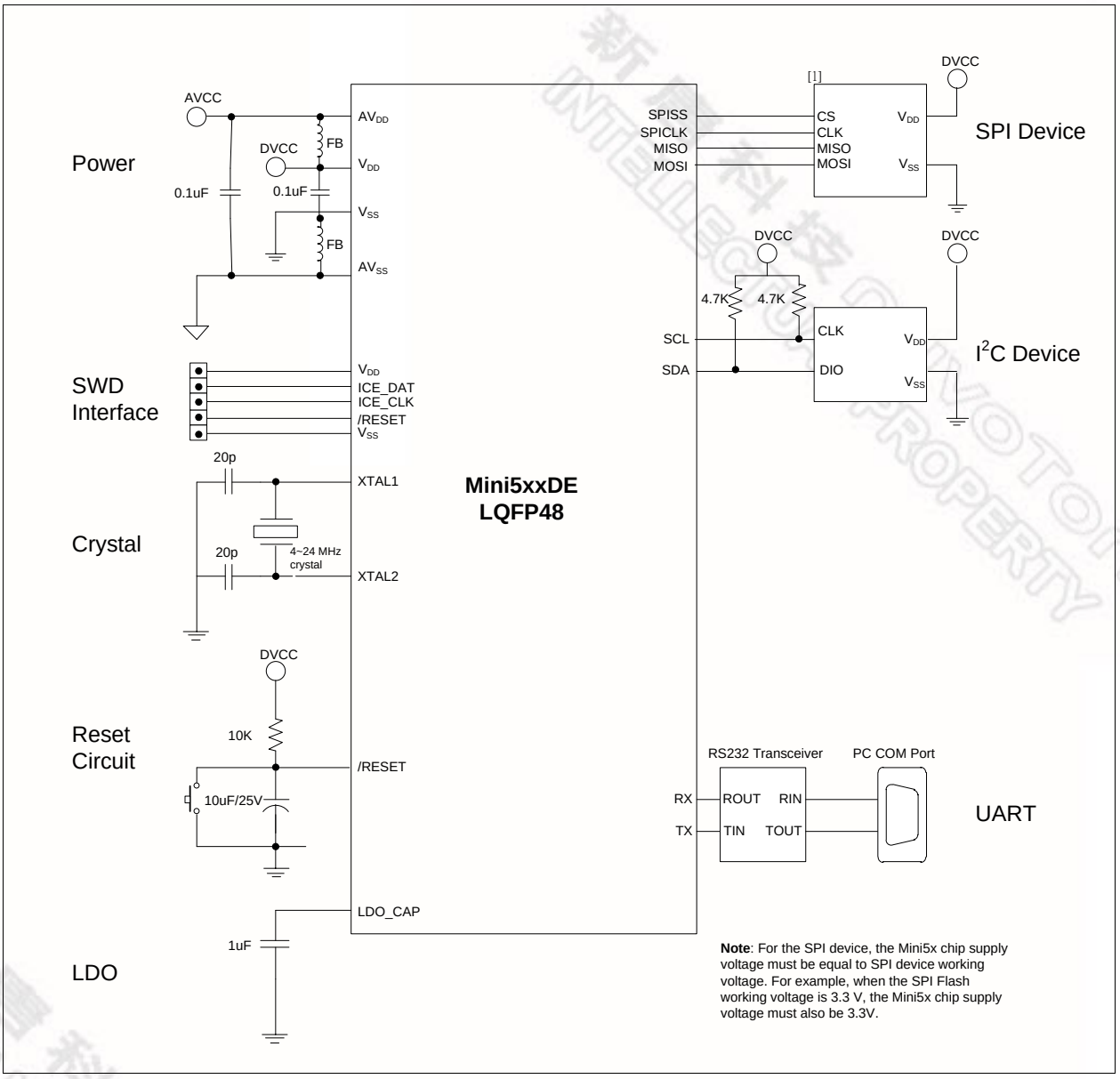
6.13.1 Overview

The NuMicro Mini51™ series provides one channel of Universal Asynchronous Receiver/Transmitters (UART). UART Controller performs Normal Speed UART, and supports flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, and RS-485 function mode.

6.13.2 Features

- Full duplex, asynchronous communications
- Separates 16-byte receive and transmitted FIFO for data payloads
- Supports hardware auto flow control, flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY(UA_TOR[15:8]) register
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit
  - Programmable stop bit, 1, 1.5, or 2 stop bit
- Supports IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enable to program RTS pin to control RS-485 transmission direction directly

8 APPLICATION CIRCUIT



9 MINI51XXDE ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

9.2 DC Electrical Characteristics

(VDD - VSS = 2.5 ~ 5.5 V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operation voltage	2.5	-	5.5	V	V_{DD} = 2.5V ~ 5.5V up to 24 MHz
V_{SS} / AV_{SS}	Power Ground	-0.3	-	-	V	
V_{LDO}	LDO Output Voltage	1.62	1.8	1.98	V	V_{DD} ≥ 2.5 V
V_{BG}	Band-gap Voltage	1.20	1.24	1.28	V	V_{DD} = 2.5V ~ 5.5V, T_A = 25°C
		1.18	1.24	1.32	V	V_{DD} = 2.5V ~ 5.5V, T_A = -40°C~105°C
V_{DD}-AV_{DD}	Allowed Voltage Difference for V_{DD} and AV_{DD}	-0.3	0	0.3	V	-
I_{DD1}	Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Executed from Flash	-	9.2	-	mA	V_{DD} 5.5V; HXT 24 MHz; HIRC Disable; All digital modules Enabled

I_{IDLE9}	Operating Current Idle Mode HCLK =12 MHz	-	4.4	-	mA	V_{DD} 5.5 V HXT 12 MHz HIRC Disabled All digital modules Enabled
I_{IDLE10}		-	3.3	-	mA	V_{DD} 5.5 V HXT 12 MHz HIRC Disabled All digital modules Disabled
I_{IDLE11}		-	2.9	-	mA	V_{DD} 3.3 V HXT 12 MHz HIRC Disabled All digital modules Enabled
I_{IDLE12}		-	1.8	-	mA	V_{DD} 3.3 V HXT 12 MHz HIRC Disabled All digital modules Disabled
I_{IDLE13}	Operating Current Idle Mode HCLK =4 MHz	-	2.9	-	mA	V_{DD} 5.5 V HXT 4 MHz HIRC Disabled All digital modules Enabled
I_{IDLE14}		-	2.5	-	mA	V_{DD} 5.5 V HXT 4 MHz HIRC Disabled All digital modules Disabled
I_{IDLE15}		-	1.5	-	mA	V_{DD} 3.3 V HXT 4 MHz HIRC Disabled All digital modules Enabled

I_{IDLE16}	Operating Current Idle Mode at 10 kHz	-	1.1	-	mA	V_{DD} 3.3 V; HXT 4 MHz; HIRC Disabled; All digital modules Disabled
I_{IDLE17}		-	225	-	µA	V_{DD} 5.5 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Enabled; Only enable modules which support 10 kHz LIRC clock source
I_{IDLE18}		-	225	-	µA	V_{DD} 5.5 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Disabled
I_{IDLE19}		-	200	-	µA	V_{DD} 3.3 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Enabled; Only enable modules which support 10 kHz LIRC clock source
I_{IDLE20}		-	200	-	µA	V_{DD} 3.3 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Disabled
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)	-	10	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.
I_{PWD2}		-	9	-	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off.
I_{IL}	Logic 0 Input Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-	-70	-75	µA	V_{DD} = 5.5 V, V_{IN} = 0V

I_{SK13}	Drain and Push-pull Mode)	5	8	-	mA	V_{DD} = 2.5 V, V_S = 0.45 V

Notes:

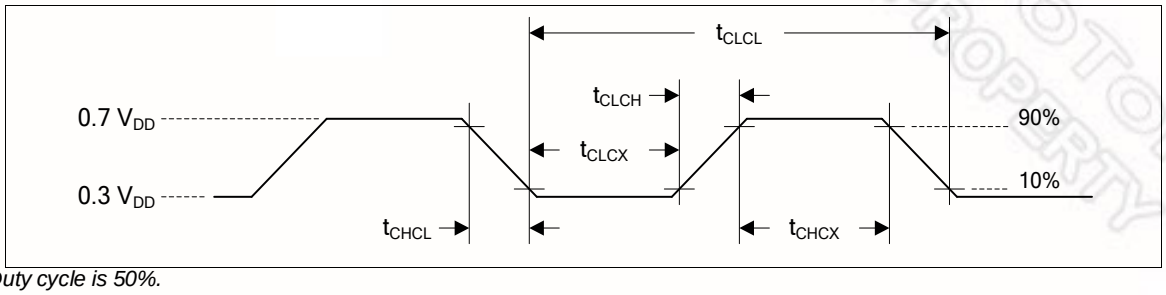
1. /RESET pin is a Schmitt trigger input.

2. XTAL1 is a CMOS input.

3. Pins of P0, P1, P2, P3, P4 and P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of VDD=5.5V, the transition current reaches its maximum value when VIN approximates to 2V.

9.3 AC Electrical Characteristics

9.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

9.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	2.5	-	mA	12 MHz, V_{DD} = 5.5V
		-	1.0	-	mA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

9.3.3 Typical Crystal Application Circuits

Crystal	C1	C2
4MHz ~ 24 MHz	10~20 pF	10~20 pF

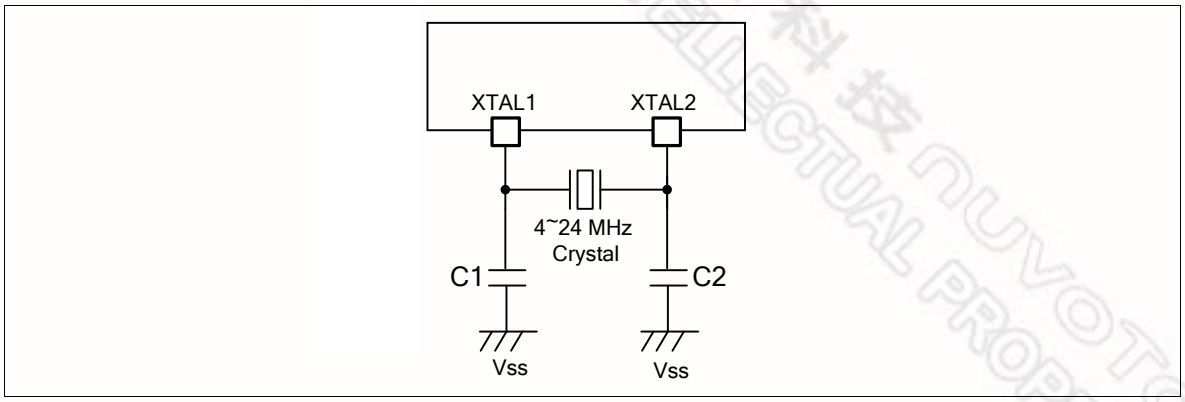
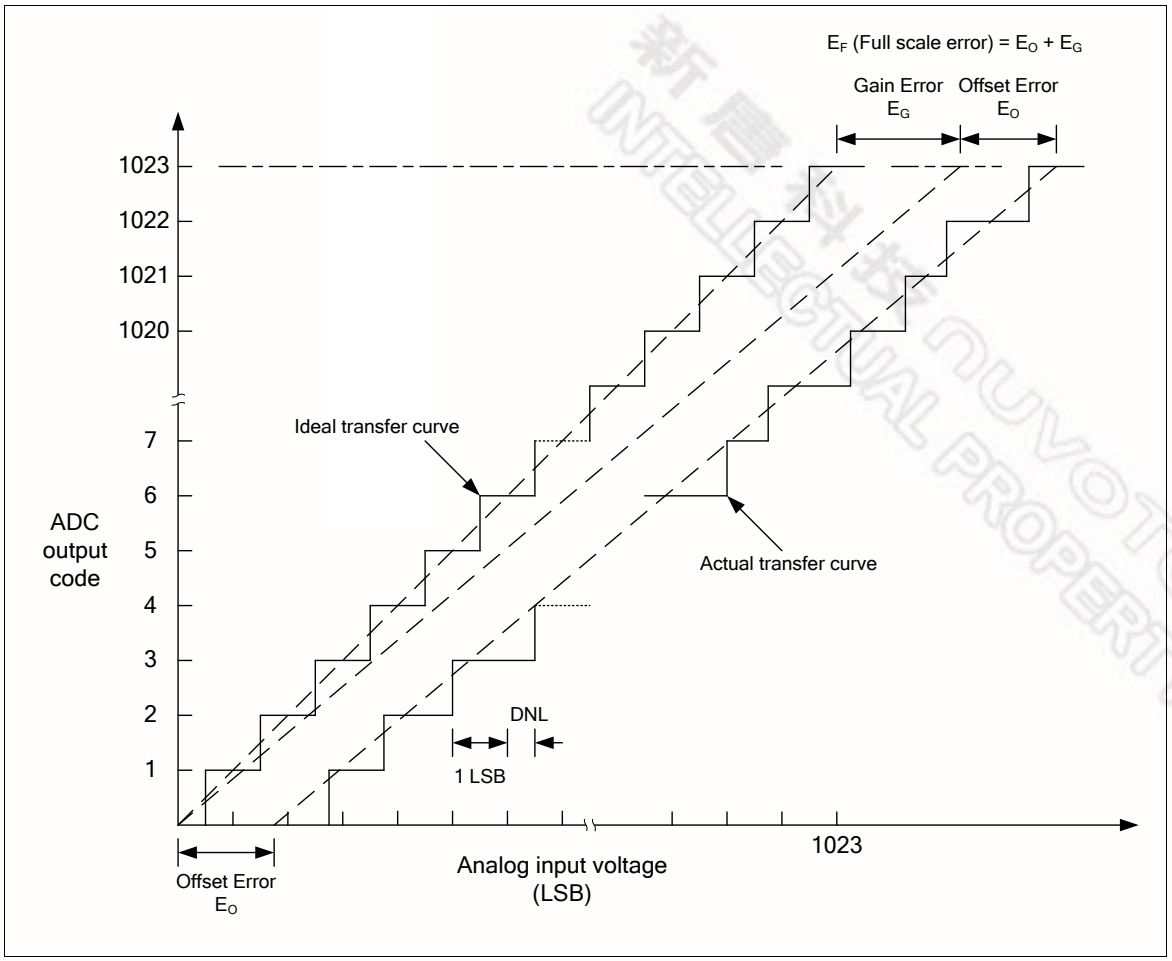


Figure 9-1Mini5xDE Typical Crystal Application Circuit

9.3.4 22.1184 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	22.1184		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5 V
		-2	-	+2	%	T_A = -40℃~105℃ V_{DD}=2.5 V~ 5.5 V
I_{HRC}	Operating Current	-	700	-	μA	T_A = 25 ℃,V_{DD} = 5 V



9.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.5	-	5.5	V	-
V_{LDO}	Output Voltage	1.62	1.8	1.98	V	-
T_A	Temperature	-40	25	105	℃	

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

9.4.3 Low Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-