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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	33-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini52tde

LIST OF FIGURES

LIST OF TABLES

- Full-duplex synchronous serial data transfer
- Provides 3-wire function
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Rx latching data can be either at rising edge or at falling edge of serial clock
- Tx sending data can be either at rising edge or at falling edge of serial clock
- Supports Byte Suspend mode in 32-bit transmission
- 4-level depth FIFO buffer

- I^2C
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
  - Supports Power-down wake-up function
  - Support FIFO function
- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 300K SPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger, PWM trigger, or external pin trigger
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Build-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro Mini51™ Series Selection Code

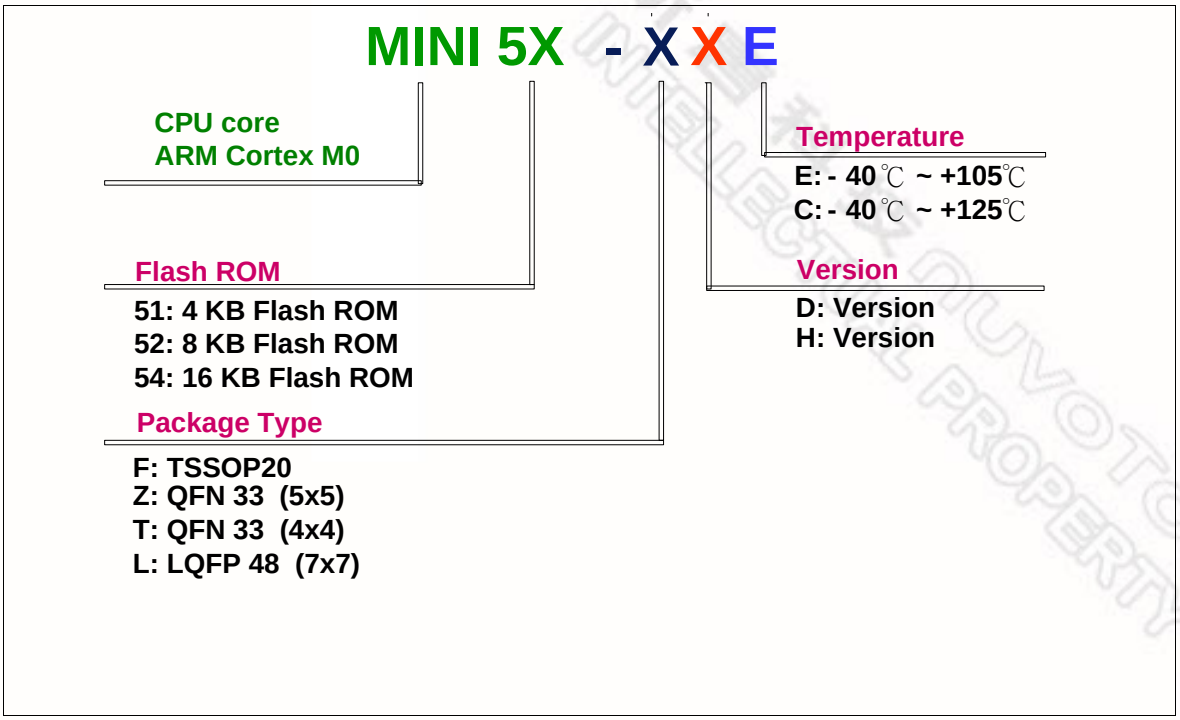


Figure 4.1-1 NuMicro Mini51™ Series Selection Code

4.3.2 QFN 33-pin

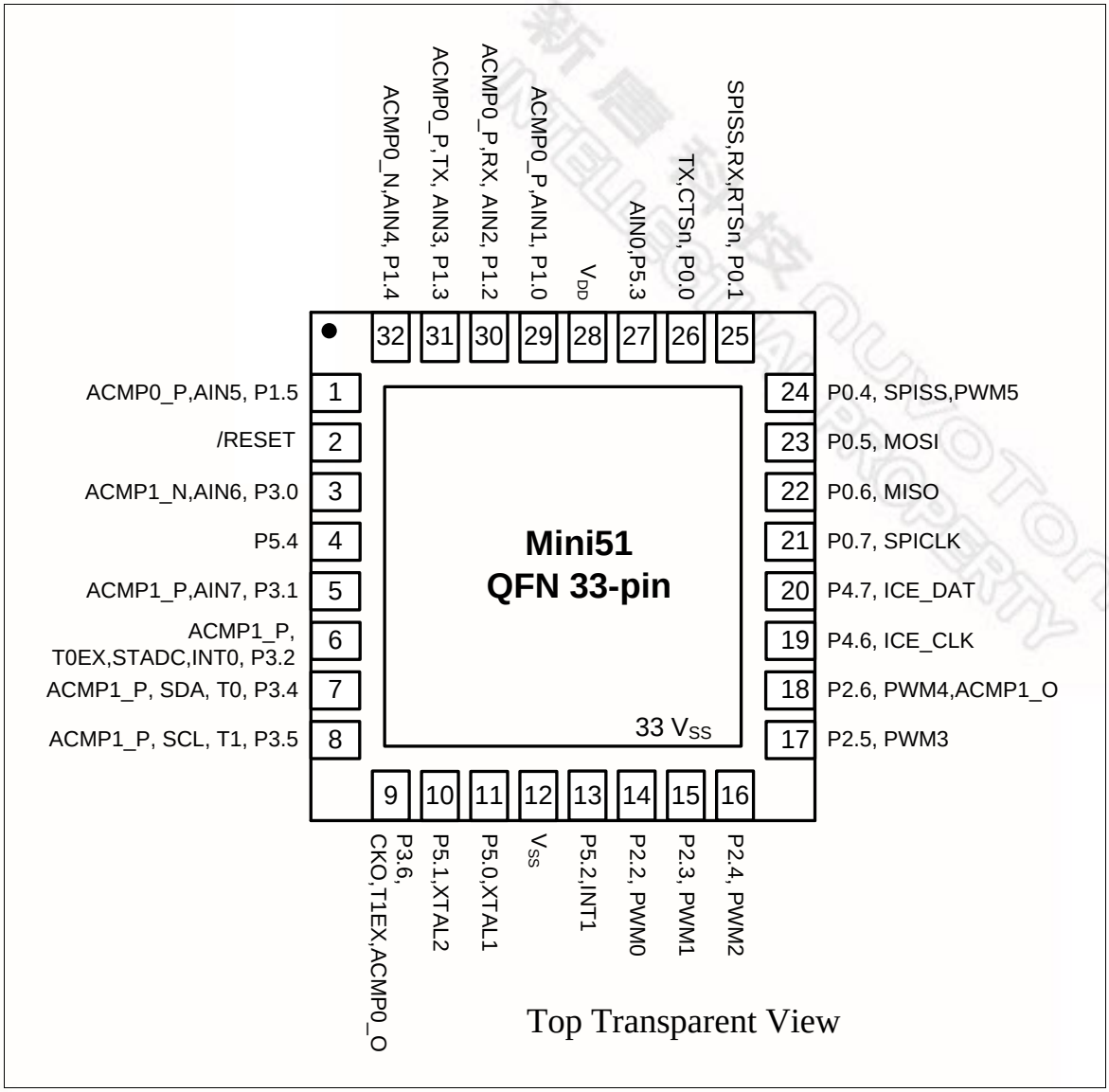


Figure 4.3-2 NuMicro Mini51™ Series QFN 33-pin Diagram

5 BLOCK DIAGRAM

5.1 NuMicro Mini51™ Block Diagram

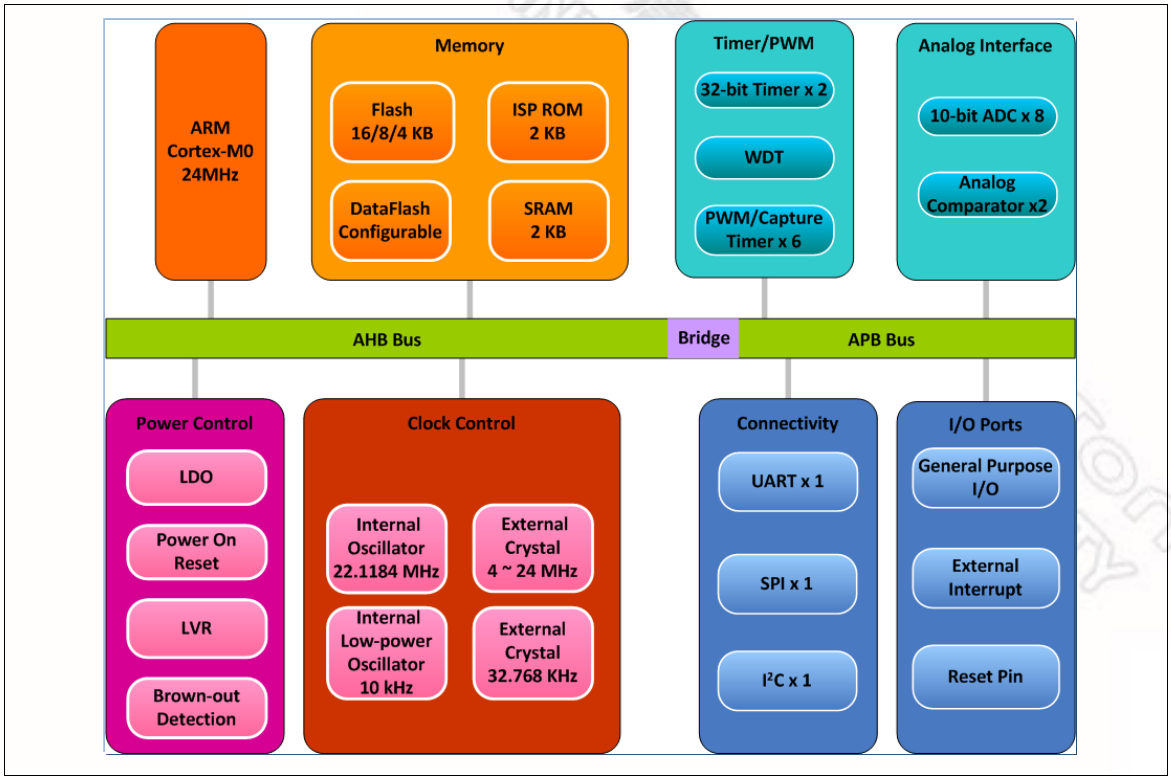


Figure 5.1-1 NuMicro Mini51™ Series Block Diagram

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
29	13	-	-	-	
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	-	-	-	
32	16	**GP5_INT**	GPIO	External signal interrupt from GPIO group P5 except P5.2	Yes
33	17	**HIRC_TRIM_INT**	HIRC	HIRC trim interrupt	No
34	18	**I2C_INT**	I^2C	I^2C interrupt	Yes
35 ~ 40	19 ~ 24	-	-	-	
41	25	**ACMP_INT**	ACMP	Analog Comparator 0 or Comparator 1 interrupt	Yes
42 ~ 43	26 ~ 27	-	-	-	
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	-	-	-	

Table 6.2-2 System Interrupt Map Vector Table

6.2.4 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table based address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with the exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer Value
Exception Number * 0x04	Exception Entry Pointer using that Exception Number

Table 6.2-3 Vector Table Format

6.4.3 ISP Clock Source Selection

The clock source of ISP is from AHB clock (HCLK). Please refer to the register AHBCLK.

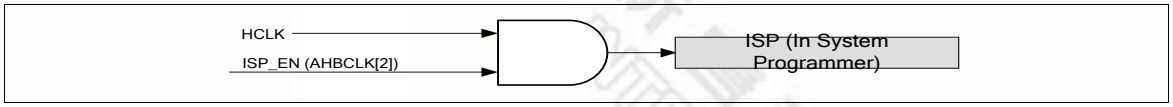


Figure 6.4-4 AHB Clock Source for HCLK

6.4.4 Module Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals. Please refer to the CLKSEL1 and APBCLK register description in section **Error! Reference source not found.**.

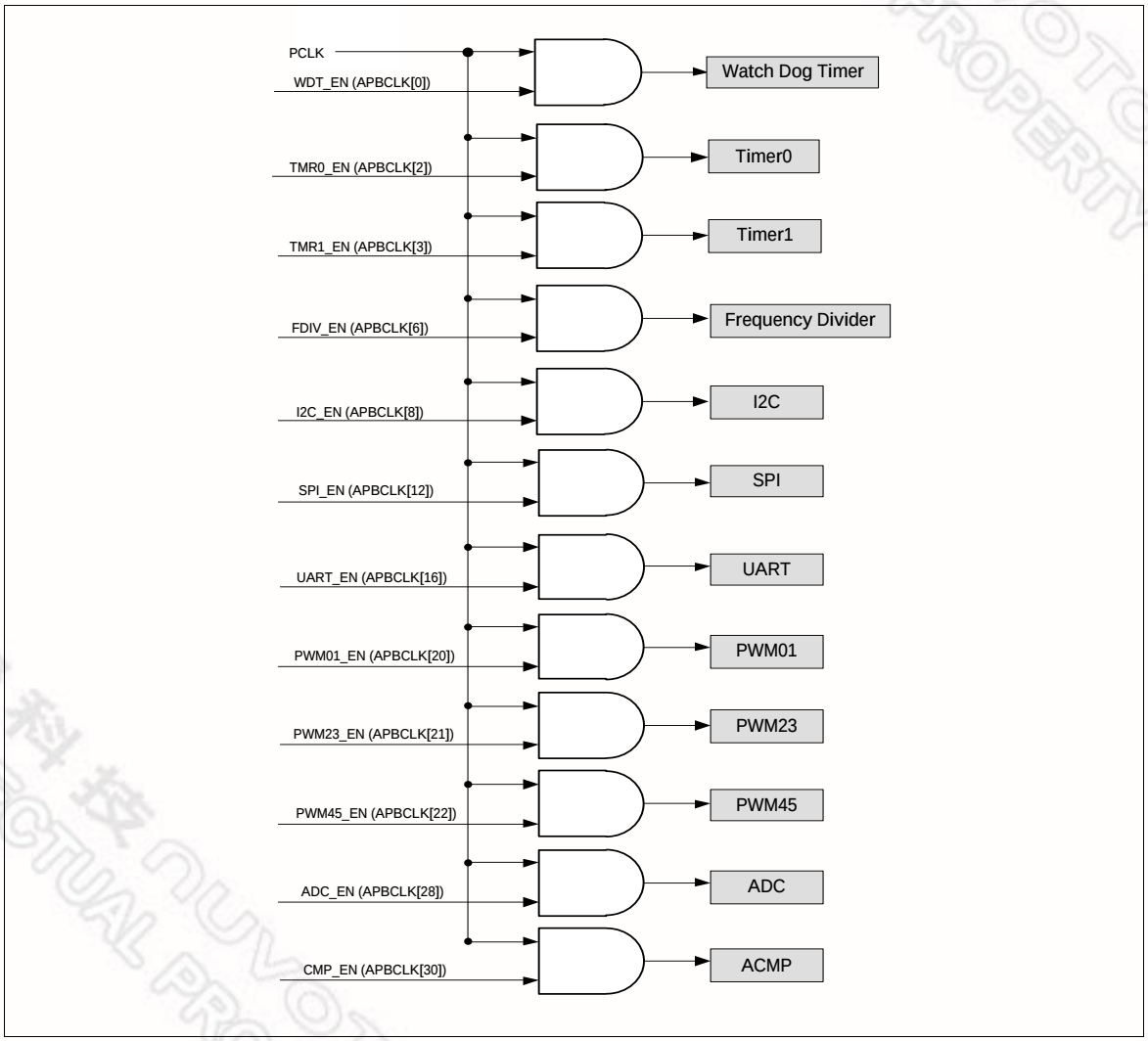


Figure 6.4-5 Peripherals Clock Source Selection for PCLK

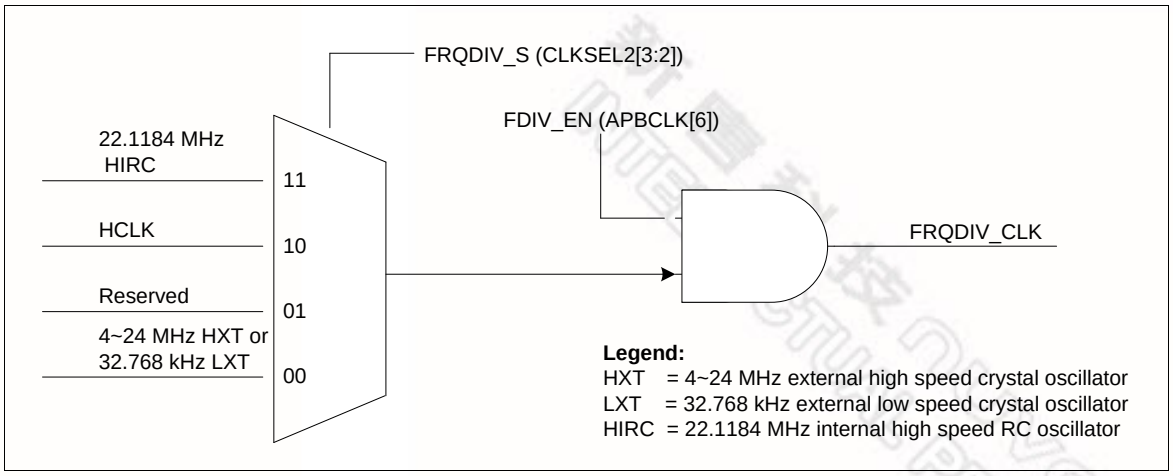


Figure 6.4-6 Clock Source of Frequency Divider

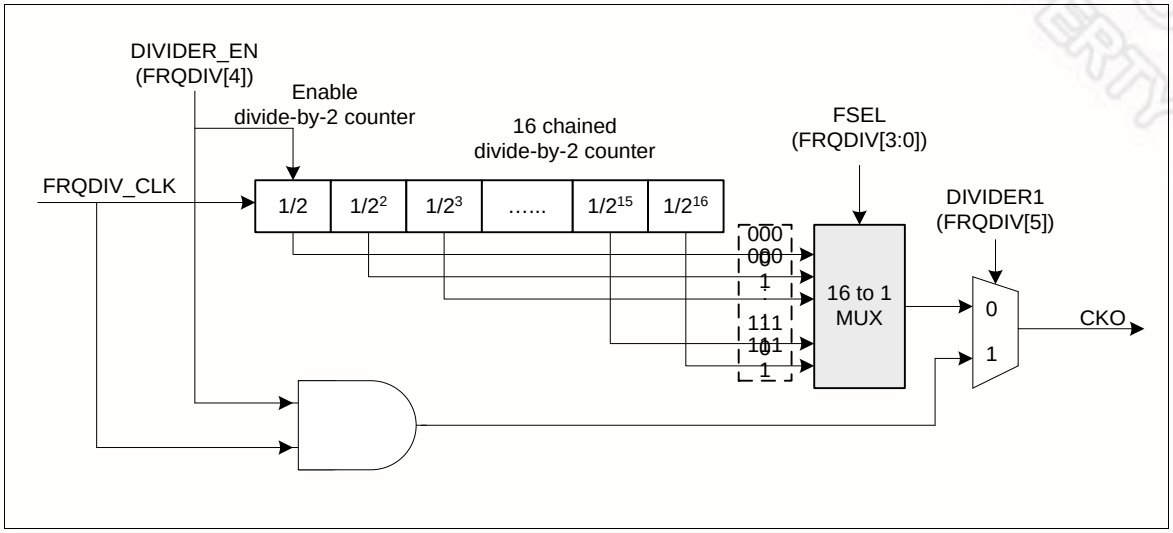


Figure 6.4-7 Block Diagram of Frequency Divider

6.7 Flash Memory Controller (FMC)

6.7.1 Overview

The NuMicro Mini51™ series is equipped with 4K/8K/16K bytes on chip embedded flash memory for application program (APROM) that can be updated through ISP procedure. In-System-Programming (ISP) and In-Application-Programming (IAP) enable user to update program memory when chip is soldered on PCB. After chip power on Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro Mini51™ series also provides Data Flash region that is shared with APROM and its start address is configurable and defined by user in CONFIG1.

6.7.2 Features

- Running up to 24 MHz with zero wait state for discontinuous address read access
- 4/8/16 Kbytes application program memory (APROM)
- 2 Kbytes in system programming (ISP) loader program memory (LDROM)
- Programmable data flash start address
- All embedded flash memory supports 512 bytes page erase
- In System Program (ISP)/In Application Program (IAP) to update on chip flash memory

6.10 Enhanced PWM Generator

6.10.1 Overview

The NuMicro Mini51™ series has built one PWM unit which is specially designed for motor driving control applications. The PWM unit supports six PWM generators which can be configured as six independent PWM outputs, PWM0~PWM5, or as three complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5) with three programmable dead-zone generators.

Every complementary PWM pairs share one 8-bit prescaler. There are six clock dividers providing five divided frequencies (1, 1/2, 1/4, 1/8, 1/16) for each channel. Each PWM output has independent 16-bit counter for PWM period control, and 16-bit comparators for PWM duty control. The six PWM generators provide twelve independent PWM interrupt flags which are set by hardware when the corresponding PWM period counter comparison matched period and duty. Each PWM interrupt source with its corresponding enable bit can request PWM interrupt. The PWM generators can be configured as One-shot mode to produce only one PWM cycle signal or Auto-reload mode to output PWM waveform continuously.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be loaded into the 16-bit down counter/ comparator at the end of current period. The double buffering feature avoids glitch at PWM outputs.

Besides PWM, Motor controlling also need Timer, ACMP and ADC to work together. In order to control motor more precisely, we provide some registers that not only configure PWM but also Timer, ADC and ACMP, by doing so, it can save more CPU time and control motor with ease especially in BLDC.

6.10.2 Features

The PWM unit supports the following features:

- Independent 16-bit PWM duty control units with maximum six port pins:
  - Six independent PWM outputs – PWM0, PWM1, PWM2, PWM3, PWM4, and PWM5
  - Three complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-zone insertion – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
  - Three synchronous PWM pairs, with each pin in a pair in-phase – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
- Group control bit – PWM2 and PWM4 are synchronized with PWM0, PWM3 and PWM5 are synchronized with PWM1
- One-shot (only support edge alignment mode) or Auto-reload mode PWM
- Up to 16-bit resolution
- Supports Edge-aligned and Center-aligned mode
- Programmable dead-zone insertion between complementary paired PWMs
- Each pin of PWM0 to PWM5 has independent polarity setting control
- Hardware fault brake protections

- Two Interrupt source types:
  - Synchronously requested at PWM frequency when down counter comparison matched (edge- and center-aligned mode) or underflow (edge-aligned mode)
  - Requested when external fault brake asserted
    - BKP0: EINT0 or CPO1
    - BKP1: EINT1 or CPO0

- The PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register.
- Supports independently rising CMR matching (in Center-aligned mode), CNR matching (in Center-aligned mode), falling CMR matching, period matching to trigger ADC conversion
- Timer comparing matching event trigger PWM to do phase change in BLDC application
- Supports ACMP output event trigger PWM to force PWM output at most one period low, this feature is usually for step motor control
- Provides interrupt accumulation function

7 ARM® CORTEX™-M0 CORE

7.1 Overview

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset and can be entered as a result of an exception return. The following figure shows the functional controller of the processor.

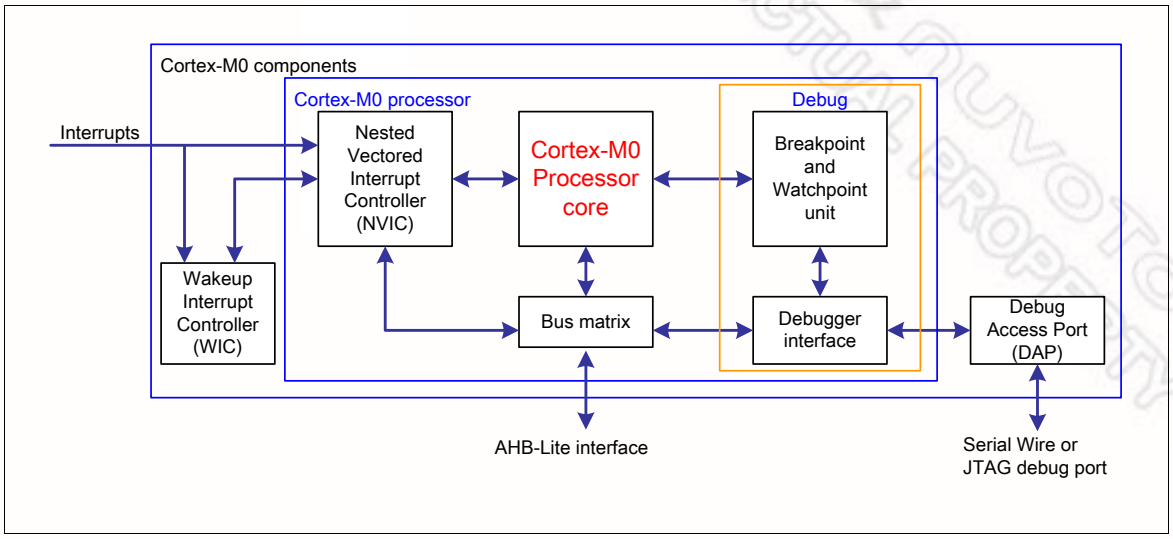


Figure 7.1-1 Functional Block Diagram

7.2 Features

- A low gate count processor
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model:

    This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power Idle mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC

I_{DD2}	Operating Current Normal Run Mode HCLK =22.1184 MHz while(1){} Executed from Flash	-	7.0	-	mA	V_{DD} 5.5V HXT 24 MHz HIRC Disabled All digital modules Disabled
I_{DD3}		-	7.1	-	mA	V_{DD} 3.3V HXT 24 MHz HIRC Disable All digital modules Enabled
I_{DD4}		-	5.0	-	mA	V_{DD} 3.3 V HXT 24 MHz HIRC Disabled All digital modules Disabled
I_{DD5}		-	6.1	-	mA	V_{DD} 5.5V HXT Disabled HIRC Enabled All digital modules Enabled
I_{DD6}		-	3.9	-	mA	. V_{DD} 5.5V HXT Disabled HIRC Enabled All digital modules Disabled
I_{DD7}		-	6.0	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled All digital modules Enabled
I_{DD8}		-	3.9	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled All digital modules Disabled

I_{IDLE9}	Operating Current Idle Mode HCLK =12 MHz	-	4.4	-	mA	V_{DD} 5.5 V HXT 12 MHz HIRC Disabled All digital modules Enabled
I_{IDLE10}		-	3.3	-	mA	V_{DD} 5.5 V HXT 12 MHz HIRC Disabled All digital modules Disabled
I_{IDLE11}		-	2.9	-	mA	V_{DD} 3.3 V HXT 12 MHz HIRC Disabled All digital modules Enabled
I_{IDLE12}		-	1.8	-	mA	V_{DD} 3.3 V HXT 12 MHz HIRC Disabled All digital modules Disabled
I_{IDLE13}	Operating Current Idle Mode HCLK =4 MHz	-	2.9	-	mA	V_{DD} 5.5 V HXT 4 MHz HIRC Disabled All digital modules Enabled
I_{IDLE14}		-	2.5	-	mA	V_{DD} 5.5 V HXT 4 MHz HIRC Disabled All digital modules Disabled
I_{IDLE15}		-	1.5	-	mA	V_{DD} 3.3 V HXT 4 MHz HIRC Disabled All digital modules Enabled

I_{IDLE16}	Operating Current Idle Mode at 10 kHz	-	1.1	-	mA	V_{DD} 3.3 V; HXT 4 MHz; HIRC Disabled; All digital modules Disabled
I_{IDLE17}		-	225	-	µA	V_{DD} 5.5 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Enabled; Only enable modules which support 10 kHz LIRC clock source
I_{IDLE18}		-	225	-	µA	V_{DD} 5.5 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Disabled
I_{IDLE19}		-	200	-	µA	V_{DD} 3.3 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Enabled; Only enable modules which support 10 kHz LIRC clock source
I_{IDLE20}		-	200	-	µA	V_{DD} 3.3 V; HXT Disabled; HIRC Disabled; LIRC Enabled; All digital modules Disabled
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)	-	10	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.
I_{PWD2}		-	9	-	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off.
I_{IL}	Logic 0 Input Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-	-70	-75	µA	V_{DD} = 5.5 V, V_{IN} = 0V

I_{SK13}	Drain and Push-pull Mode)	5	8	-	mA	V_{DD} = 2.5 V, V_S = 0.45 V

Notes:

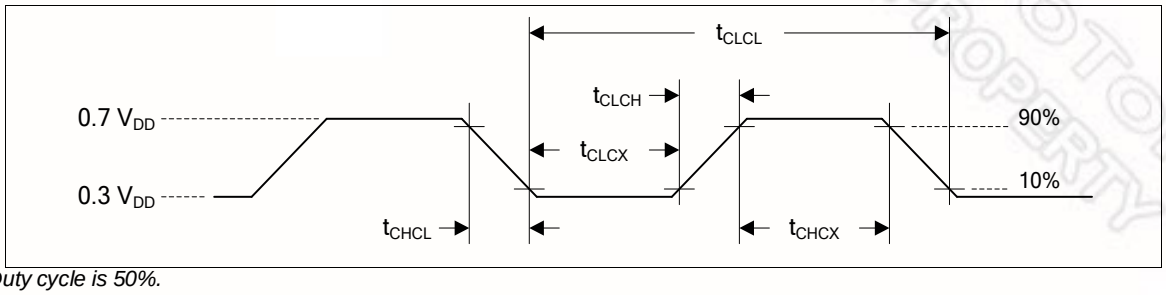
1. /RESET pin is a Schmitt trigger input.

2. XTAL1 is a CMOS input.

3. Pins of P0, P1, P2, P3, P4 and P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of VDD=5.5V, the transition current reaches its maximum value when VIN approximates to 2V.

9.3 AC Electrical Characteristics

9.3.1 External Input Clock

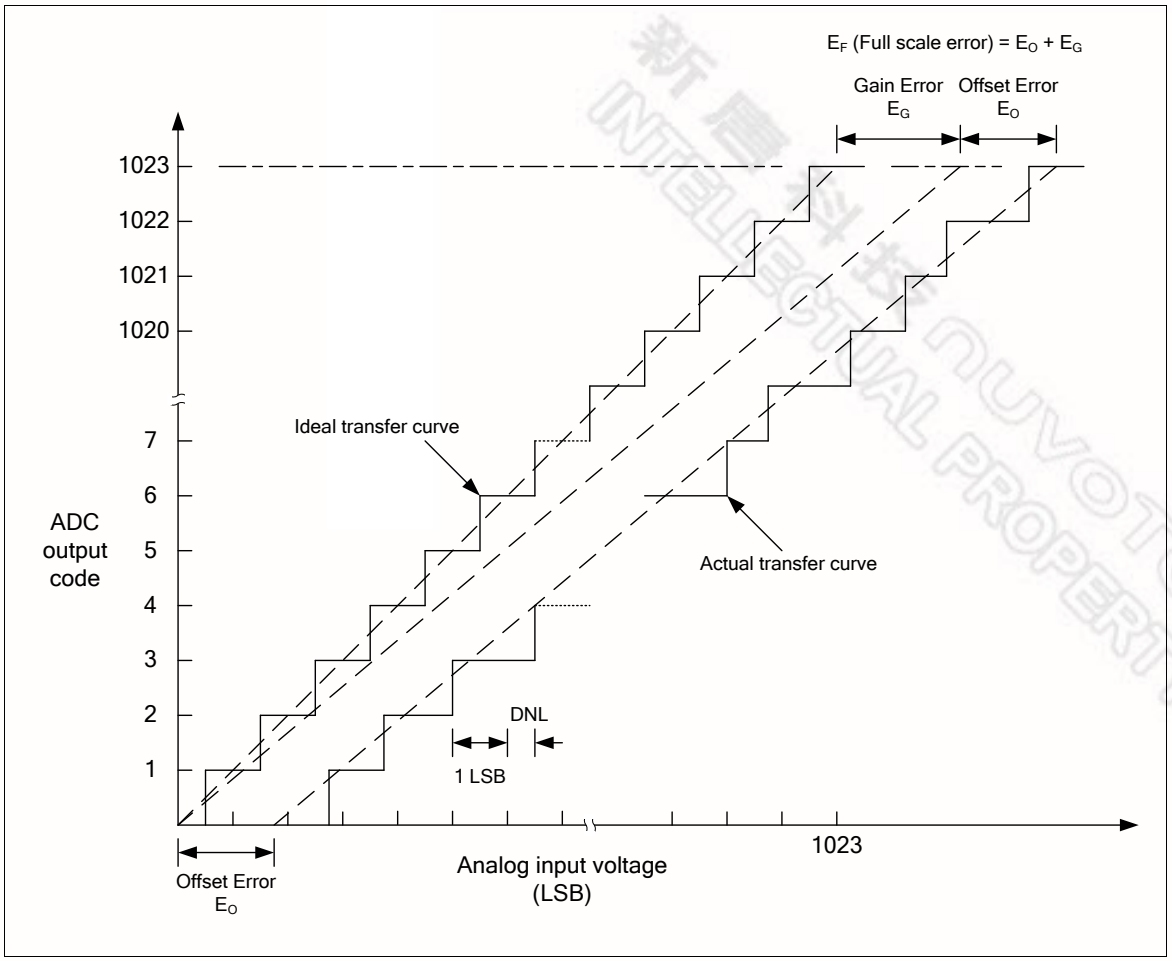


Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

9.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	2.5	-	mA	12 MHz, V_{DD} = 5.5V
		-	1.0	-	mA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-



9.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.5	-	5.5	V	-
V_{LDO}	Output Voltage	1.62	1.8	1.98	V	-
T_A	Temperature	-40	25	105	℃	

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

9.4.3 Low Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-

T_A	Temperature	-40	25	105	℃	-
I_{LVR}	Quiescent Current	-	1	5	μA	AV_{DD} =5.5V
V_{LVR}	Threshold Voltage	1.90	2.00	2.10	V	T_A=25℃
		1.70	1.90	2.05	V	T_A=-40℃
		2.00	2.20	2.45	V	T_A =105℃

9.4.4 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	-	140	μA	AV_{DD} =5.5V
V_{BOD}	Brown-out Detector (Falling edge)	4.2	4.38	4.55	V	BOD_VL [1:0]=11
		3.5	3.68	3.85	V	BOD_VL [1:0]=10
		2.5	2.68	2.85	V	BOD_VL [1:0]=01
		2.0	2.18	2.35	V	BOD_VL [1:0]=00
V_{BOD}	Brown-out Detector (Rising edge)	4.3	4.52	4.75	V	BOD_VL [1:0]=11
		3.5	3.8	4.05	V	BOD_VL [1:0]=10
		2.5	2.77	3.05	V	BOD_VL [1:0]=01
		2.0	2.25	2.55	V	BOD_VL [1:0]=00

9.4.5 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Reset Voltage	1.6	2	2.4	V	-
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	-	-	100	mV	
RR_{VDD}	V_{DD} Raising Rate to Ensure Power-on Reset	0.025	-	-	V/ms	
t_{POR}	Minimum Time for V_{DD} Stays at VPOR to Ensure Power-on Reset	0.5	-	-	ms	

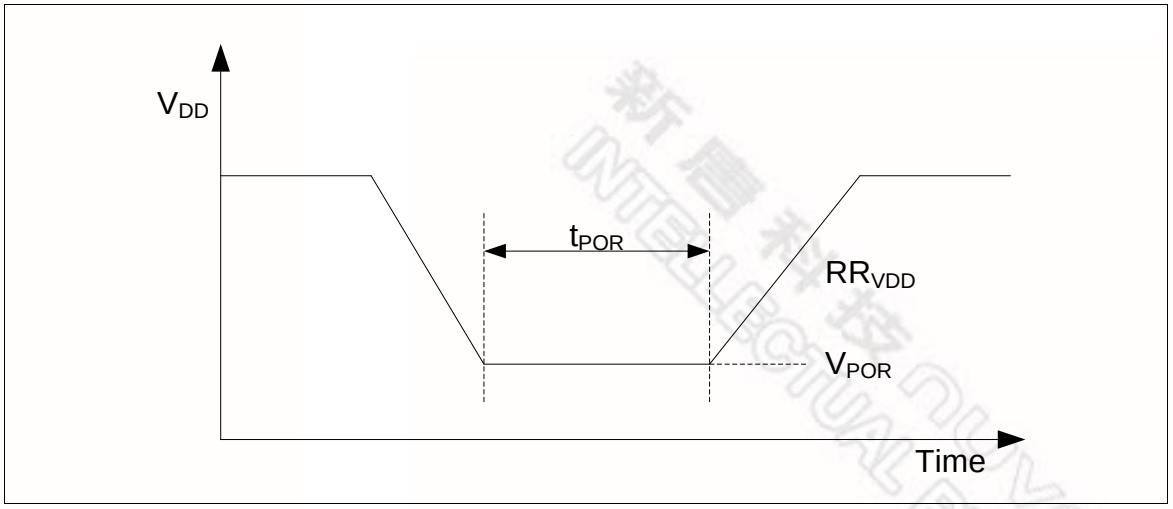


Figure 9-2Power-up Ramp Condition

9.4.6 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.5	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	40	80	μA	AV_{DD}=5V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	AV_{DD} -0.1	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD}– 0.1	V	-
-	DC Gain	40	70	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{COM}=1.2 V, V_{DIFF}=0.1 V
V_{HYS}	Hysteresis	-	±30	±60	mV	V_{COM}=1.2 V
T_{STB}	Stable time	-	-	1	μs	