Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	33-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini52zde

Table of Contents

LIST OF TABLES

- Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage level: 2.0V
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP (7x7), 33-pin QFN (5x5) , 33-pin QFN (4x4), 20-pin TSSOP

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer

Table 4.1-1 List of Abbreviations

4.2 NuMicro Mini51™ Series Product Selection Guide

Part No.	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP IAP	IRC 22.1184 MHz	Package
							UART	SPI	I²C						
MINI51FDE	4 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI51LDE	4 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI51ZDE	4 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI51TDE	4 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
MINI52FDE	8 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI52LDE	8 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI52ZDE	8 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI52TDE	8 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
MINI54FDE	16 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI54LDE	16 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI54ZDE	16 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI54TDE	16 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
*MINI54FHC	16 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	6	3x10-bit	v	v	TSSOP20

Table 4.2-1NuMicro Mini51™ Series Product Selection Guide

* Mini54FHC is a special part number, not pin to pin compatible to others Mini51series part number.

4.3.2 QFN 33-pin

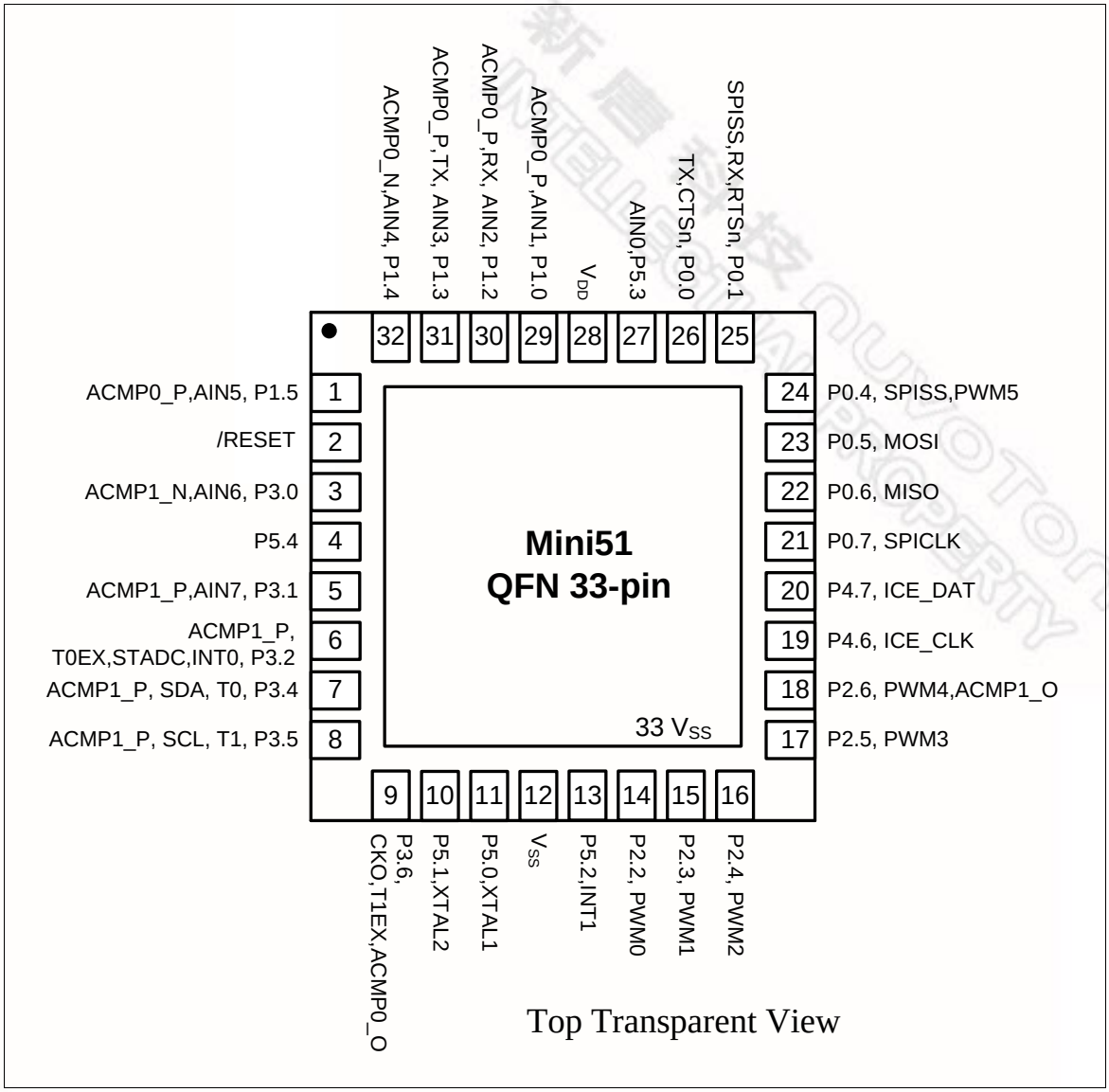


Figure 4.3-2 NuMicro Mini51™ Series QFN 33-pin Diagram

4.3.3 TSSOP 20-pin

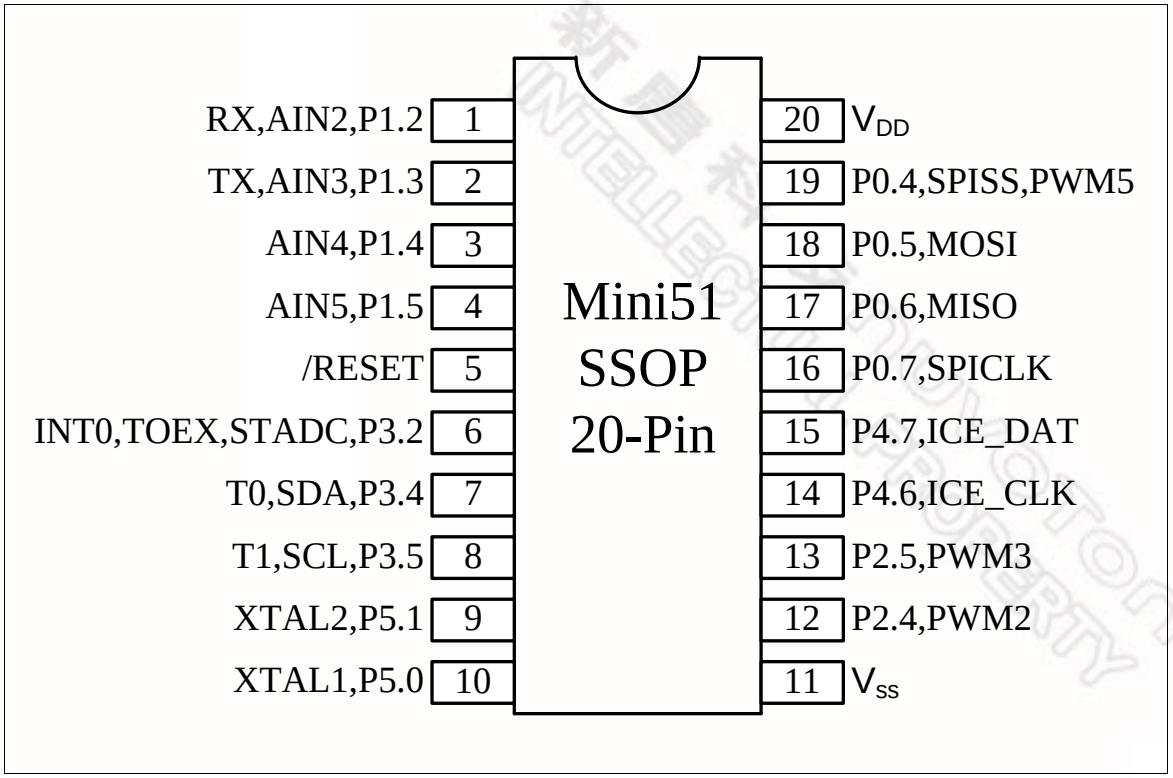


Figure 4.3-3 NuMicro Mini51™ Series TSSOP 20-pin Diagram

4.3.4 Mini54FHC (TSSOP20-pin)

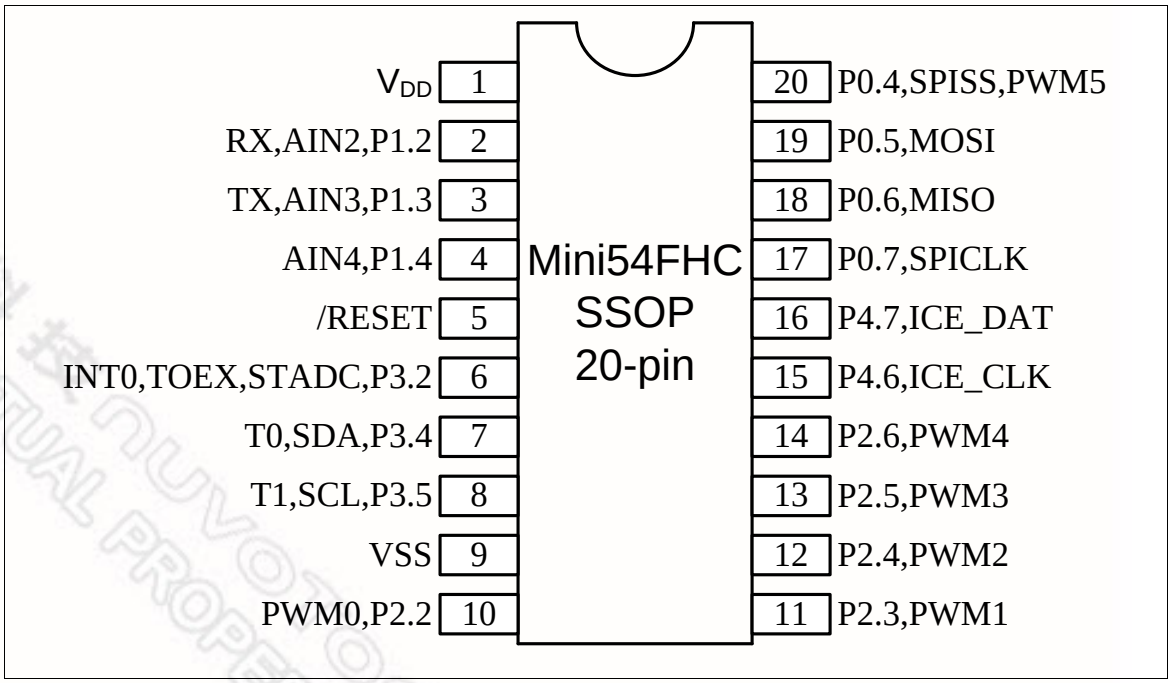


Figure 4.3-4 NuMicro Mini51™ Series TSSOP 20-pin Diagram

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
				RX	**I**	UART data receiver input pin.
				ACMP0_P	**AI**	Analog comparator positive input pin.
46	31	2	3	P1.3	**I/O**	General purpose digital I/O pin.
				AIN3	**AI**	ADC analog input pin.
				TX	**O**	UART transmitter output pin.
				ACMP0_P	**AI**	Analog comparator positive input pin.
47	32	3	4	P1.4	**I/O**	General purpose digital I/O pin.
				AIN4	**I/O**	PWM5: PWM output/Capture input.
				ACMP0_N	**AI**	Analog comparator negative input pin.
48	---	--	--	NC	**---**	Not connected.

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

6.3.4 Whole System Memory Mapping

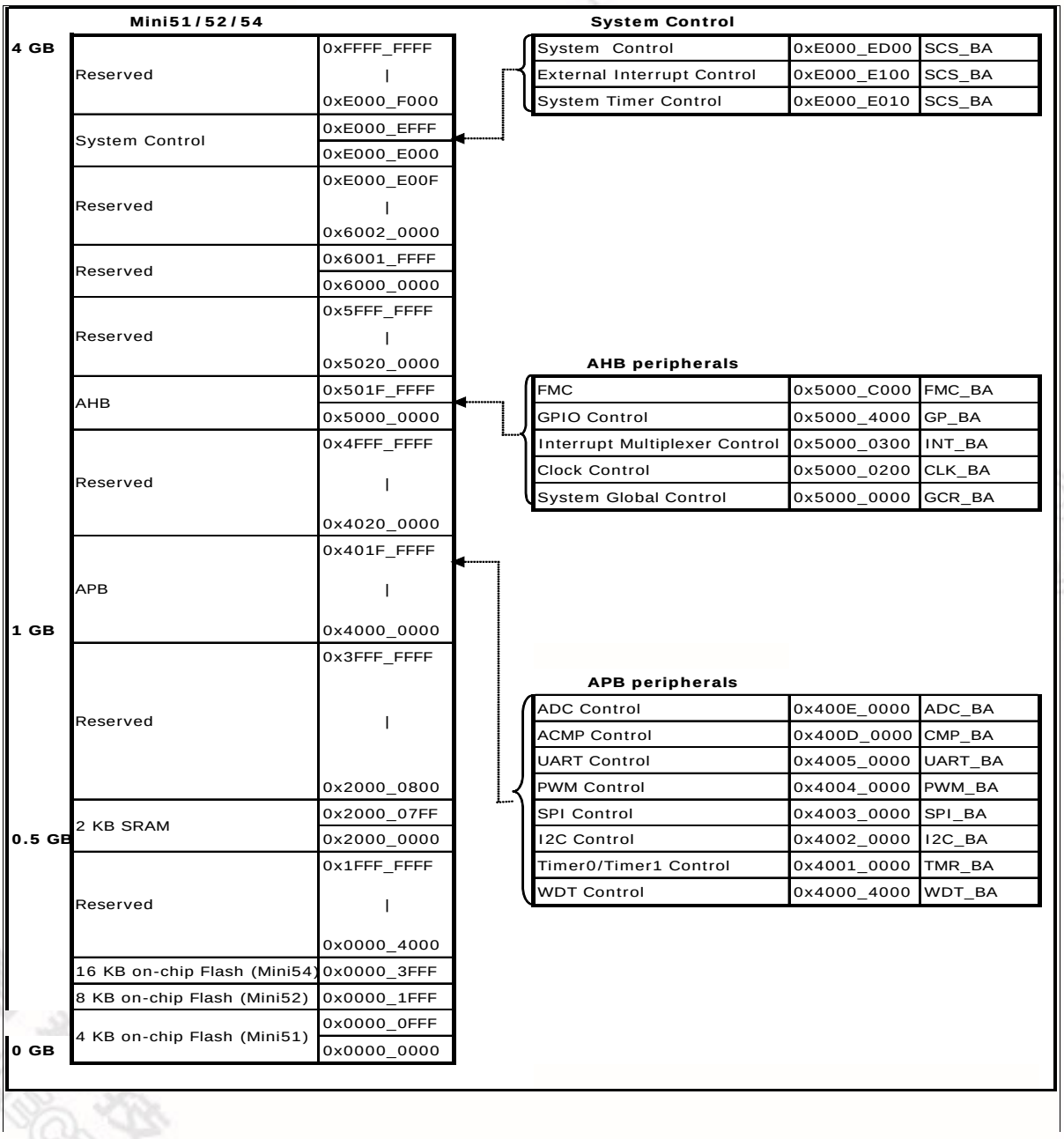


Table 6.3-1 Memory Mapping Table

6.4 Clock Controller

6.4.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex™-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 3 sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT) or 32.768 kHz (LXT) external low speed crystal oscillator
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

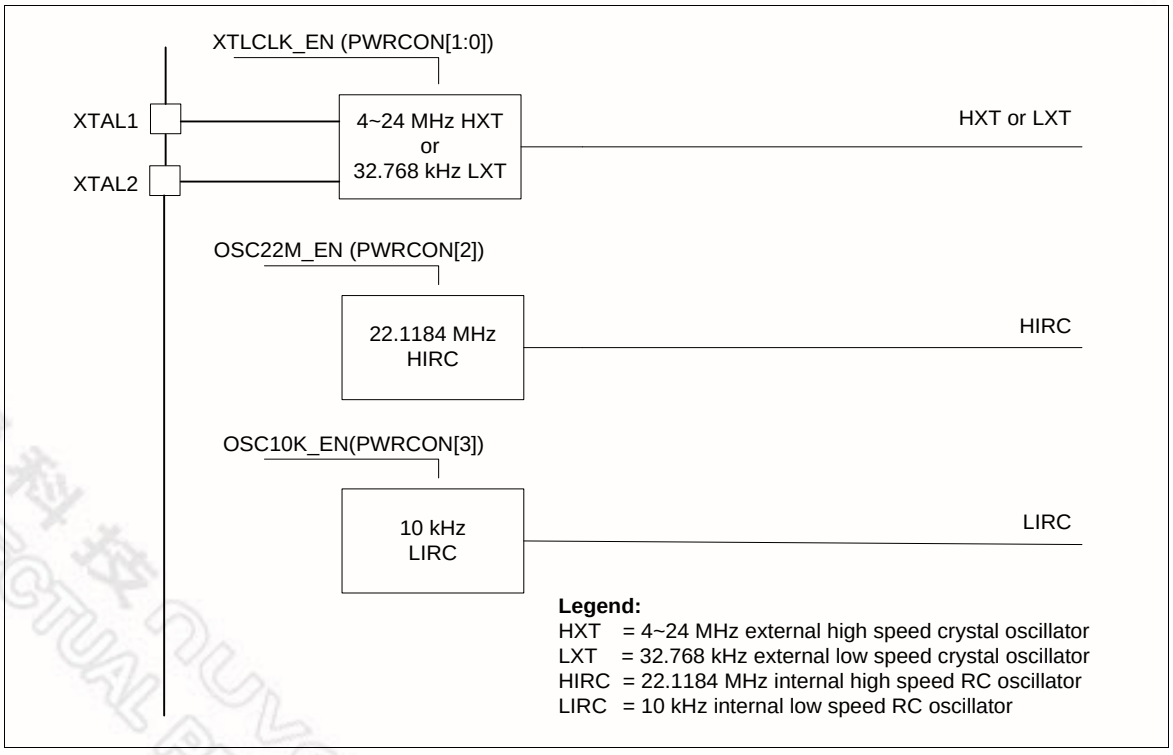


Figure 6.4-1 Clock Generator Block Diagram

6.7 Flash Memory Controller (FMC)

6.7.1 Overview

The NuMicro Mini51™ series is equipped with 4K/8K/16K bytes on chip embedded flash memory for application program (APROM) that can be updated through ISP procedure. In-System-Programming (ISP) and In-Application-Programming (IAP) enable user to update program memory when chip is soldered on PCB. After chip power on Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro Mini51™ series also provides Data Flash region that is shared with APROM and its start address is configurable and defined by user in CONFIG1.

6.7.2 Features

- Running up to 24 MHz with zero wait state for discontinuous address read access
- 4/8/16 Kbytes application program memory (APROM)
- 2 Kbytes in system programming (ISP) loader program memory (LDROM)
- Programmable data flash start address
- All embedded flash memory supports 512 bytes page erase
- In System Program (ISP)/In Application Program (IAP) to update on chip flash memory

7 ARM® CORTEX™-M0 CORE

7.1 Overview

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset and can be entered as a result of an exception return. The following figure shows the functional controller of the processor.

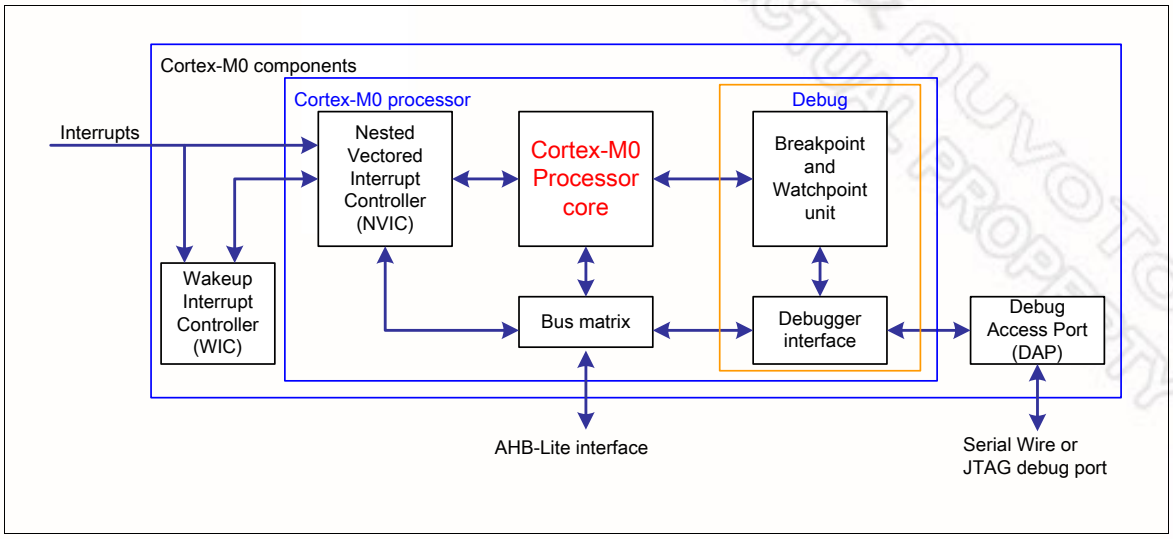


Figure 7.1-1 Functional Block Diagram

7.2 Features

- A low gate count processor
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model:

    This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power Idle mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Idle mode

- Debug support
  - Four hardware breakpoints
  - Two watch points
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

7.3 System Timer (SysTick)

The Cortex™-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer to count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

I_{SK13}	Drain and Push-pull Mode)	5	8	-	mA	V_{DD} = 2.5 V, V_S = 0.45 V

Notes:

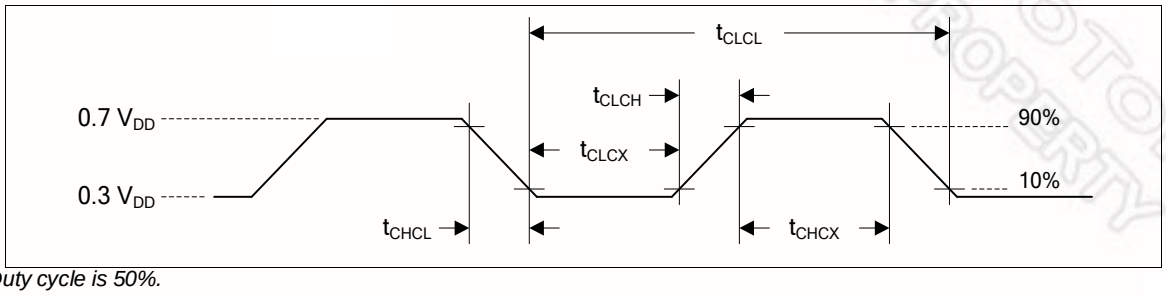
1. /RESET pin is a Schmitt trigger input.

2. XTAL1 is a CMOS input.

3. Pins of P0, P1, P2, P3, P4 and P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of VDD=5.5V, the transition current reaches its maximum value when VIN approximates to 2V.

9.3 AC Electrical Characteristics

9.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

9.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	2.5	-	mA	12 MHz, V_{DD} = 5.5V
		-	1.0	-	mA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

9.3.3 Typical Crystal Application Circuits

Crystal	C1	C2
4MHz ~ 24 MHz	10~20 pF	10~20 pF

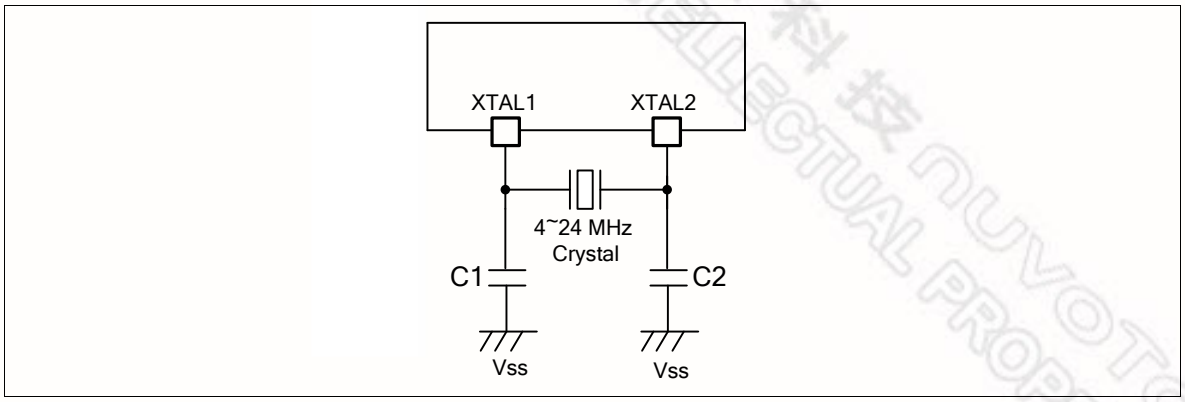
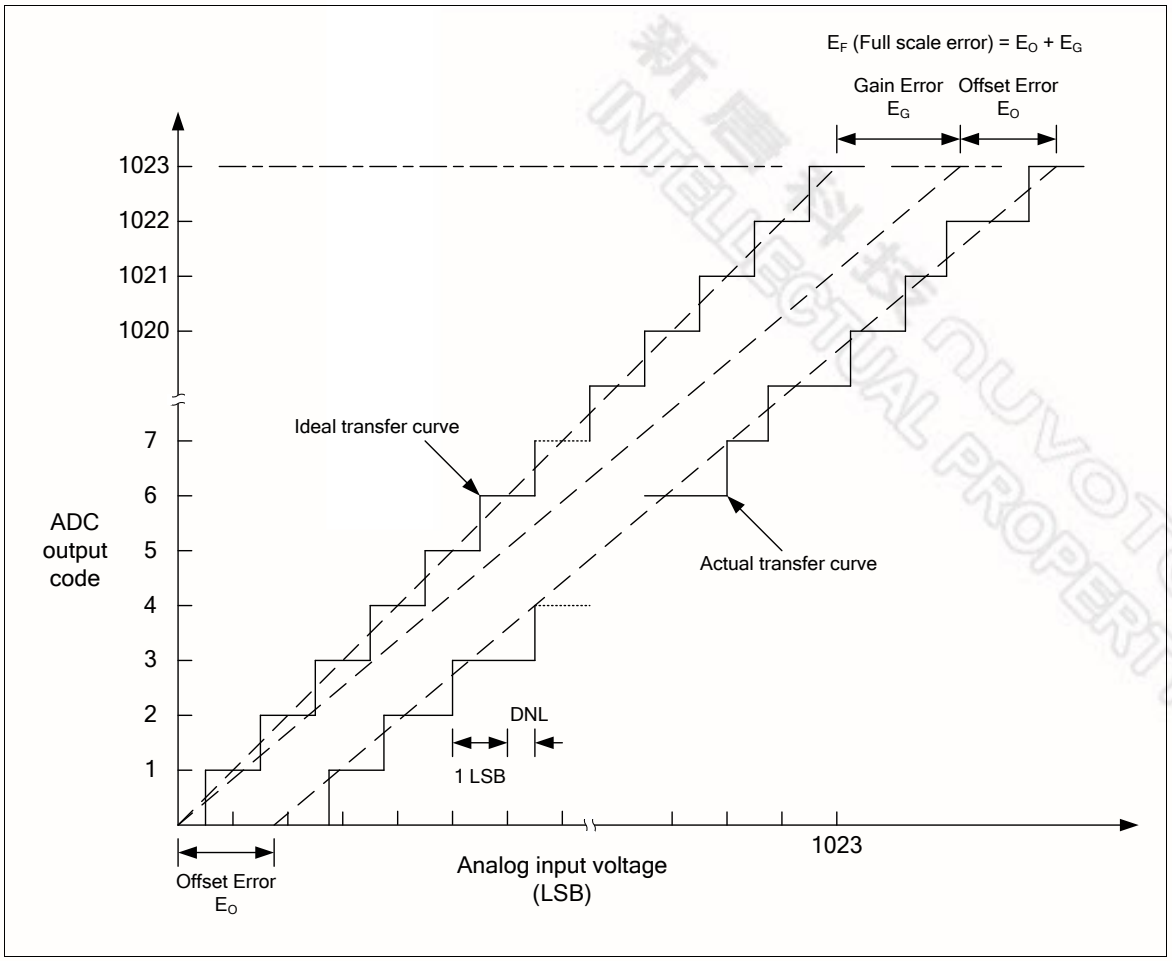


Figure 9-1Mini5xDE Typical Crystal Application Circuit

9.3.4 22.1184 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	22.1184		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5 V
		-2	-	+2	%	T_A = -40℃~105℃ V_{DD}=2.5 V~ 5.5 V
I_{HRC}	Operating Current	-	700	-	μA	T_A = 25 ℃,V_{DD} = 5 V



9.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.5	-	5.5	V	-
V_{LDO}	Output Voltage	1.62	1.8	1.98	V	-
T_A	Temperature	-40	25	105	℃	

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

9.4.3 Low Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-

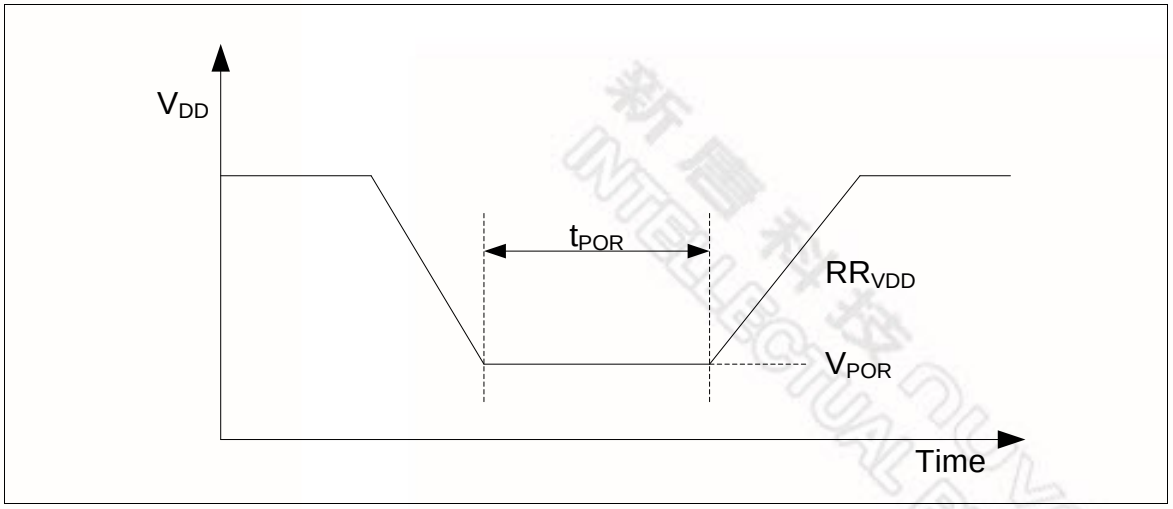


Figure 9-2Power-up Ramp Condition

9.4.6 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.5	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	40	80	μA	AV_{DD}=5V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	AV_{DD} -0.1	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD}– 0.1	V	-
-	DC Gain	40	70	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{COM}=1.2 V, V_{DIFF}=0.1 V
V_{HYS}	Hysteresis	-	±30	±60	mV	V_{COM}=1.2 V
T_{STB}	Stable time	-	-	1	μs	

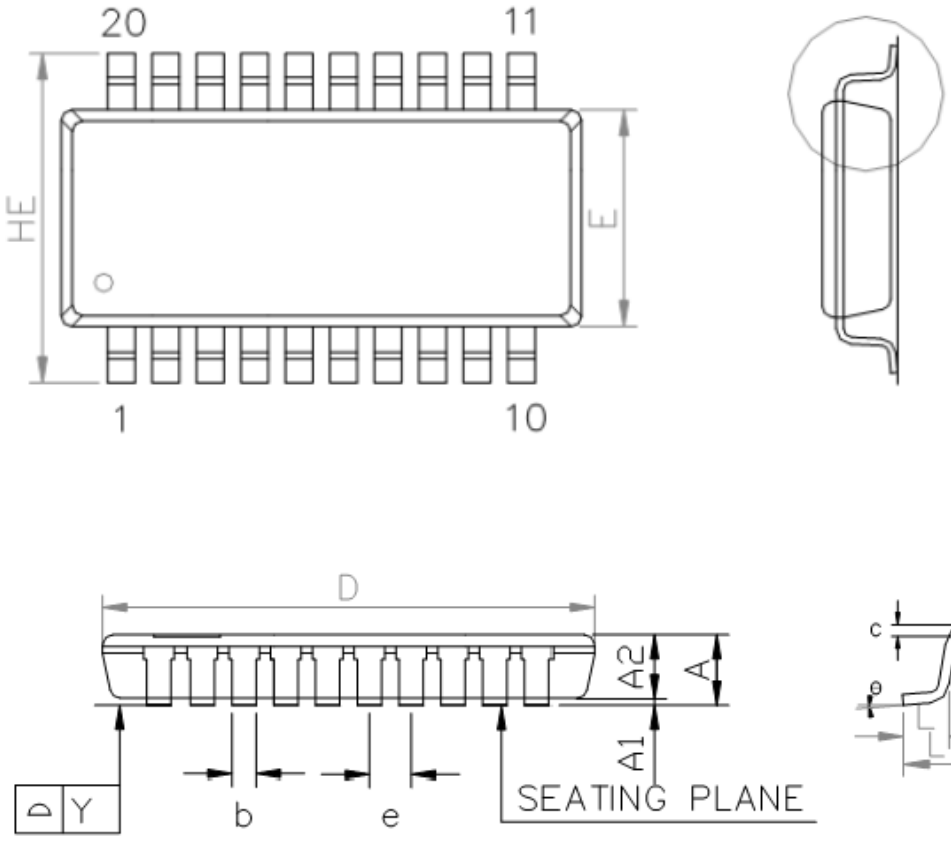
9.5 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.62	1.8	1.98	V	
N_{ENDUR}	Endurance	20,000	-	-	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A =85℃
T_{ERASE}	Page Erase Time	-	20	-	ms	
T_{PROG}	Program Time	-	60	-	us	
I_{DD1}	Read Current	-	6	-	mA	
I_{DD2}	Program Current	-	8	-	mA	
I_{DD3}	Erase Current	-	12	-	mA	

Notes:

1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
3. Guaranteed by design, not test in production.

10.4 20-pin TSSOP



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	—	0.30	0.007	—	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	—	0.20	0.004	—	0.008
θ	0°	—	8°	0°	—	8°
Y	0.10 BASIC			0.004 BASIC		