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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini54fde

LIST OF FIGURES

- Provides two channel 32-bit timers. One 8-bit pre-scale counter with 24-bit up counter for each timer
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous operation modes
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
- Provides event counter function
- Supports wake-up from Idle or Power-down mode

- WDT (Watchdog Timer)
  - Multiple clock sources
  - Supports wake-up from Idle or Power-down mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Independent 16-bit PWM duty control units with maximum six outputs
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake protections
  - Supports duty, period, and fault break interrupts
  - Supports duty/period trigger ADC conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period
  - Provides interrupt accumulation function
- UART (Universal Asynchronous Receiver/Transmitters)
  - One UART device
  - Buffered receiver and transmitter, each with 16-byte FIFO
  - Optional flow control function (CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports RS-485 function
- SPI (Serial Peripheral Interface)
  - One SPI devices
  - Supports Master/Slave mode

- Full-duplex synchronous serial data transfer
- Provides 3-wire function
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Rx latching data can be either at rising edge or at falling edge of serial clock
- Tx sending data can be either at rising edge or at falling edge of serial clock
- Supports Byte Suspend mode in 32-bit transmission
- 4-level depth FIFO buffer

- I^2C
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
  - Supports Power-down wake-up function
  - Support FIFO function
- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 300K SPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger, PWM trigger, or external pin trigger
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Build-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V

- Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage level: 2.0V
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP (7x7), 33-pin QFN (5x5) , 33-pin QFN (4x4), 20-pin TSSOP

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro Mini51™ Series Selection Code

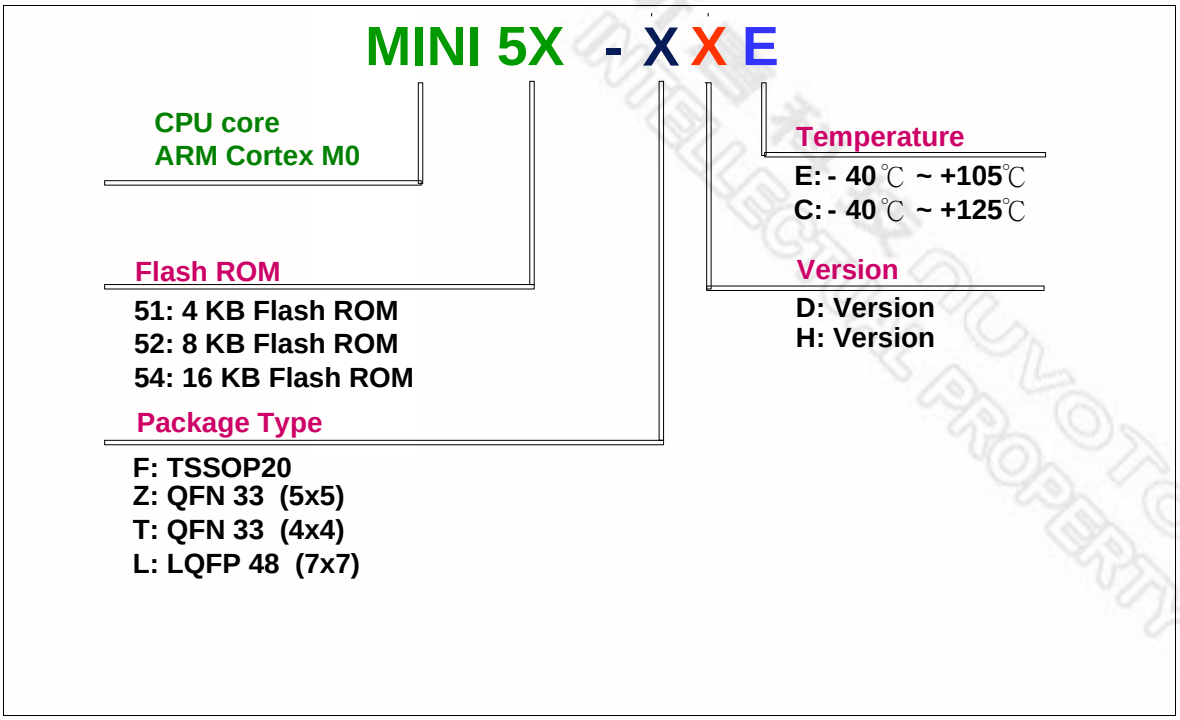


Figure 4.1-1 NuMicro Mini51™ Series Selection Code

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
29	13	-	-	-	
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	-	-	-	
32	16	**GP5_INT**	GPIO	External signal interrupt from GPIO group P5 except P5.2	Yes
33	17	**HIRC_TRIM_INT**	HIRC	HIRC trim interrupt	No
34	18	**I2C_INT**	I^2C	I^2C interrupt	Yes
35 ~ 40	19 ~ 24	-	-	-	
41	25	**ACMP_INT**	ACMP	Analog Comparator 0 or Comparator 1 interrupt	Yes
42 ~ 43	26 ~ 27	-	-	-	
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	-	-	-	

Table 6.2-2 System Interrupt Map Vector Table

6.2.4 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table based address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with the exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer Value
Exception Number * 0x04	Exception Entry Pointer using that Exception Number

Table 6.2-3 Vector Table Format

	Ext. CLK (HXT Or LXT)	HIRC	LIRC	PCLK
WDT	Yes	No	Yes	Yes
Timer0	Yes	Yes	Yes	Yes
Timer1	Yes	Yes	Yes	Yes
I²C	No	No	No	Yes
SPI	No	No	No	Yes
UART	Yes	Yes	No	No
PWM	No	No	No	Yes
ADC	Yes	Yes	No	Yes
ACMP	No	No	No	Yes

Table 6.4-1 Peripheral Clock Source Selection Table

6.4.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripheral clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator (LIRC) clock
- 32.768 kHz external low speed crystal oscillator (LXT) clock (If PD_32K = 1 and XTLCLK_EN[1:0] = 10)
- Peripherals Clock (When 10 kHz low speed oscillator is adopted as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

6.4.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\boldsymbol{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

if DIVIDER1(FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CKO pin directly.

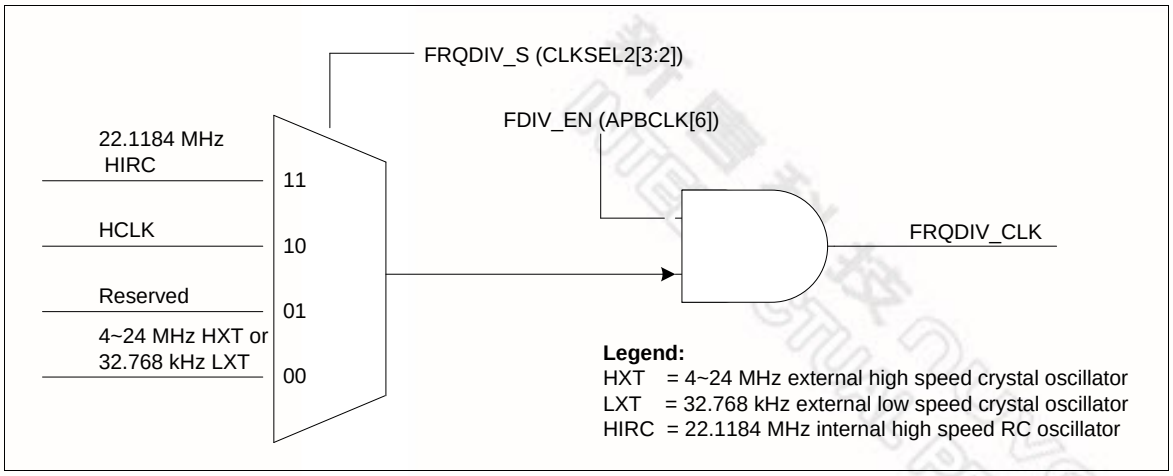


Figure 6.4-6 Clock Source of Frequency Divider

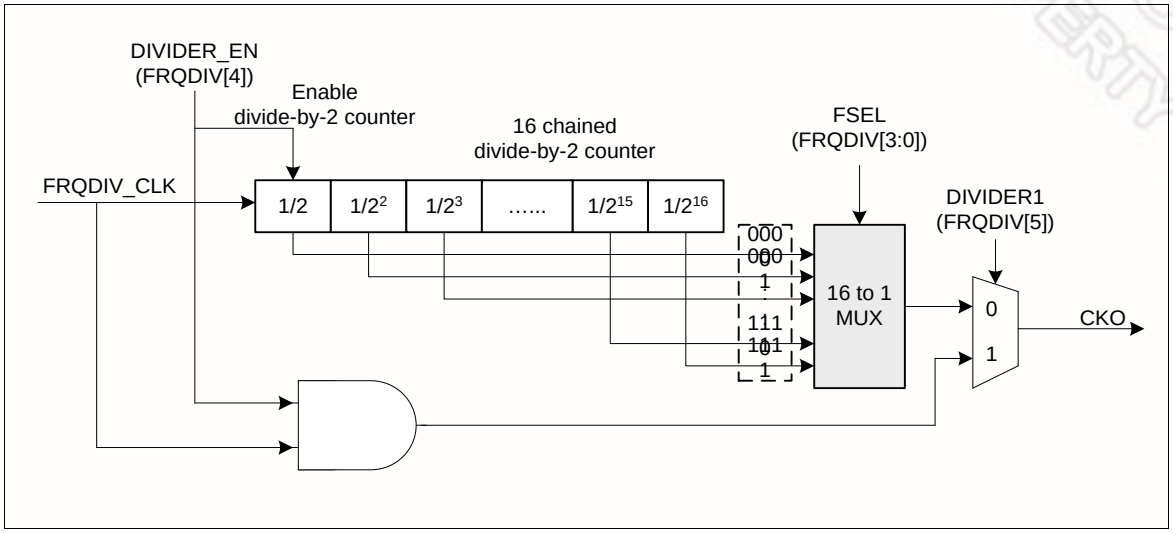


Figure 6.4-7 Block Diagram of Frequency Divider

6.5 Analog Comparator (ACMP)

6.5.1 Overview

The NuMicro Mini51™ Series contains two comparators which can be used in a number of different configurations. The comparator output is logic 1 when positive input greater than negative input, otherwise the output is 0. Each comparator can be configured to generate interrupt when the comparator output value changes.

6.5.2 Features

- Analog input voltage range: 0 ~ AV_{DD}
- Supports Hysteresis function
- Optional internal reference voltage source for each comparator negative input

6.6 Analog-to-Digital Converter (ADC)

6.6.1 Overview

The NuMicro Mini51™ series contains one 10-bit successive approximation analog-to-digital converters (SAR A/D converter) with eight input channels. The A/D converters can be started by software, external pin (STADC/P3.2) or PWM trigger.

6.6.2 Features

- Analog input voltage range: 0 ~ Analog Supply Voltage from AV_{DD}
- 10-bit resolution and 8-bit accuracy is guaranteed
- Up to eight single-end analog input channels
- 300 KSPS (AV_{DD} 4.5V - 5.5V) and 200 KSPS (AV_{DD} 2.5V - 5.5V) conversion rate
- An A/D conversion is performed one time on a specified channel
- An A/D conversion can be started by:
  - Software write 1 to ADST bit
  - External pin STADC
  - PWM trigger with optional start delay period
- Each conversion result is held in data register with valid and overrun indicators
- Conversion results can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 2 input sources: External analog voltage and internal fixed band-gap voltage

6.8 General Purpose I/O (GPIO)

6.8.1 Overview

The NuMicro Mini51™ series have up to 30 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 30 pins are arranged in 6 ports named as P0, P1, P2, P3, P4 and P5. Each of the 30 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each pin can be configured by software individually as Input, Push-pull output, Open-drain output, or Quasi-bidirectional mode. For Quasi-bidirectional mode, each I/O pin is equipped with a very weak individual pull-up resistor about 110 kΩ ~ 300 kΩ for V_{DD} is from 5.0 V to 2.5 V.

6.8.2 Features

- Four I/O modes:
  - Input-only with high impendence
  - Push-pull output
  - Open-drain output
  - Quasi-bidirectional
- TTL/Schmitt trigger input mode selected by Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function
- High driver and high sink I/O mode support
- Configurable default I/O mode of all pins after reset by CIOINI (Config0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in Input tri-state mode after chip reset (default)

6.9 I2C Serial Interface Controller (I2C)

6.9.1 Overview

I^2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I^2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. The I^2C also supports Power-down wake up function.

6.9.2 Features

The I^2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus include:

- Master/Slave mode
- Bi-directional data transfer between masters and slaves
- Multi-master bus
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter that requests the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
- External pull-up needed for higher output pull-up speed
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address registers with mask option)
- Supports Power-down wake-up function
- Support FIFO function

6.11 Serial Peripheral Interface (SPI)

6.11.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. The SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. SPI controller can be configured as a master or a slave device.

6.11.2 Features

- Supports Master or Slave mode operation
- Configurable transfer bit length
- Provides four 32-bit FIFO buffers
- Supports MSB first or LSB first transfer
- Supports byte reorder function
- Supports byte or word suspend mode
- Supports Slave 3-wire mode

6.13 UART Controller (UART)

6.13.1 Overview

The NuMicro Mini51™ series provides one channel of Universal Asynchronous Receiver/Transmitters (UART). UART Controller performs Normal Speed UART, and supports flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, and RS-485 function mode.

6.13.2 Features

- Full duplex, asynchronous communications
- Separates 16-byte receive and transmitted FIFO for data payloads
- Supports hardware auto flow control, flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY(UA_TOR[15:8]) register
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit
  - Programmable stop bit, 1, 1.5, or 2 stop bit
- Supports IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enable to program RTS pin to control RS-485 transmission direction directly

I_{DD16}		-	1.4	-	mA	V_{DD} 3.3 V HXT 4 MHz HIRC Disabled All digital modules Disabled
I_{DD17}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	225	-	μA	V_{DD} 5.5 V HXT Disabled HIRC □isabled LIRC Enabled All digital modules Enabled Only enable modules which support 10 kHz LIRC clock source
I_{DD18}		-	225	-	μA	V_{DD} 5.5 V HXT Disabled HIRC Disabled LIRC Enabled All digital modules Disabled
I_{DD19}		-	200	-	μA	V_{DD} 3.3 V HXT Disa□led HIRC Disabled LIRC Enabled All digital modules Enabled Only enable modules which support 10 kHz LIRC clock source
I_{DD20}		-	200	-	μA	V_{DD} 3.3 V HXT Disabled HIRC Disabled LIRC Enabled All digital modules Disa□led
I_{IDLE1}	Operating Current Idle Mode HCLK = 24MHz	-	7.1	-	mA	V_{DD} 5.5V HXT 24 MHz HIRC Disable All digital modules Enabled

I_{TL}	Logic 1 to 0 Transition Current P0/1/2/3/4/5 (Quasi-bidirectional Mode) [*3]	-	-690	-750	µA	V_{DD} = 5.5 V, V_{IN} = 2.0V
I_{LK}	Input Leakage Current P0/1/2/3/4/5	-1	-	+1	µA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage P0/1/2/3/4/5 (TTL Input)	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
V_{IH1}	Input High Voltage P0/1/2/3/4/5 (TTL Input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{IL3}	Input Low Voltage XTAL1[*2]	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 2.5 V
V_{IH3}	Input High Voltage XTAL1[*2]	3.5	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{ILS}	Negative-going Threshold (Schmitt Input), /RESET	-0.3	-	0.2V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), /RESET	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
R_{RST}	Internal /RESETPin Pull-up Resistor	40		150	kΩ	V_{DD} = 2.5 V ~ 5.5V
V_{ILS}	Negative-going Threshold (Schmitt input), P0/1/2/3/4/5	-0.3	-	0.3V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt input), P0/1/2/3/4/5	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
I_{SR11}	Source Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-300	-400	-	µA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR12}		-50	-80	-	µA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR13}		-40	-73	-	µA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SR21}	Source Current P0/1/2/3/4/5 (Push-pull Mode)	-20	-26	-	mA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR22}		-3	-5	-	mA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR23}		-2.5	-5	-	mA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SK11}	Sink Current P0/1/2/3/4/5 (Quasi-bidirectional, Open-	10	15	-	mA	V_{DD} = 4.5 V, V_S = 0.45 V
I_{SK12}		6	9	-	mA	V_{DD} = 2.7 V, V_S = 0.45 V

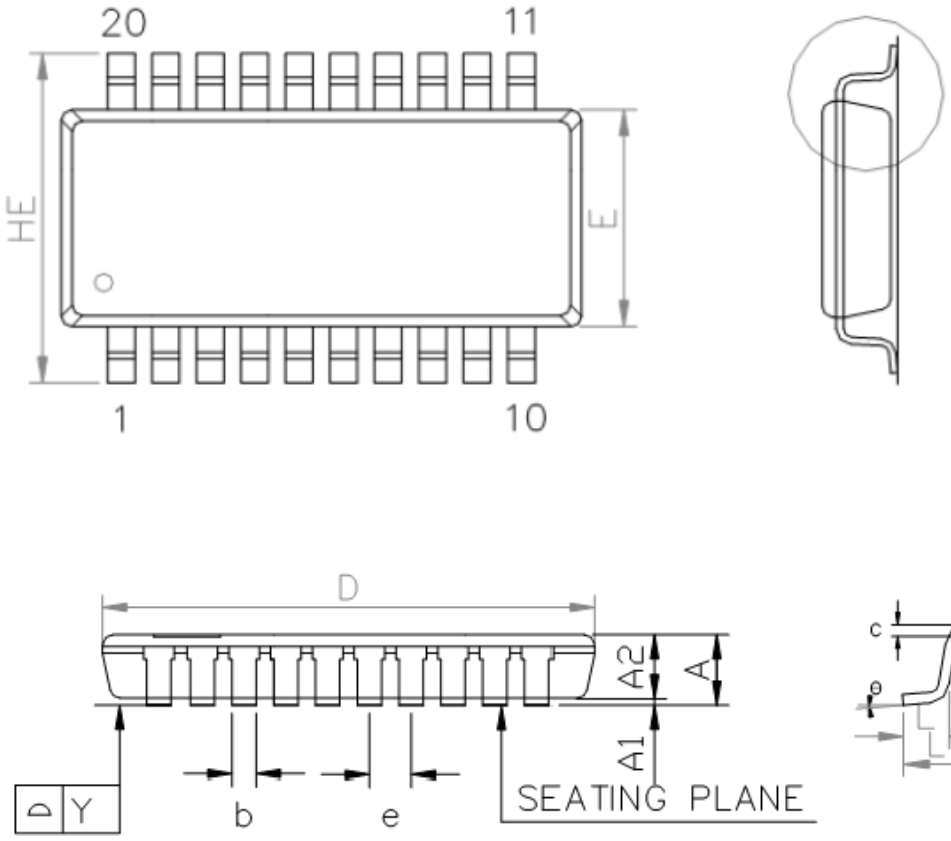
9.4 Analog Characteristics

9.4.1 10-bit SARADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	10	Bit	-
DNL	Differential Nonlinearity Error	-	-1~1.5	-1~+2.5	LSB	-
INL	Integral Nonlinearity Error	-	±1	±2	LSB	-
E_O	Offset Error	-	1	2	LSB	-
E_G	Gain Error (Transfer Gain)	-	-1	-3	LSB	-
E_A	Absolute Error	-	3	4	LSB	-
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency	-	-	4.2	MHz	AV_{DD} = 4.5~5.5 V
		-	-	2.8		AV_{DD} =2.5~5.5 V
F_S	Sample Rate (F_{ADC}/T_{CONV})	-	-	300	kSPS	AV_{DD} = 4.5~5.5 V
		-	-	200	kSPS	AV_{DD} = 2.5~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	N is sampling counter, N=0,1,2, 4,8, 16,32, 4, 128, 256,1024
T_{CONV}	Total Conversion Time	N+14			$1/F_{ADC}$	
AV_{DD}	Supply Voltage	2.5	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	600	-	μA	AV_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	3.2	-	pF	-
R_{IN}	Input Load	-	6	-	kΩ	-

Note: ADC voltage reference is same with AV_{DD}

10.4 20-pin TSSOP



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	—	0.30	0.007	—	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	—	0.20	0.004	—	0.008
θ	0°	—	8°	0°	—	8°
Y	0.10 BASIC			0.004 BASIC		

11 REVISION HISTORY

Revision	Date	Description
1.00	Oct. 18, 2013	Preliminary version
1.01	May 20, 2014	Supported the Mini54FHC for NuMicro Mini51 series.