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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini54lde



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- Provides two channel 32-bit timers. One 8-bit pre-scale counter with 24-bit up counter for each timer
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous operation modes
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
- Provides event counter function
- Supports wake-up from Idle or Power-down mode
- WDT (Watchdog Timer)
 - Multiple clock sources
 - Supports wake-up from Idle or Power-down mode
 - Interrupt or reset selectable on watchdog time-out
- PWM
 - Independent 16-bit PWM duty control units with maximum six outputs
 - Supports group/synchronous/independent/ complementary modes
 - Supports One-shot or Auto-reload mode
 - Supports Edge-aligned and Center-aligned type
 - Programmable dead-zone insertion between complementary channels
 - Each output has independent polarity setting control
 - Hardware fault brake protections
 - Supports duty, period, and fault break interrupts
 - Supports duty/period trigger ADC conversion
 - Timer comparing matching event trigger PWM to do phase change
 - Supports comparator event trigger PWM to force PWM output low for current period
 - Provides interrupt accumulation function
- UART (Universal Asynchronous Receiver/Transmitters)
 - One UART device
 - Buffered receiver and transmitter, each with 16-byte FIFO
 - Optional flow control function (CTS_n and RTS_n)
 - Supports IrDA (SIR) function
 - Programmable baud-rate generator up to 1/16 system clock
 - Supports RS-485 function
- SPI (Serial Peripheral Interface)
 - One SPI devices
 - Supports Master/Slave mode

- Full-duplex synchronous serial data transfer
- Provides 3-wire function
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Rx latching data can be either at rising edge or at falling edge of serial clock
- Tx sending data can be either at rising edge or at falling edge of serial clock
- Supports Byte Suspend mode in 32-bit transmission
- 4-level depth FIFO buffer
- I²C
 - Supports Master/Slave mode
 - Bidirectional data transfer between masters and slaves
 - Multi-master bus (no central master)
 - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
 - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
 - Programmable clocks allow for versatile rate control
 - Supports 7-bit addressing mode
 - Supports multiple address recognition (four slave addresses with mask option)
 - Supports Power-down wake-up function
 - Support FIFO function
- ADC (Analog-to-Digital Converter)
 - 10-bit SAR ADC with 300K SPS
 - Up to 8-ch single-end input and one internal input from band-gap
 - Conversion started either by software trigger, PWM trigger, or external pin trigger
 - Supports conversion value monitoring (or comparison) for threshold voltage detection
- Analog Comparator
 - Two analog comparators with programmable 16-level internal voltage reference
 - Build-in CRV (comparator reference voltage)
 - Supports Hysteresis function
 - Interrupt when compared results changed
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
 - With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V

- Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
 - Threshold voltage level: 2.0V
- Operating Temperature: -40°C~105°C
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
 - Green package (RoHS)
 - 48-pin LQFP (7x7), 33-pin QFN (5x5) , 33-pin QFN (4x4), 20-pin TSSOP

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer

Table 4.1-1 List of Abbreviations



5 BLOCK DIAGRAM

5.1 NuMicro Mini51™ Block Diagram

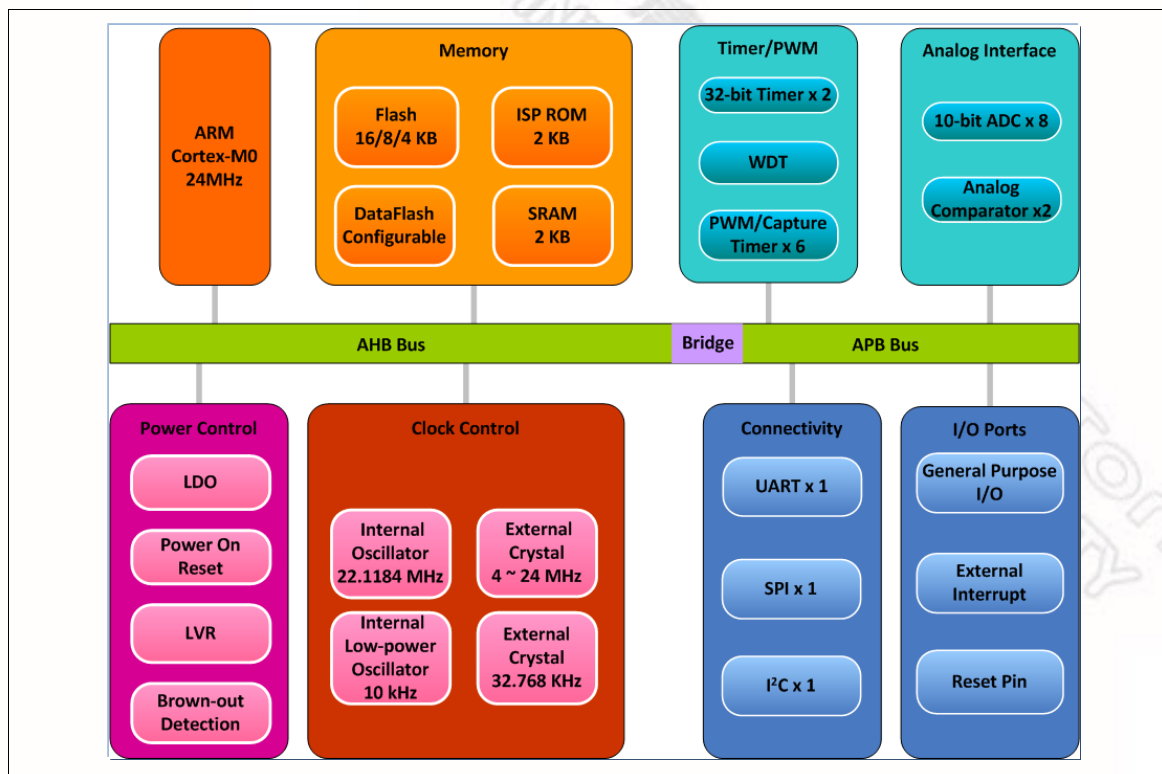


Figure 5.1-1 NuMicro Mini51™ Series Block Diagram



6.2.5 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending; however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 System Manager

6.3.1 Overview

System management includes the following sections:

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.3.2 System Reset

The system reset can be included by one of the following listed events. For these reset events flags can be read by RSTSRC register.

- Power-On Reset (POR)
- Low level on the Reset Pin (/RESET)
- Watchdog Timer Time-out Reset (WDT)
- Brown-out Detector Reset (BOD)
- Cortex™-M0 MCU Reset
- CPU Reset

6.3.3 System Power Architecture

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. AV_{DD} must be equal to V_{DD} to avoid leakage current.
- Digital power from V_{DD} and V_{SS} supplies power to the I/O pins and internal regulator which provides a fixed 1.8V power for digital operation.
- Build-in a capacitor for internal voltage regulator

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level as the digital power (V_{DD}). The following figure shows the power distribution of the Mini51™DE series.

6.4 Clock Controller

6.4.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex™-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 3 sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT) or 32.768 kHz (LXT) external low speed crystal oscillator
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

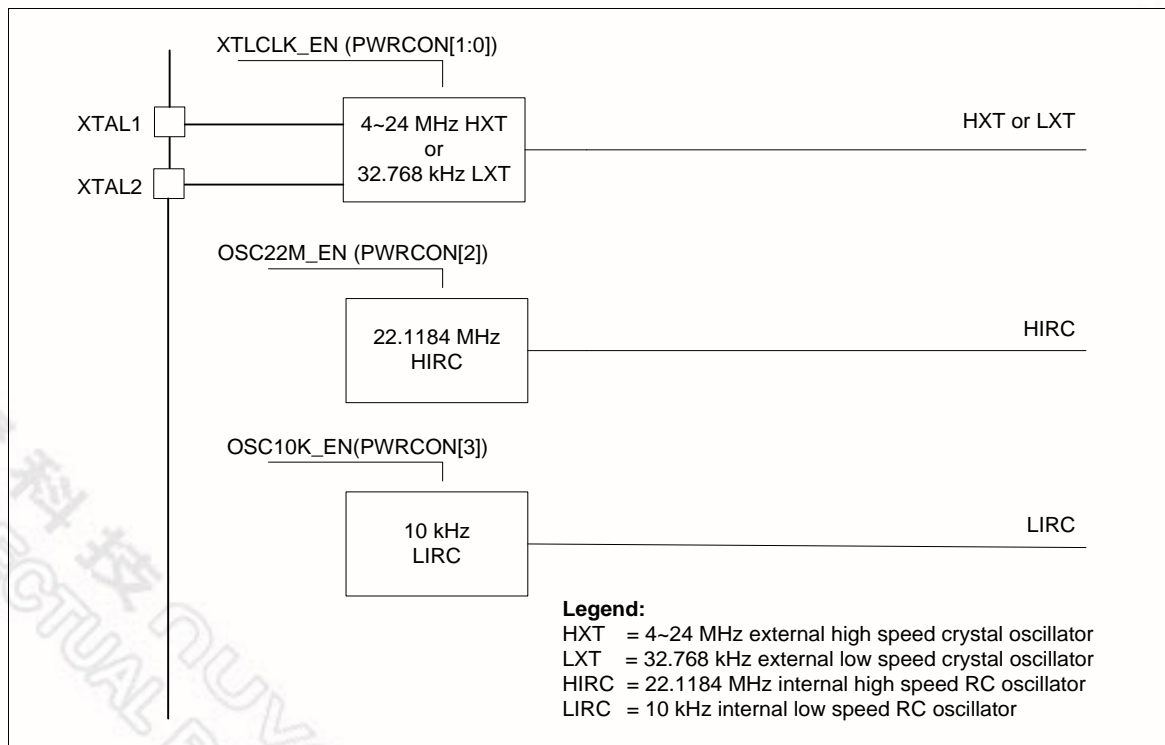


Figure 6.4-1 Clock Generator Block Diagram



6.4.2 System Clock and SysTick Clock

The system clock has three clock sources which are generated from clock generator block. The clock source switches depending on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown below.

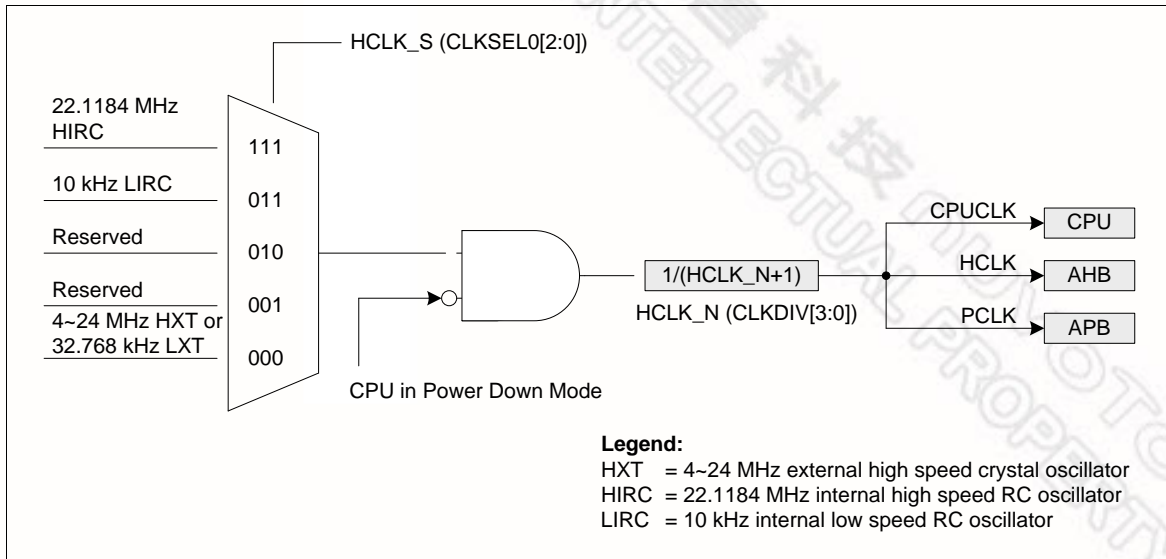


Figure 6.4-2 System Clock Block Diagram

The clock source of SysTick in Cortex™-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switches depending on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown below.

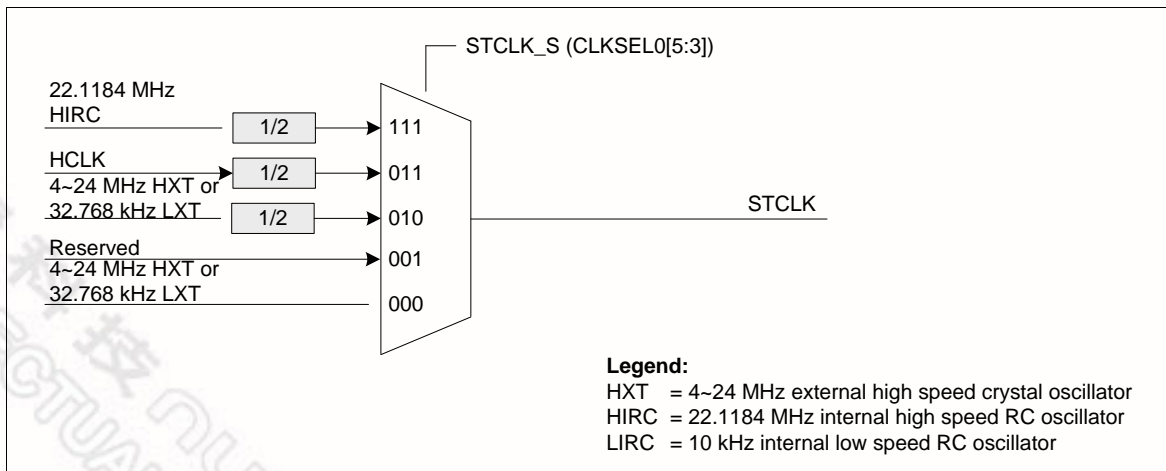


Figure 6.4-3 SysTick Clock Control Block Diagram



6.4.3 ISP Clock Source Selection

The clock source of ISP is from AHB clock (HCLK). Please refer to the register AHBCLK.

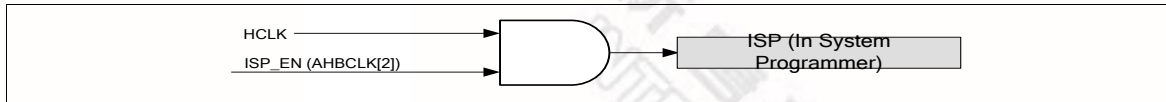


Figure 6.4-4 AHB Clock Source for HCLK

6.4.4 Module Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals. Please refer to the CLKSEL1 and APBCLK register description in section **Error! Reference source not found.**

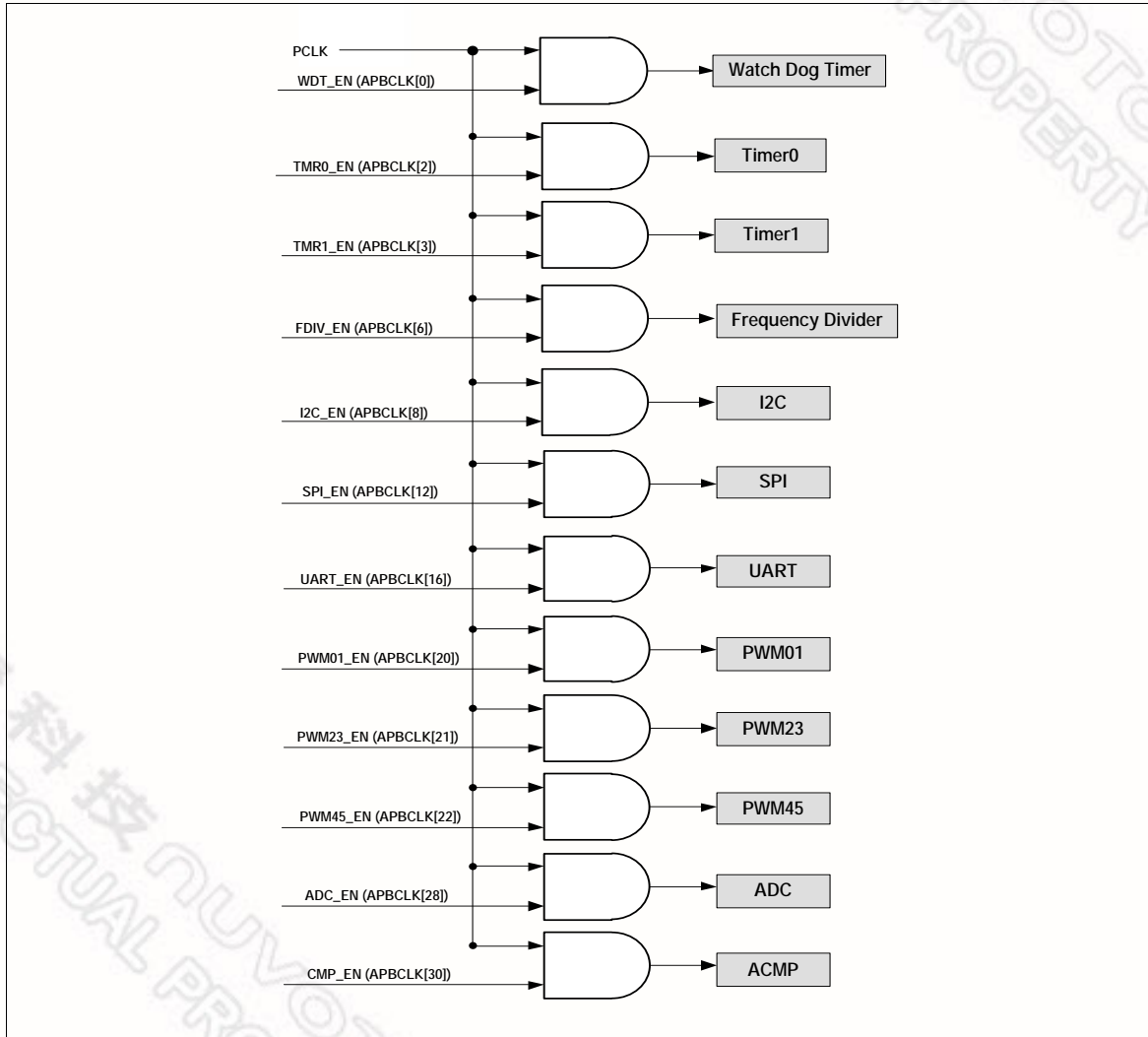


Figure 6.4-5 Peripherals Clock Source Selection for PCLK

6.9 I2C Serial Interface Controller (I2C)

6.9.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. The I²C also supports Power-down wake up function.

6.9.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus include:

- Master/Slave mode
- Bi-directional data transfer between masters and slaves
- Multi-master bus
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter that requests the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
- External pull-up needed for higher output pull-up speed
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address registers with mask option)
- Supports Power-down wake-up function
- Support FIFO function



6.12 Timer Controller (TMR)

6.12.1 Overview

The Timer Controller includes two 32-bit timers, TIMER0 ~ TIMER1, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.12.2 Features

- Two sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each channel (TMR0_CLK, TMR1_CLK)
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = $(1 / T \text{ MHz}) * (2^8) * (2^{24})$; T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external pin (T0, T1)
- 24-bit capture value is readable through TCAP (Timer Capture Data Register)
- Supports external capture pin (T0EX, T1EX) for interval measurement
- Supports internal signal (CPO0, CPO1) for interval measurement
- Supports external capture pin (T0EX, T1EX) to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

6.13 UART Controller (UART)

6.13.1 Overview

The NuMicro Mini51™ series provides one channel of Universal Asynchronous Receiver/Transmitters (UART). UART Controller performs Normal Speed UART, and supports flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, and RS-485 function mode.

6.13.2 Features

- Full duplex, asynchronous communications
- Separates 16-byte receive and transmitted FIFO for data payloads
- Supports hardware auto flow control, flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY(UA_TOR[15:8]) register
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
 - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
 - Programmable parity bit, even, odd, no parity or stick parity bit
 - Programmable stop bit, 1, 1.5, or 2 stop bit
- Supports IrDA SIR function mode
 - Supports 3/16-bit duration for normal mode
- Supports RS-485 function mode
 - Supports RS-485 9-bit mode
 - Supports hardware or software enable to program RTS pin to control RS-485 transmission direction directly

7 ARM® CORTEX™-M0 CORE

7.1 Overview

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset and can be entered as a result of an exception return. The following figure shows the functional controller of the processor.

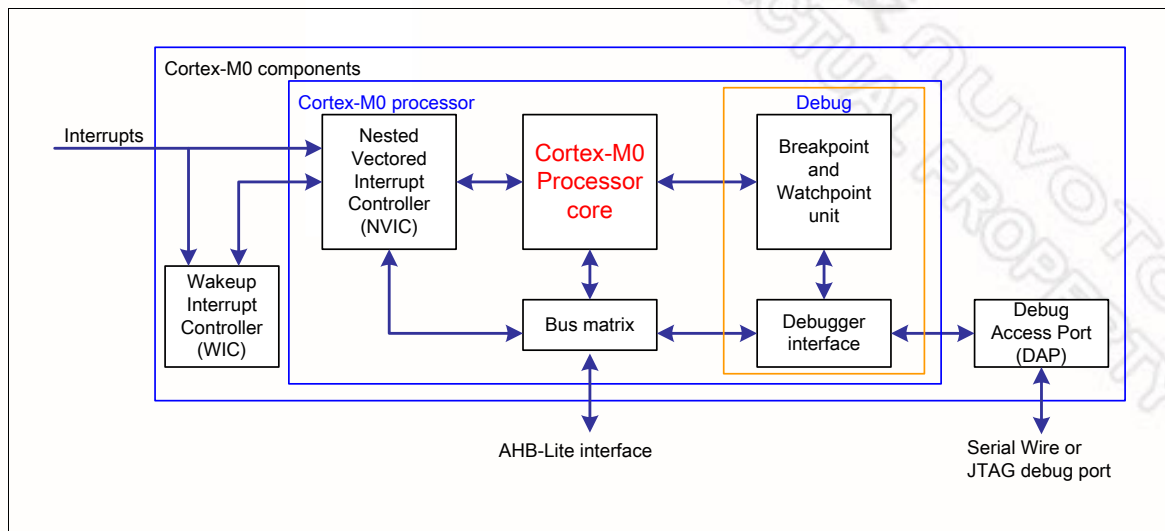


Figure 7.1-1 Functional Block Diagram

7.2 Features

- A low gate count processor
 - ARMv6-M Thumb® instruction set
 - Thumb-2 technology
 - ARMv6-M compliant 24-bit SysTick timer
 - A 32-bit hardware multiplier
 - System interface supported with little-endian data accesses
 - Ability to have deterministic, fixed-latency, interrupt handling
 - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
 - C Application Binary Interface compliant exception model:

This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
 - Low power Idle mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Idle mode
- Debug support
 - Four hardware breakpoints
 - Two watch points
 - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
 - Single step and vector catch capabilities
- Bus interfaces
 - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
 - Single 32-bit slave port that supports the DAP (Debug Access Port)

7.3 System Timer (SysTick)

The Cortex™-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

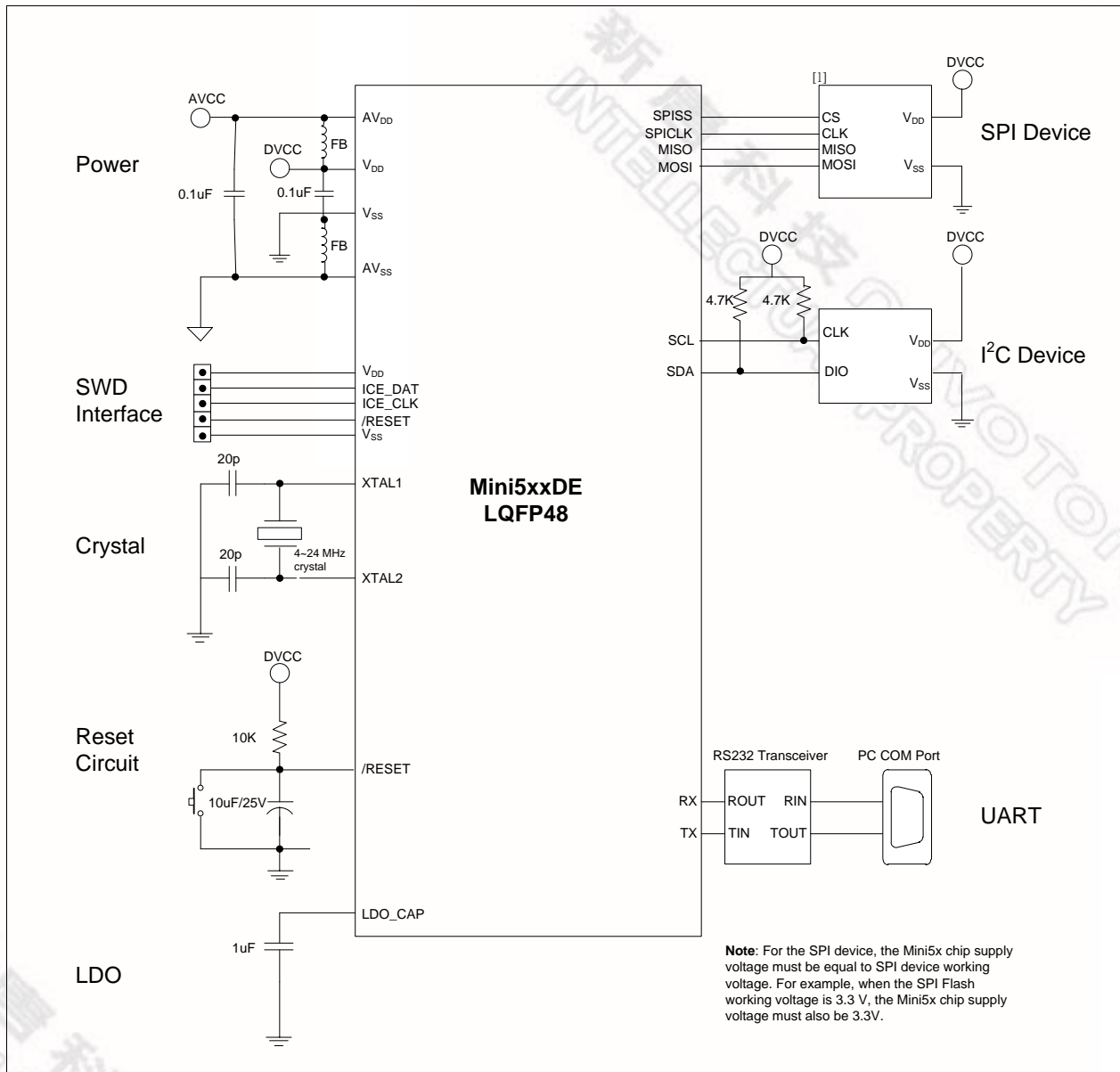
The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer to count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.



8 APPLICATION CIRCUIT



9.3.3 Typical Crystal Application Circuits

Crystal	C1	C2
4MHz ~ 24 MHz	10~20 pF	10~20 pF

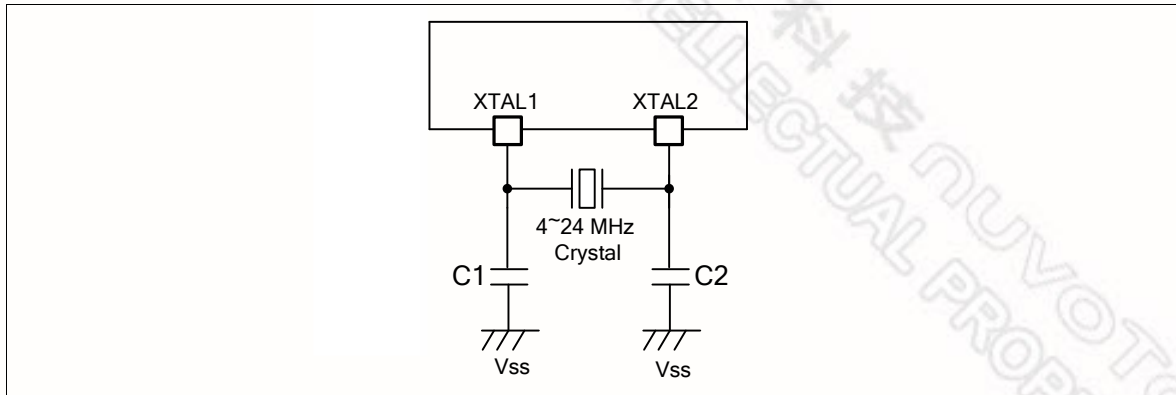
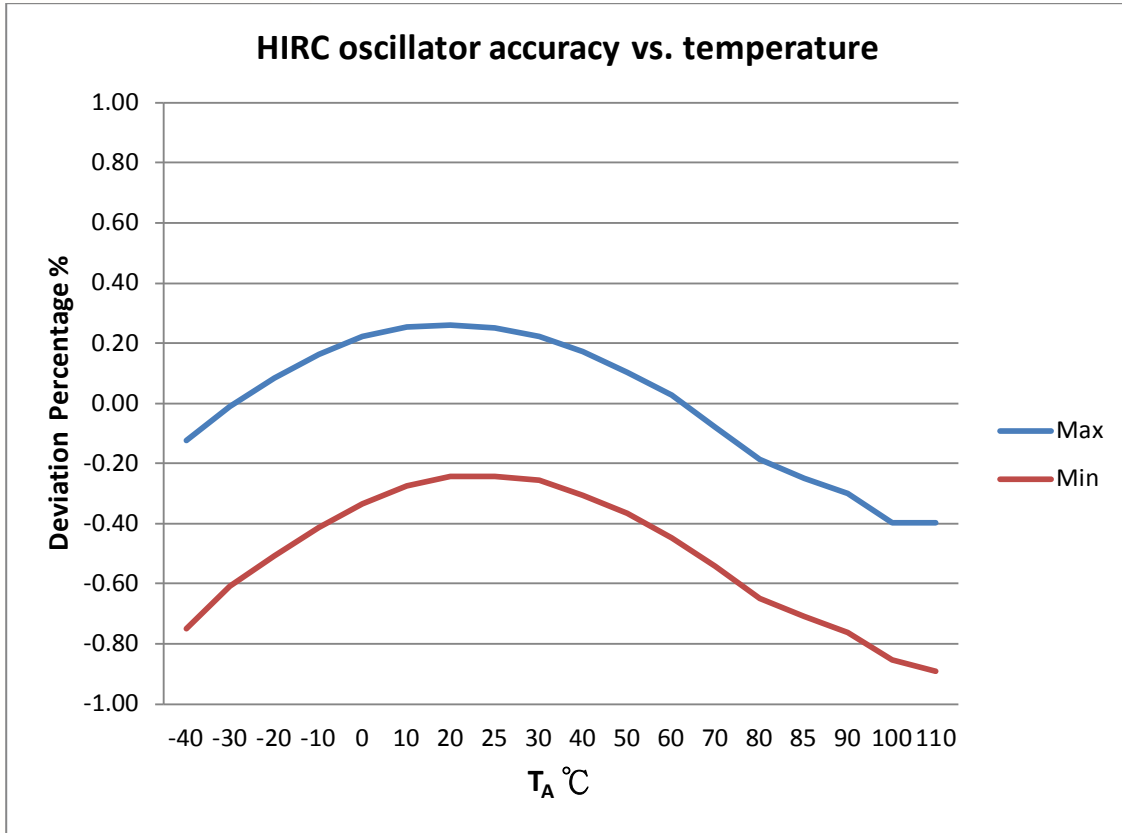


Figure 9-1 Mini5xDE Typical Crystal Application Circuit

9.3.4 22.1184 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	22.1184		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	$T_A = 25\text{ }^\circ\text{C}$ $V_{DD} = 5\text{ V}$
-2		-	+2	%	$T_A = -40\text{ }^\circ\text{C} \sim 105\text{ }^\circ\text{C}$ $V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$	
I_{HRC}	Operating Current	-	700	-	μA	$T_A = 25\text{ }^\circ\text{C}, V_{DD} = 5\text{ V}$



9.3.5 10 kHz Internal Low Speed RC Oscillator(LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{LRC}	Supply Voltage	2.5	-	5.5	V	-
f _{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-10	-	+10	%	V _{DD} =2.5V~ 5.5V T _A = 25°C
		-40	-	+40	%	V _{DD} =2.5V~ 5.5V T _A = -40°C~+105°C



10 PACKAGE DIMENSIONS

10.1 48-pin LQFP

