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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	33-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini54tde

Table of Contents

2 FEATURES

- Core
  - ARM® Cortex™-M0 core running up to 24 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Built-in LDO for wide operating voltage ranged: 2.5 V to 5.5 V
- Memory
  - 4 KB/ 8 KB/ 16 KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2 KB Flash for loader (LDROM)
  - 2 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - 4 ~ 24 MHz external crystal input (HXT)
  - 32.768 kHz external crystal input (LXT) for Power-down wake-up and system operation clock
  - 22.1184 MHz internal oscillator (HIRC) (1% accuracy at 25°C, 5V)
    - Dynamically calibrating the HIRC OSC to 22.1184 MHz ±1% from -40°C to 105°C by external 32.768K crystal oscillator (LXT)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and Power-down wake-up
- I/O Port
  - Up to 30 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - Input-only with high impendence
    - Push-pull output
    - Open-drain output
    - Quasi-bidirectional
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - Configurable default I/O mode of all pins after POR
- Timer

- Provides two channel 32-bit timers. One 8-bit pre-scale counter with 24-bit up counter for each timer
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous operation modes
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
- Provides event counter function
- Supports wake-up from Idle or Power-down mode

- WDT (Watchdog Timer)
  - Multiple clock sources
  - Supports wake-up from Idle or Power-down mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Independent 16-bit PWM duty control units with maximum six outputs
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake protections
  - Supports duty, period, and fault break interrupts
  - Supports duty/period trigger ADC conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period
  - Provides interrupt accumulation function
- UART (Universal Asynchronous Receiver/Transmitters)
  - One UART device
  - Buffered receiver and transmitter, each with 16-byte FIFO
  - Optional flow control function (CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports RS-485 function
- SPI (Serial Peripheral Interface)
  - One SPI devices
  - Supports Master/Slave mode

- Full-duplex synchronous serial data transfer
- Provides 3-wire function
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Rx latching data can be either at rising edge or at falling edge of serial clock
- Tx sending data can be either at rising edge or at falling edge of serial clock
- Supports Byte Suspend mode in 32-bit transmission
- 4-level depth FIFO buffer

- I^2C
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
  - Supports Power-down wake-up function
  - Support FIFO function
- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 300K SPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger, PWM trigger, or external pin trigger
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Build-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V

4.3.3 TSSOP 20-pin

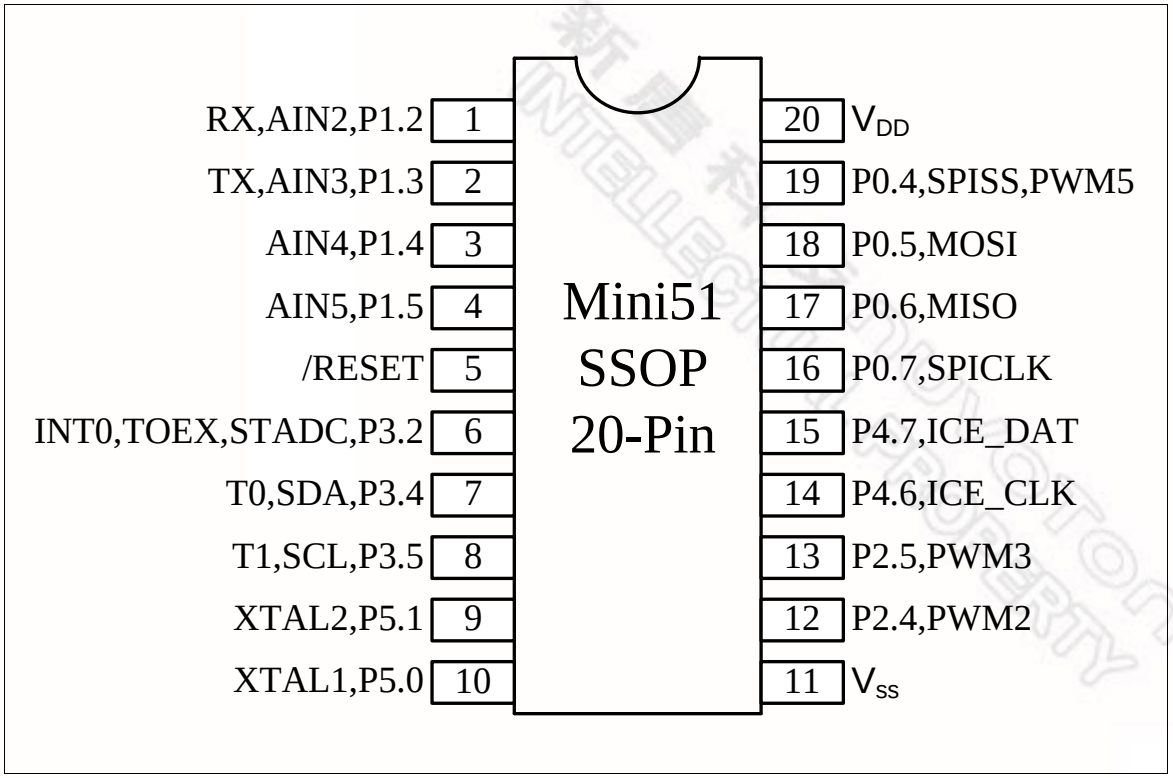


Figure 4.3-3 NuMicro Mini51™ Series TSSOP 20-pin Diagram

4.3.4 Mini54FHC (TSSOP20-pin)

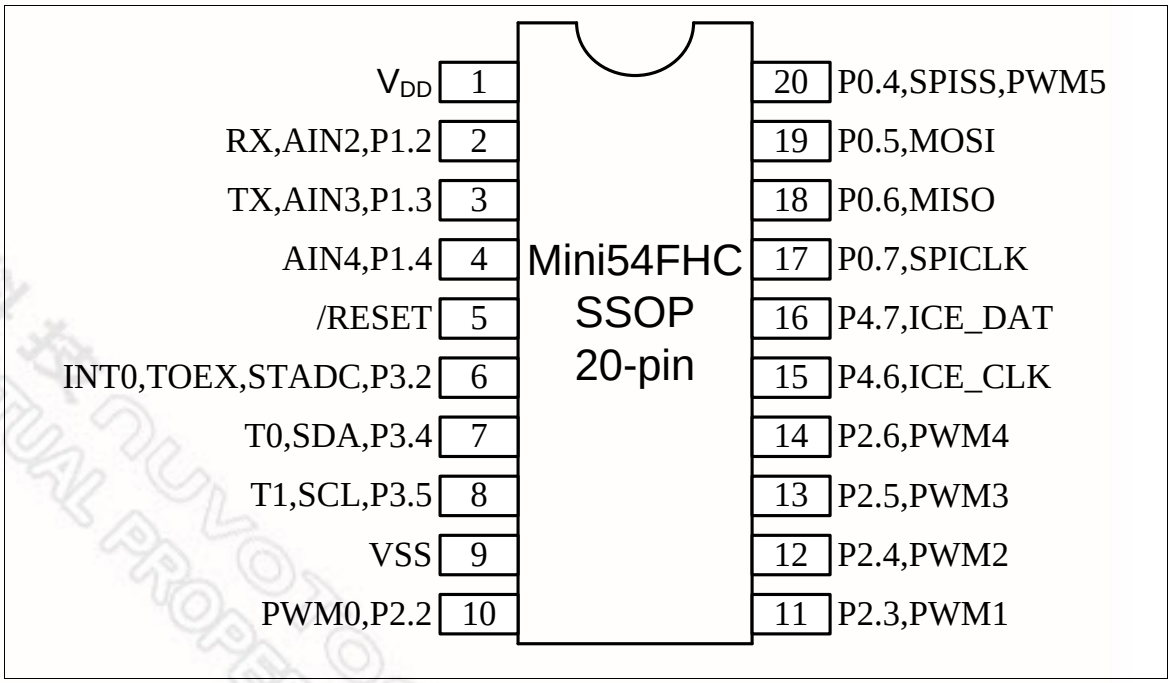


Figure 4.3-4 NuMicro Mini51™ Series TSSOP 20-pin Diagram

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
14	9	---	---	P3.6	I/O	General purpose digital I/O pin.
				ACMP0_O	O	Analog comparator output pin.
				CKO	O	Frequency divider output pin.
				T1EX	I	Timer 1 external capture/reset trigger input pin.
15	10	9	---	P5.1	I/O	General purpose digital I/O pin.
				XTAL2	O	The output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
16	11	10	---	P5.0	I/O	General purpose digital I/O pin.
				XTAL1	I	The input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
17	12	11	9	V_{SS}	P	Ground pin for digital circuit.
	33					
18	---	---	---	LDO_CAP	P	LDO output pin.
19	---	---	---	P5.5	I/O	General purpose digital I/O pin. User program must enable pull-up resistor in the QFN-33 package.
20	13	---	---	P5.2	I/O	General purpose digital I/O pin.
				INT1	I	External interrupt 1 input pin.
21	---	---	---	NC	---	Not connected.
22	14	---	10	P2.2	I/O	General purpose digital I/O pin.
				PWM0	O	PWM0 output of PWM unit.
23	15	---	11	P2.3	I/O	General purpose digital I/O pin.
				PWM1	O	PWM1 output of PWM unit.
24	16	12	12	P2.4	I/O	General purpose input/output digital pin.
				PWM2	O	PWM2 output of PWM unit.
25	17	13	13	P2.5	I/O	General purpose digital I/O pin.
				PWM3	O	PWM3 output of PWM unit.
26	18	---	14	P2.6	I/O	General purpose digital I/O pin.
				PWM4	O	PWM4 output of PWM unit.
				ACMP1_O	O	Analog comparator output pin.
27	---	---	---	NC	---	Not connected.
28	---	---	---	NC	---	Not connected.
29	19	14	15	P4.6	I/O	General purpose digital I/O pin.

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
				ICE_CLK	**I**	Serial wired debugger clock pin.
30	20	15	16	P4.7	**I/O**	General purpose digital I/O pin.
				ICE_DAT	**I/O**	Serial wired debugger data pin.
31	---	---	---	NC	**---**	Not connected.
32	21	16	17	P0.7	**I/O**	General purpose digital I/O pin.
				SPICLK	**I/O**	SPI serial clock pin.
33	22	17	18	P0.6	**I/O**	General purpose digital I/O pin.
				MISO	**I/O**	SPI MISO (master in/slave out) pin.
34	23	18	19	P0.5	**I/O**	General purpose digital I/O pin.
				MOSI	**O**	SPI MOSI (master out/slave in) pin.
35	24	19	20	P0.4	**I/O**	General purpose digital I/O pin.
				SPISS	**I/O**	SPI slave select pin.
				PWM5	**O**	PWM5 output of PWM unit.
36	---	---	---	NC	**---**	Not connected.
37	25	---	---	P0.1	**I/O**	General purpose digital I/O pin.
				RTSn	**O**	UART RTS pin.
				RX	**I**	UART data receiver input pin.
				SPISS	**I/O**	SPI slave select pin.
38	26	---	---	P0.0	**I/O**	General purpose digital I/O pin.
				CTSn	**I**	UART CTS pin.
				TX	**O**	UART transmitter output pin.
39	---	---	---	NC	**---**	Not connected.
40	---	---	---	NC	**---**	Not connected.
41	27	---	---	P5.3	**I/O**	General purpose digital I/O pin.
				AIN0	**AI**	ADC analog input pin.
42	28	20	1	V_{DD}	**P**	Power supply for digital circuit.
43				AV_{DD}	**P**	Power supply for analog circuit.
44	29	---	---	P1.0	**I/O**	General purpose digital I/O pin.
				AIN1	**AI**	ADC analog input pin.
				ACMP0_P	**AI**	Analog comparator positive input pin.
45	30	1	2	P1.2	**I/O**	General purpose digital I/O pin.
				AIN2	**AI**	ADC analog input pin.

6.2 Nested Vectored Interrupt Controller (NVIC)

6.2.1 Overview

The Cortex™-M0 CPU provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features.

6.2.2 Features

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority change
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the Interrupt Service Routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.3 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro Mini51™ series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as 0 and the lowest priority is denoted as 3. The default priority of all the user-configurable interrupts is 0. Note that the priority 0 is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-1 Exception Model

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
1 ~ 15	-	-	-	System exceptions	-
16	0	**BOD_OUT**	Brown-out	Brown-out low voltage detected interrupt	Yes
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt	Yes
18	2	**EINT0**	GPIO	External signal interrupt from P3.2 pin	Yes
19	3	**EINT1**	GPIO	External signal interrupt from P5.2 pin	Yes
20	4	**GP0/1_INT**	GPIO	External signal interrupt from GPIO group P0~P1	Yes
21	5	**GP2/3/4_INT**	GPIO	External signal interrupt from GPIO group P2~P4 except P3.2	Yes
22	6	**PWM_INT**	PWM	PWM interrupt	No
23	7	**BRAKE_INT**	PWM	PWM interrupt	No
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt	Yes
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt	Yes
26 ~ 27	10 ~ 11	-	-	-	
28	12	**UART_INT**	UART	UART interrupt	Yes

6.2.5 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending; however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

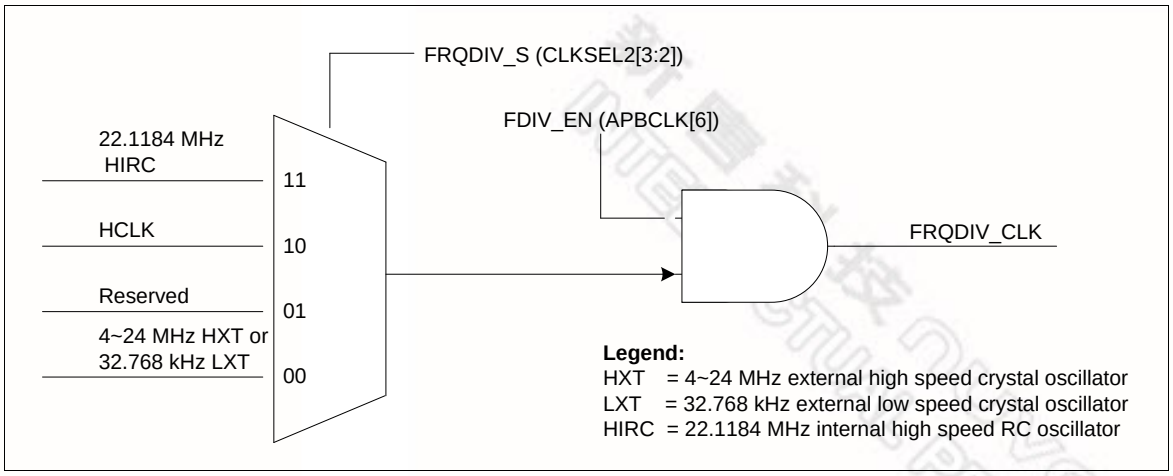


Figure 6.4-6 Clock Source of Frequency Divider

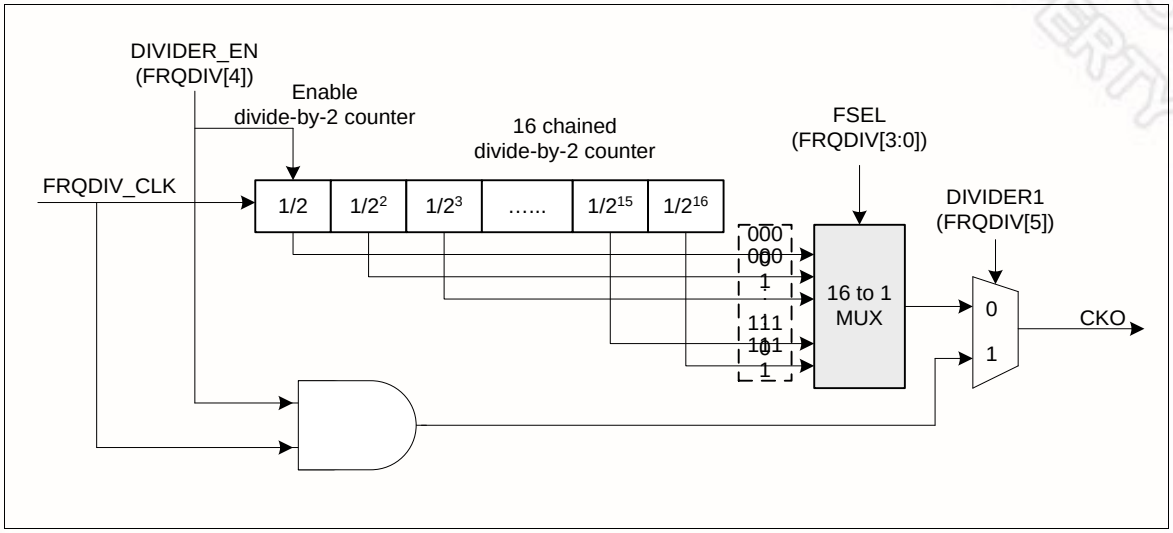


Figure 6.4-7 Block Diagram of Frequency Divider

6.6 Analog-to-Digital Converter (ADC)

6.6.1 Overview

The NuMicro Mini51™ series contains one 10-bit successive approximation analog-to-digital converters (SAR A/D converter) with eight input channels. The A/D converters can be started by software, external pin (STADC/P3.2) or PWM trigger.

6.6.2 Features

- Analog input voltage range: 0 ~ Analog Supply Voltage from AV_{DD}
- 10-bit resolution and 8-bit accuracy is guaranteed
- Up to eight single-end analog input channels
- 300 KSPS (AV_{DD} 4.5V - 5.5V) and 200 KSPS (AV_{DD} 2.5V - 5.5V) conversion rate
- An A/D conversion is performed one time on a specified channel
- An A/D conversion can be started by:
  - Software write 1 to ADST bit
  - External pin STADC
  - PWM trigger with optional start delay period
- Each conversion result is held in data register with valid and overrun indicators
- Conversion results can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 2 input sources: External analog voltage and internal fixed band-gap voltage

6.14 Watchdog Timer (WDT)

6.14.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.14.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

9 MINI51XXDE ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

9.2 DC Electrical Characteristics

(VDD - VSS = 2.5 ~ 5.5 V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operation voltage	2.5	-	5.5	V	V_{DD} = 2.5V ~ 5.5V up to 24 MHz
V_{SS} / AV_{SS}	Power Ground	-0.3	-	-	V	
V_{LDO}	LDO Output Voltage	1.62	1.8	1.98	V	V_{DD} ≥ 2.5 V
V_{BG}	Band-gap Voltage	1.20	1.24	1.28	V	V_{DD} = 2.5V ~ 5.5V, T_A = 25°C
		1.18	1.24	1.32	V	V_{DD} = 2.5V ~ 5.5V, T_A = -40°C~105°C
V_{DD}-AV_{DD}	Allowed Voltage Difference for V_{DD} and AV_{DD}	-0.3	0	0.3	V	-
I_{DD1}	Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Executed from Flash	-	9.2	-	mA	V_{DD} 5.5V; HXT 24 MHz; HIRC Disable; All digital modules Enabled

I_{DD16}		-	1.4	-	mA	V_{DD} 3.3 V HXT 4 MHz HIRC Disabled All digital modules Disabled
I_{DD17}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	225	-	μA	V_{DD} 5.5 V HXT Disabled HIRC □isabled LIRC Enabled All digital modules Enabled Only enable modules which support 10 kHz LIRC clock source
I_{DD18}		-	225	-	μA	V_{DD} 5.5 V HXT Disabled HIRC Disabled LIRC Enabled All digital modules Disabled
I_{DD19}		-	200	-	μA	V_{DD} 3.3 V HXT Disa□led HIRC Disabled LIRC Enabled All digital modules Enabled Only enable modules which support 10 kHz LIRC clock source
I_{DD20}		-	200	-	μA	V_{DD} 3.3 V HXT Disabled HIRC Disabled LIRC Enabled All digital modules Disa□led
I_{IDLE1}	Operating Current Idle Mode HCLK = 24MHz	-	7.1	-	mA	V_{DD} 5.5V HXT 24 MHz HIRC Disable All digital modules Enabled

I_{SK13}	Drain and Push-pull Mode)	5	8	-	mA	V_{DD} = 2.5 V, V_S = 0.45 V

Notes:

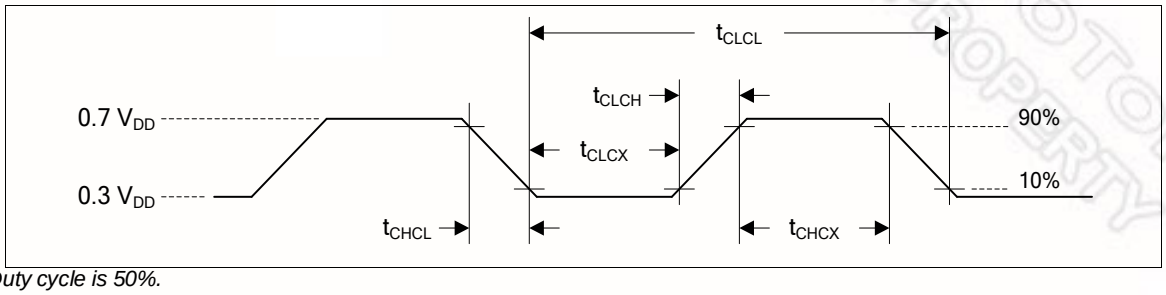
1. /RESET pin is a Schmitt trigger input.

2. XTAL1 is a CMOS input.

3. Pins of P0, P1, P2, P3, P4 and P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of VDD=5.5V, the transition current reaches its maximum value when VIN approximates to 2V.

9.3 AC Electrical Characteristics

9.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

9.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	2.5	-	mA	12 MHz, V_{DD} = 5.5V
		-	1.0	-	mA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

9.3.3 Typical Crystal Application Circuits

Crystal	C1	C2
4MHz ~ 24 MHz	10~20 pF	10~20 pF

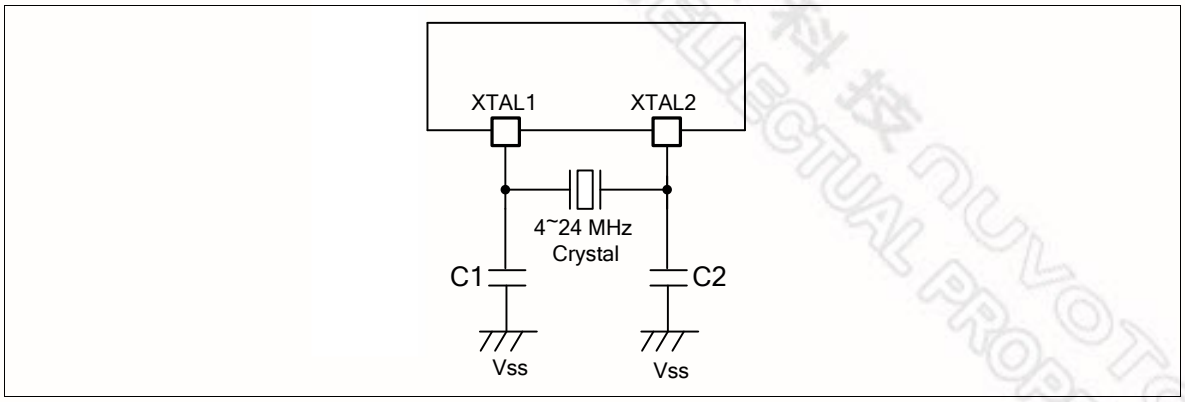
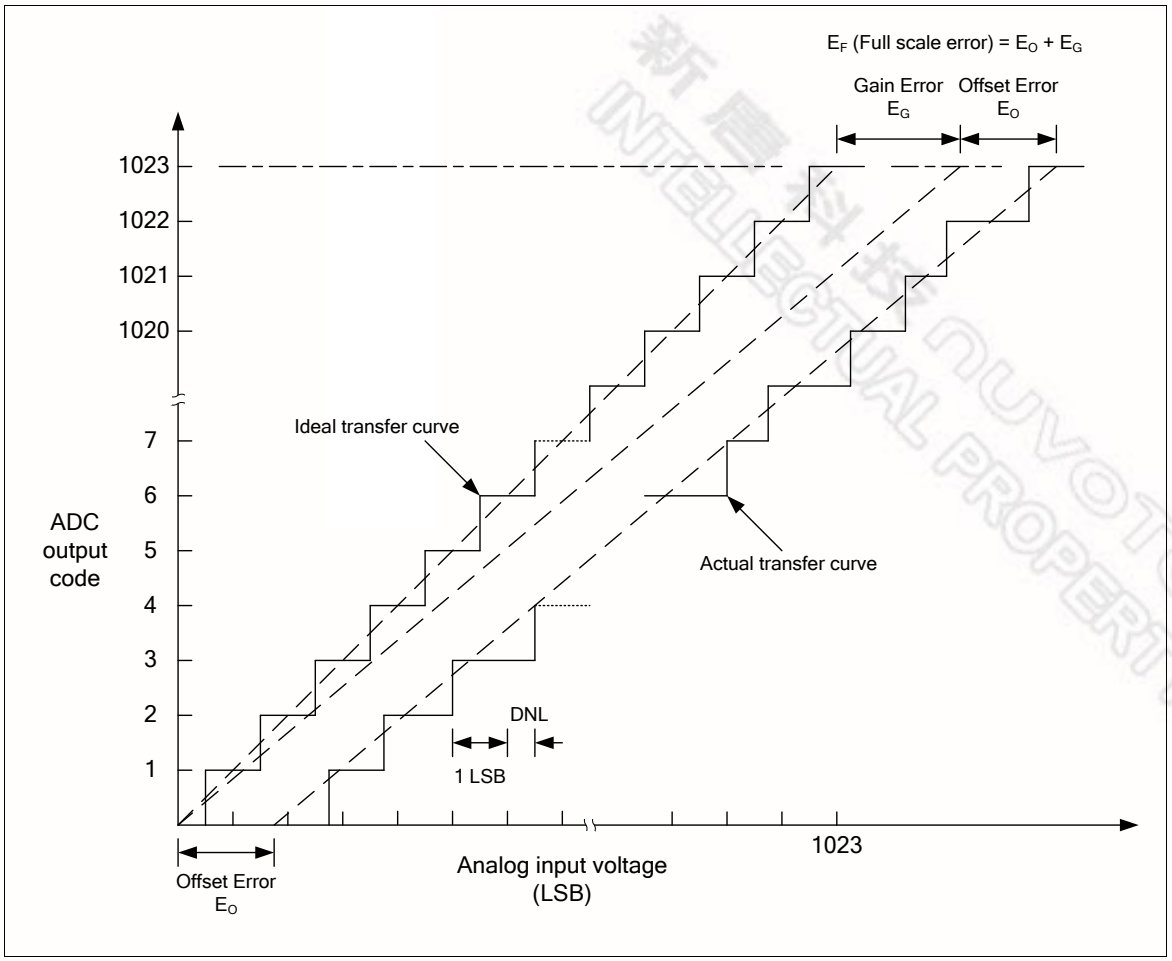


Figure 9-1Mini5xDE Typical Crystal Application Circuit

9.3.4 22.1184 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	22.1184		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5 V
		-2	-	+2	%	T_A = -40℃~105℃ V_{DD}=2.5 V~ 5.5 V
I_{HRC}	Operating Current	-	700	-	μA	T_A = 25 ℃,V_{DD} = 5 V



9.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.5	-	5.5	V	-
V_{LDO}	Output Voltage	1.62	1.8	1.98	V	-
T_A	Temperature	-40	25	105	℃	

Notes:

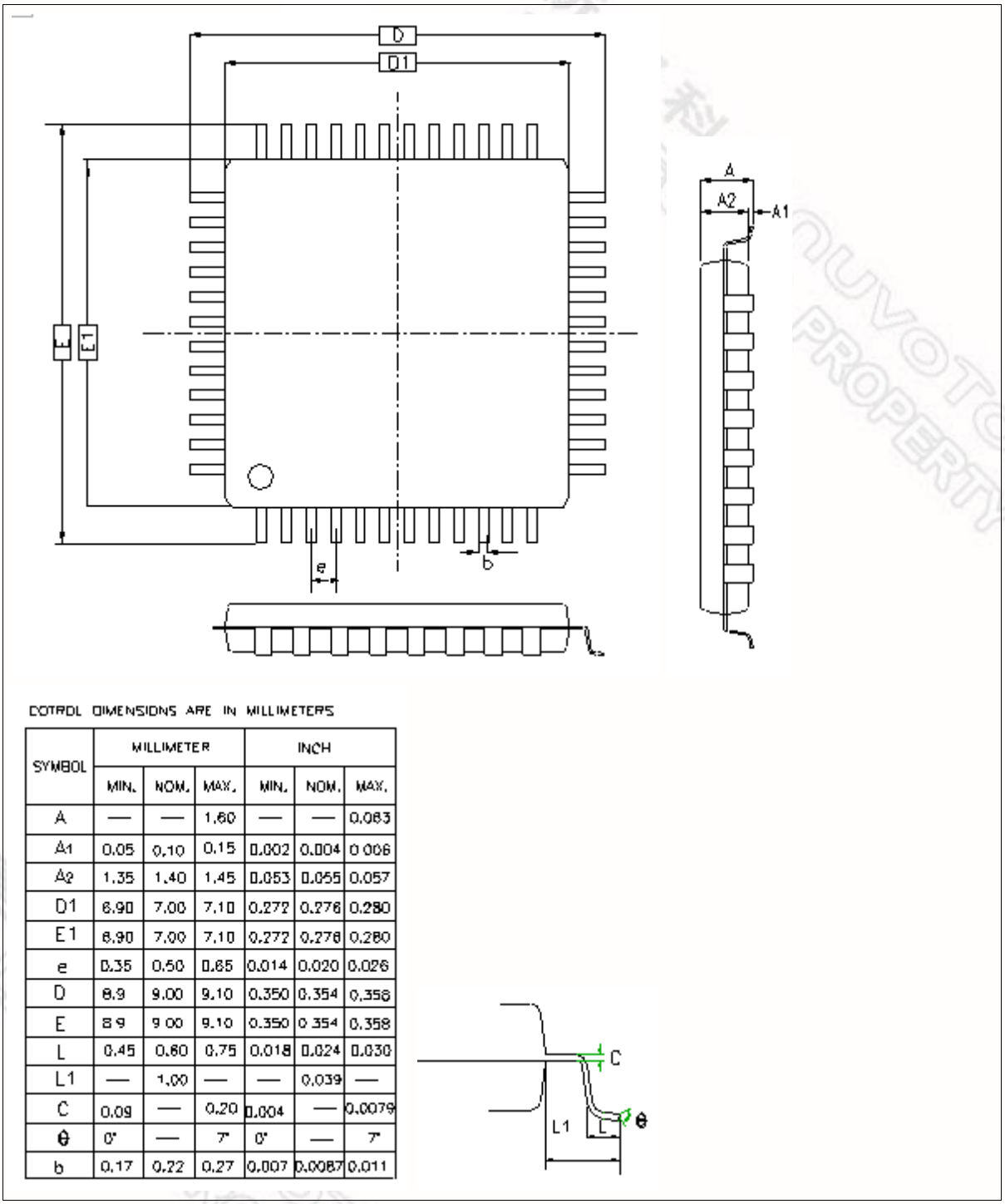
1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

9.4.3 Low Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-

10 PACKAGE DIMENSIONS

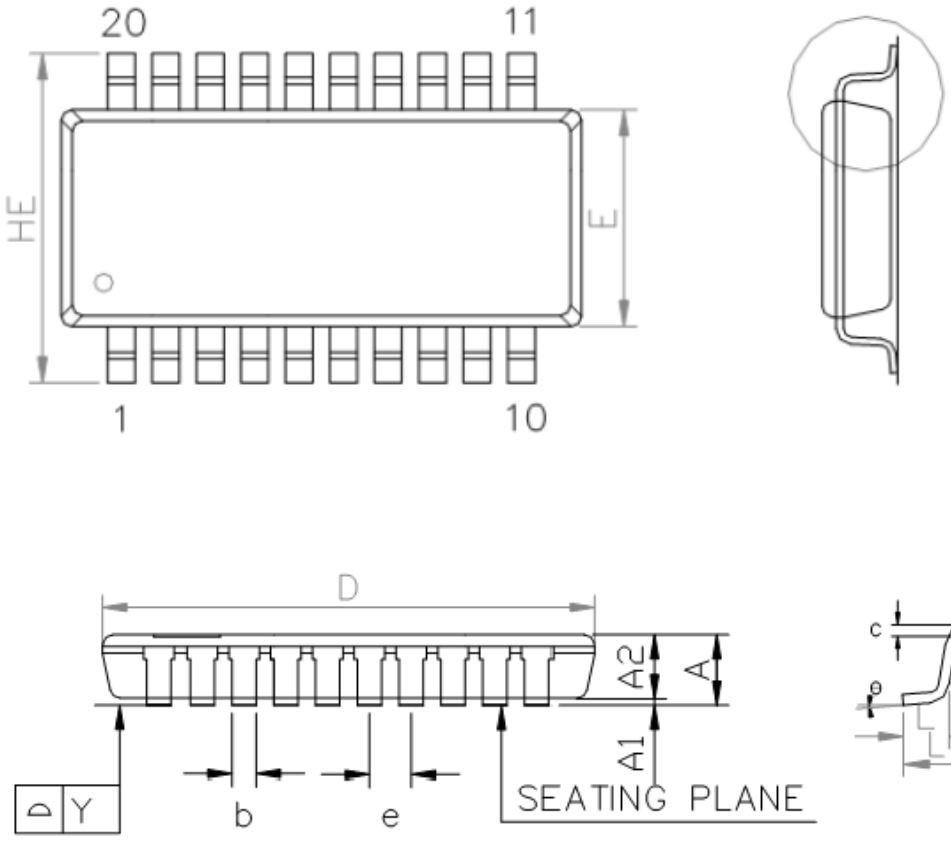
10.1 48-pin LQFP



CONTROL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.026
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.004	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

10.4 20-pin TSSOP



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	—	0.30	0.007	—	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	—	0.20	0.004	—	0.008
θ	0°	—	8°	0°	—	8°
Y	0.10 BASIC			0.004 BASIC		