Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	33-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini54zde

LIST OF TABLES

- Full-duplex synchronous serial data transfer
- Provides 3-wire function
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Rx latching data can be either at rising edge or at falling edge of serial clock
- Tx sending data can be either at rising edge or at falling edge of serial clock
- Supports Byte Suspend mode in 32-bit transmission
- 4-level depth FIFO buffer

- I^2C
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
  - Supports Power-down wake-up function
  - Support FIFO function
- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 300K SPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger, PWM trigger, or external pin trigger
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Build-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro Mini51™ Series Selection Code

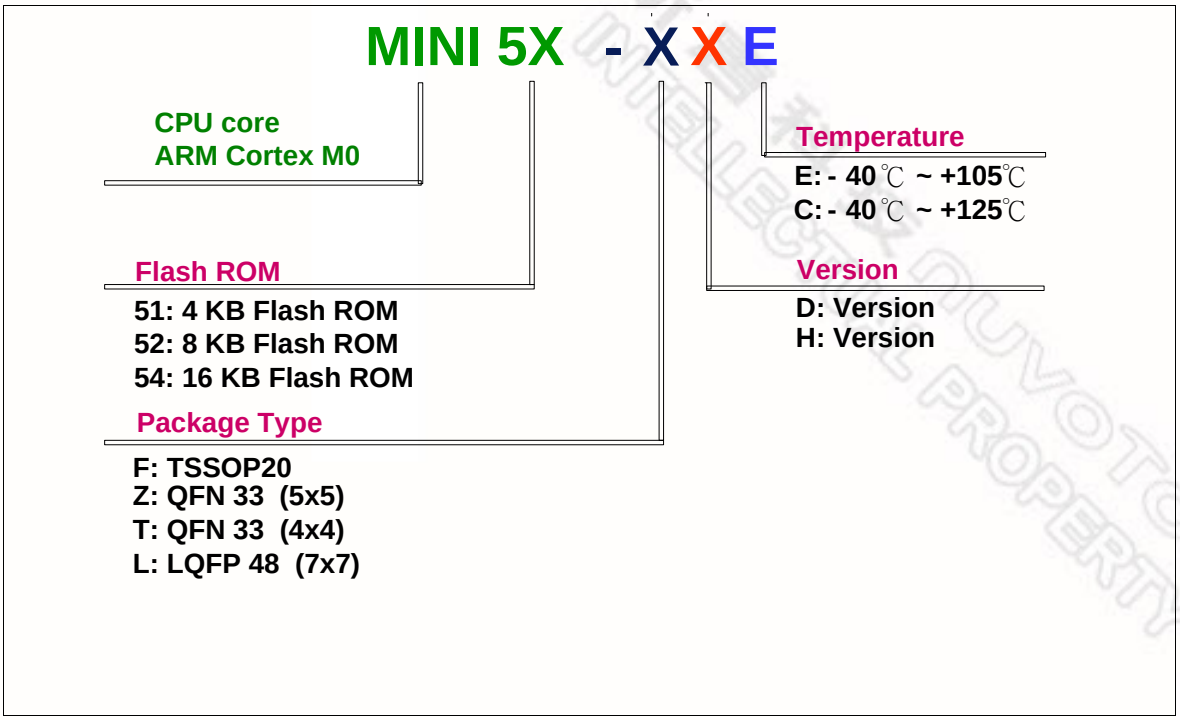


Figure 4.1-1 NuMicro Mini51™ Series Selection Code

4.2 NuMicro Mini51™ Series Product Selection Guide

Part No.	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP IAP	IRC 22.1184 MHz	Package
							UART	SPI	I²C						
MINI51FDE	4 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI51LDE	4 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI51ZDE	4 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI51TDE	4 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
MINI52FDE	8 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI52LDE	8 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI52ZDE	8 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI52TDE	8 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
MINI54FDE	16 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	3	4x10-bit	v	v	TSSOP20
MINI54LDE	16 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI54ZDE	16 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (5x5)
MINI54TDE	16 KB	2 KB	Configurable	2 KB	up to 29	2x 32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33 (4x4)
*MINI54FHC	16 KB	2 KB	Configurable	2 KB	up to 17	2x 32-bit	1	1	1	-	6	3x10-bit	v	v	TSSOP20

Table 4.2-1NuMicro Mini51™ Series Product Selection Guide

* Mini54FHC is a special part number, not pin to pin compatible to others Mini51series part number.

4.3.3 TSSOP 20-pin

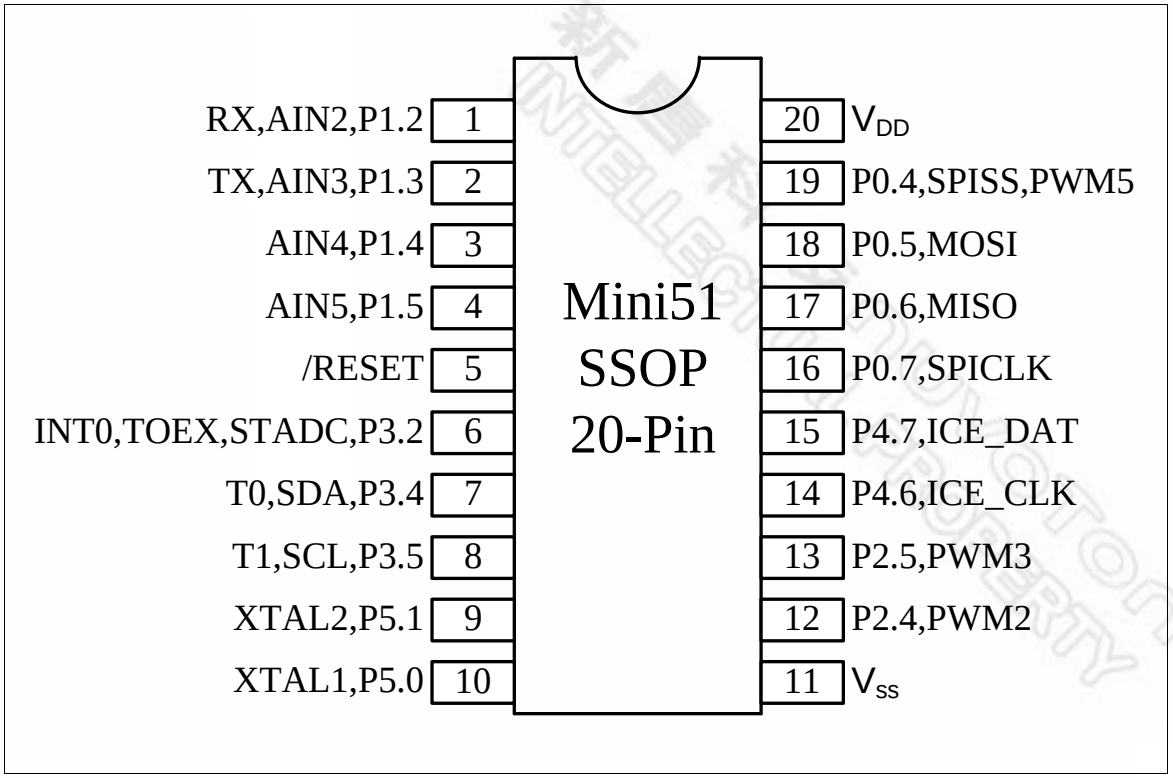


Figure 4.3-3 NuMicro Mini51™ Series TSSOP 20-pin Diagram

4.3.4 Mini54FHC (TSSOP20-pin)

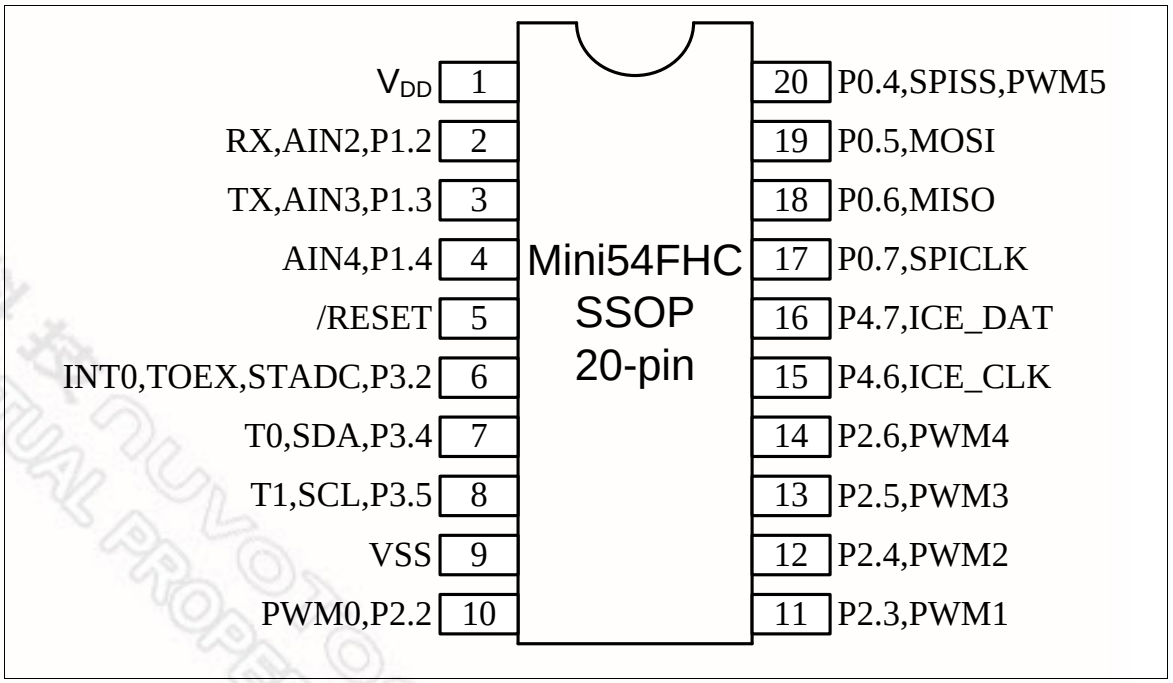


Figure 4.3-4 NuMicro Mini51™ Series TSSOP 20-pin Diagram

4.4 Pin Description

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
1	---	---	---	NC	**---**	Not connected
2	1	4	---	P1.5	**I/O**	General purpose digital I/O pin
				AIN5	**AI**	ADC analog input pin
				ACMP0_P	**AI**	Analog comparator positive input pin
3	2	5	5	/RESET	**I(ST)**	The Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. /RESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
4	3	---	---	P3.0	**I/O**	General purpose digital I/O pin
				AIN6	**AI**	ADC analog input pin
				ACMP1_N	**AI**	Analog comparator negative input pin
5	---	---	---	AV_{SS}	**AP**	Ground pin for analog circuit
6	4	---	---	P5.4	**I/O**	General purpose digital I/O pin
7	5	---	---	P3.1	**I/O**	General purpose digital I/O pin
				AIN7	**AI**	ADC analog input pin
				ACMP1_P	**AI**	Analog comparator positive input pin
8	6	6	6	P3.2	**I/O**	General purpose digital I/O pin
				INT0	**I**	External interrupt 0 input pin
				STADC	**I**	ADC external trigger input pin
				T0EX	**I**	Timer 0 external capture/reset trigger input pin
				ACMP1_P	**AI**	Analog comparator positive input pin
9	7	7	7	P3.4	**I/O**	General purpose digital I/O pin
				T0	**I/O**	Timer 0 external event counter input pin
				SDA	**I/O**	I^2C data I/O pin
				ACMP1_P	**AI**	Analog comparator positive input pin
10	8	8	8	P3.5	**I/O**	General purpose digital I/O pin
				T1	**I/O**	Timer 1 external event counter input pin
				SCL	**I/O**	I^2C clock I/O pin
				ACMP1_P	**AI**	Analog comparator positive input pin
11	---	---	---	NC	**---**	Not connected.
12	---	---	---	NC	**---**	Not connected.
13	---	--	--	NC	**---**	Not connected.

Pin Number				Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin	Mini54FHCT SSOP20-pin			
14	9	---	---	P3.6	I/O	General purpose digital I/O pin.
				ACMP0_O	O	Analog comparator output pin.
				CKO	O	Frequency divider output pin.
				T1EX	I	Timer 1 external capture/reset trigger input pin.
15	10	9	---	P5.1	I/O	General purpose digital I/O pin.
				XTAL2	O	The output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
16	11	10	---	P5.0	I/O	General purpose digital I/O pin.
				XTAL1	I	The input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
17	12	11	9	V_{SS}	P	Ground pin for digital circuit.
	33					
18	---	---	---	LDO_CAP	P	LDO output pin.
19	---	---	---	P5.5	I/O	General purpose digital I/O pin. User program must enable pull-up resistor in the QFN-33 package.
20	13	---	---	P5.2	I/O	General purpose digital I/O pin.
				INT1	I	External interrupt 1 input pin.
21	---	---	---	NC	---	Not connected.
22	14	---	10	P2.2	I/O	General purpose digital I/O pin.
				PWM0	O	PWM0 output of PWM unit.
23	15	---	11	P2.3	I/O	General purpose digital I/O pin.
				PWM1	O	PWM1 output of PWM unit.
24	16	12	12	P2.4	I/O	General purpose input/output digital pin.
				PWM2	O	PWM2 output of PWM unit.
25	17	13	13	P2.5	I/O	General purpose digital I/O pin.
				PWM3	O	PWM3 output of PWM unit.
26	18	---	14	P2.6	I/O	General purpose digital I/O pin.
				PWM4	O	PWM4 output of PWM unit.
				ACMP1_O	O	Analog comparator output pin.
27	---	---	---	NC	---	Not connected.
28	---	---	---	NC	---	Not connected.
29	19	14	15	P4.6	I/O	General purpose digital I/O pin.

6.4.2 System Clock and SysTick Clock

The system clock has three clock sources which are generated from clock generator block. The clock source switches depending on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown below.

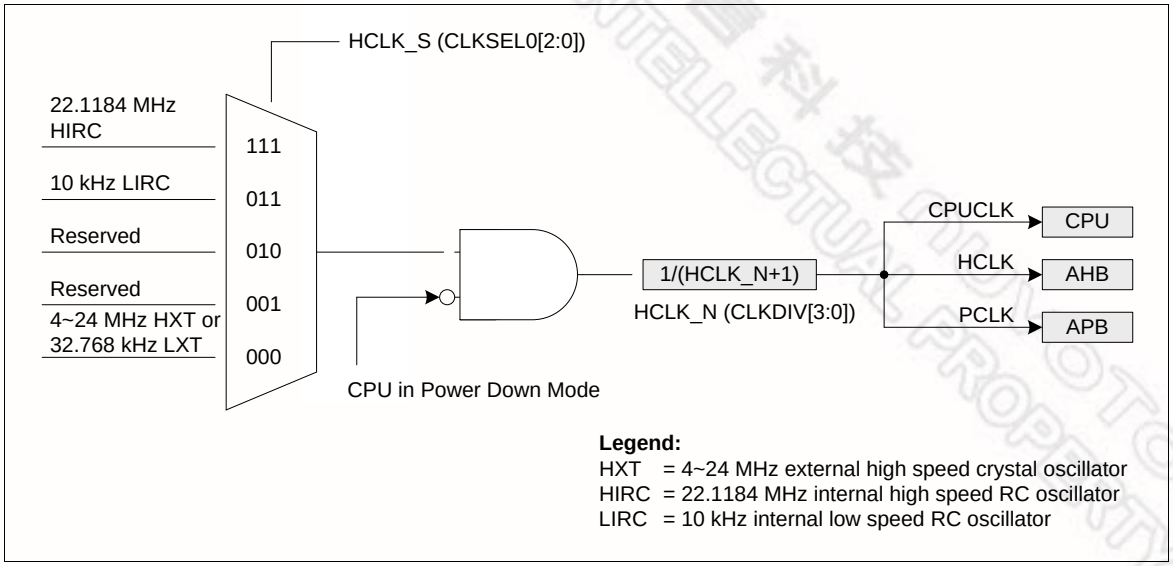


Figure 6.4-2 System Clock Block Diagram

The clock source of SysTick in Cortex™-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switches depending on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown below.

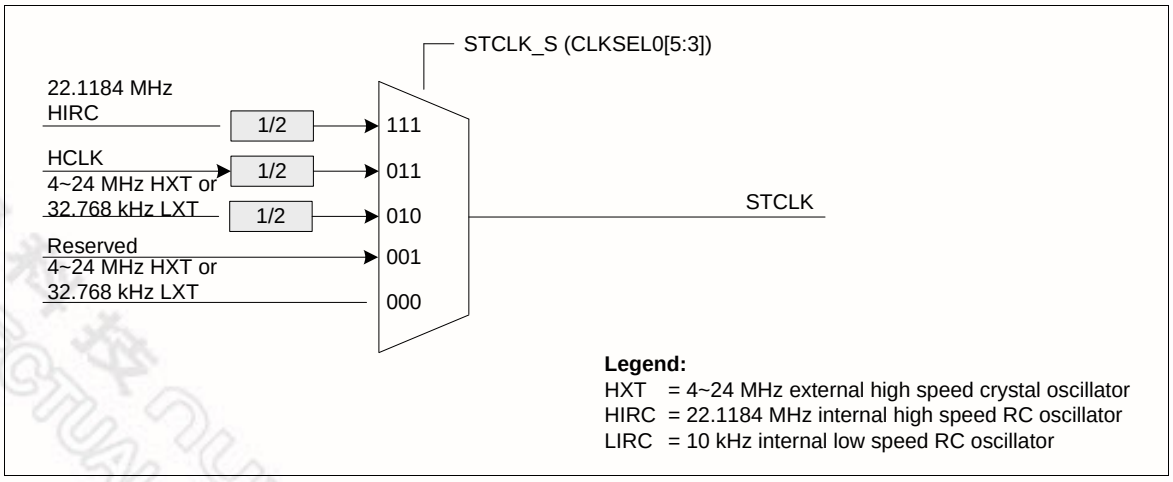


Figure 6.4-3 SysTick Clock Control Block Diagram

	Ext. CLK (HXT Or LXT)	HIRC	LIRC	PCLK
WDT	Yes	No	Yes	Yes
Timer0	Yes	Yes	Yes	Yes
Timer1	Yes	Yes	Yes	Yes
I²C	No	No	No	Yes
SPI	No	No	No	Yes
UART	Yes	Yes	No	No
PWM	No	No	No	Yes
ADC	Yes	Yes	No	Yes
ACMP	No	No	No	Yes

Table 6.4-1 Peripheral Clock Source Selection Table

6.4.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripheral clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator (LIRC) clock
- 32.768 kHz external low speed crystal oscillator (LXT) clock (If PD_32K = 1 and XTLCLK_EN[1:0] = 10)
- Peripherals Clock (When 10 kHz low speed oscillator is adopted as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

6.4.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\boldsymbol{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

if DIVIDER1(FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CKO pin directly.

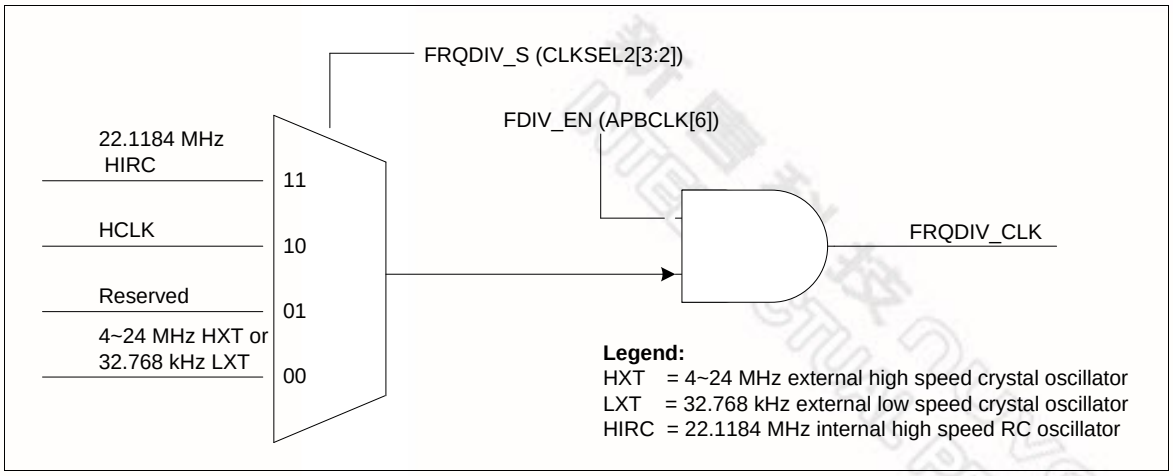


Figure 6.4-6 Clock Source of Frequency Divider

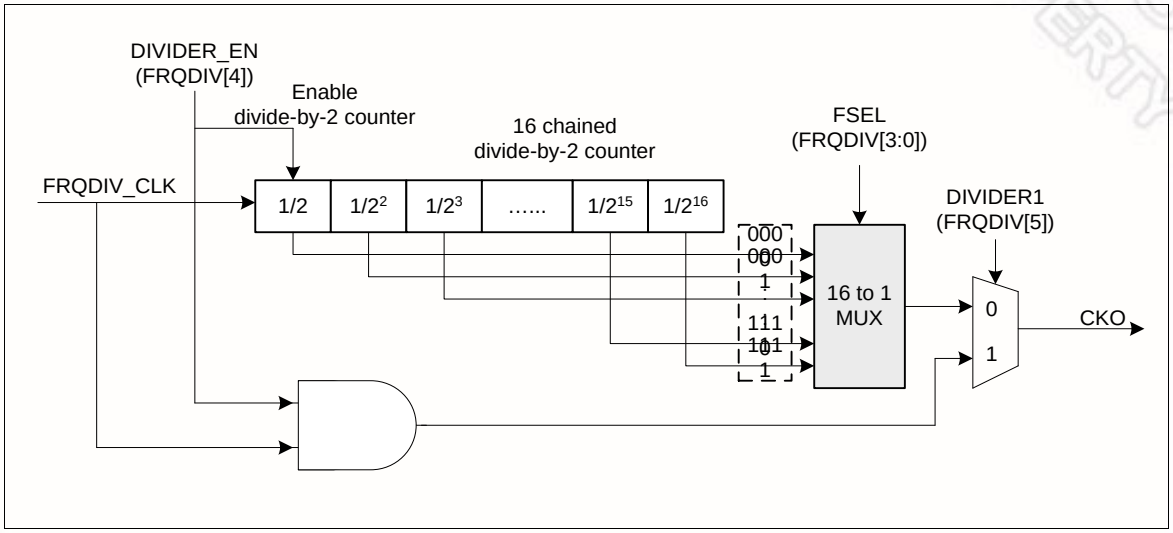


Figure 6.4-7 Block Diagram of Frequency Divider

6.6 Analog-to-Digital Converter (ADC)

6.6.1 Overview

The NuMicro Mini51™ series contains one 10-bit successive approximation analog-to-digital converters (SAR A/D converter) with eight input channels. The A/D converters can be started by software, external pin (STADC/P3.2) or PWM trigger.

6.6.2 Features

- Analog input voltage range: 0 ~ Analog Supply Voltage from AV_{DD}
- 10-bit resolution and 8-bit accuracy is guaranteed
- Up to eight single-end analog input channels
- 300 KSPS (AV_{DD} 4.5V - 5.5V) and 200 KSPS (AV_{DD} 2.5V - 5.5V) conversion rate
- An A/D conversion is performed one time on a specified channel
- An A/D conversion can be started by:
  - Software write 1 to ADST bit
  - External pin STADC
  - PWM trigger with optional start delay period
- Each conversion result is held in data register with valid and overrun indicators
- Conversion results can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 2 input sources: External analog voltage and internal fixed band-gap voltage

6.7 Flash Memory Controller (FMC)

6.7.1 Overview

The NuMicro Mini51™ series is equipped with 4K/8K/16K bytes on chip embedded flash memory for application program (APROM) that can be updated through ISP procedure. In-System-Programming (ISP) and In-Application-Programming (IAP) enable user to update program memory when chip is soldered on PCB. After chip power on Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro Mini51™ series also provides Data Flash region that is shared with APROM and its start address is configurable and defined by user in CONFIG1.

6.7.2 Features

- Running up to 24 MHz with zero wait state for discontinuous address read access
- 4/8/16 Kbytes application program memory (APROM)
- 2 Kbytes in system programming (ISP) loader program memory (LDROM)
- Programmable data flash start address
- All embedded flash memory supports 512 bytes page erase
- In System Program (ISP)/In Application Program (IAP) to update on chip flash memory

6.9 I2C Serial Interface Controller (I2C)

6.9.1 Overview

I^2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I^2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. The I^2C also supports Power-down wake up function.

6.9.2 Features

The I^2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus include:

- Master/Slave mode
- Bi-directional data transfer between masters and slaves
- Multi-master bus
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter that requests the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
- External pull-up needed for higher output pull-up speed
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address registers with mask option)
- Supports Power-down wake-up function
- Support FIFO function

7 ARM® CORTEX™-M0 CORE

7.1 Overview

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset and can be entered as a result of an exception return. The following figure shows the functional controller of the processor.

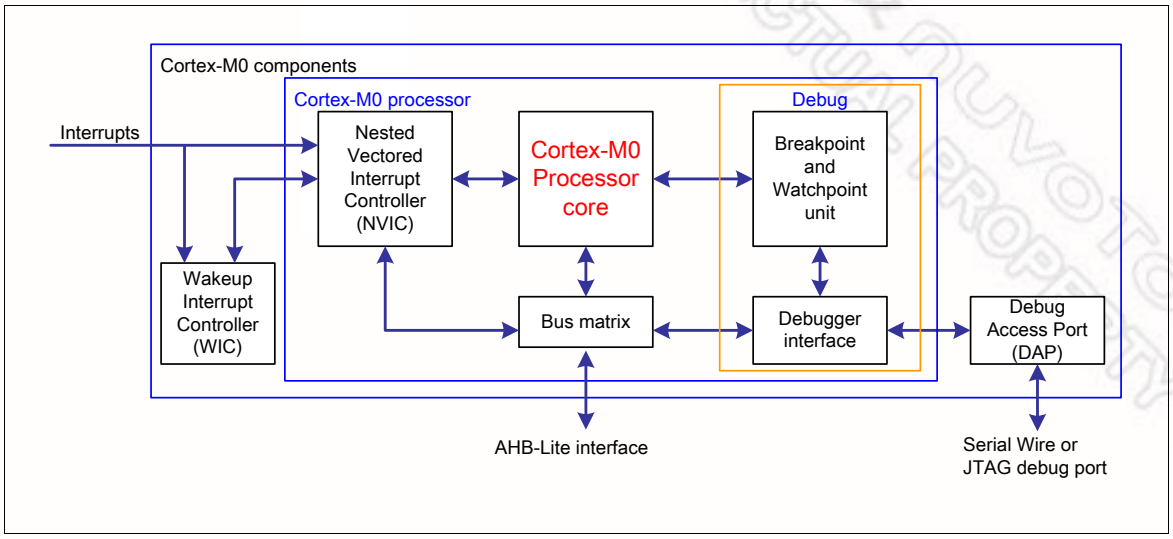


Figure 7.1-1 Functional Block Diagram

7.2 Features

- A low gate count processor
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model:

    This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power Idle mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Idle mode

- Debug support
  - Four hardware breakpoints
  - Two watch points
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

7.3 System Timer (SysTick)

The Cortex™-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer to count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

I_{DD2}	Operating Current Normal Run Mode HCLK =22.1184 MHz while(1){} Executed from Flash	-	7.0	-	mA	V_{DD} 5.5V HXT 24 MHz HIRC Disabled All digital modules Disabled
I_{DD3}		-	7.1	-	mA	V_{DD} 3.3V HXT 24 MHz HIRC Disable All digital modules Enabled
I_{DD4}		-	5.0	-	mA	V_{DD} 3.3 V HXT 24 MHz HIRC Disabled All digital modules Disabled
I_{DD5}		-	6.1	-	mA	V_{DD} 5.5V HXT Disabled HIRC Enabled All digital modules Enabled
I_{DD6}		-	3.9	-	mA	. V_{DD} 5.5V HXT Disabled HIRC Enabled All digital modules Disabled
I_{DD7}		-	6.0	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled All digital modules Enabled
I_{DD8}		-	3.9	-	mA	V_{DD} 3.3V HXT Disabled HIRC Enabled All digital modules Disabled

I_{IDLE2}	Operating Current Idle Mode HCLK=22.1184 MHz	-	4.9	-	mA	V_{DD} 5.5V; HXT 24 MHz; HIRC Disabled; All digital modules Disabled
I_{IDLE3}		-	5.1	-	mA	V_{DD} 3.3V; HXT 24 MHz; HIRC Disable; All digital modules Enabled
I_{IDLE4}		-	2.9	-	mA	V_{DD} 5.5V; HXT 24 MHz; HIRC Disabled; All digital modules Disabled
I_{IDLE5}		-	4.1	-	mA	V_{DD} 5.5V; HXT Disabled; HIRC Enabled; All digital modules Enabled
I_{IDLE6}		-	2.0	-	mA	. V_{DD} 5.5V; HXT Disabled; HIRC Enabled; All digital modules Disabled
I_{IDLE7}		-	4.1	-	mA	V_{DD} 3.3V; HXT Disabled; HIRC Enabled; All digital modules Enabled
I_{IDLE8}		-	1.9	-	mA	V_{DD} 3.3V; HXT Disabled; HIRC Enabled; All digital modules Disabled

I_{SK13}	Drain and Push-pull Mode)	5	8	-	mA	V_{DD} = 2.5 V, V_S = 0.45 V

Notes:

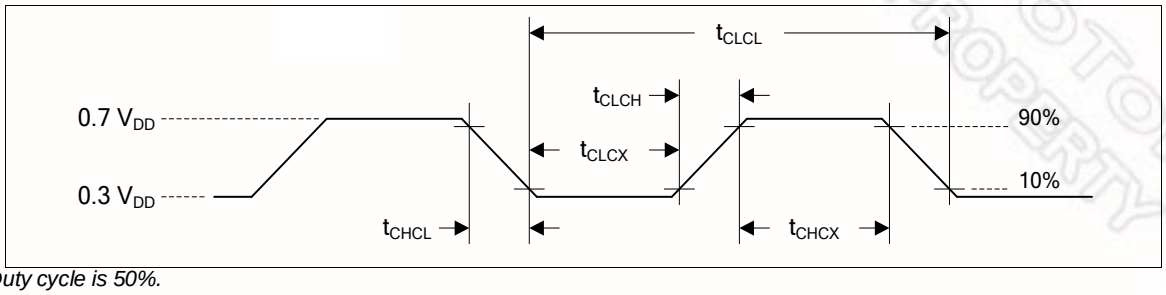
1. /RESET pin is a Schmitt trigger input.

2. XTAL1 is a CMOS input.

3. Pins of P0, P1, P2, P3, P4 and P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of VDD=5.5V, the transition current reaches its maximum value when VIN approximates to 2V.

9.3 AC Electrical Characteristics

9.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

9.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	2.5	-	mA	12 MHz, V_{DD} = 5.5V
		-	1.0	-	mA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

9.4 Analog Characteristics

9.4.1 10-bit SARADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	10	Bit	-
DNL	Differential Nonlinearity Error	-	-1~1.5	-1~+2.5	LSB	-
INL	Integral Nonlinearity Error	-	±1	±2	LSB	-
E_O	Offset Error	-	1	2	LSB	-
E_G	Gain Error (Transfer Gain)	-	-1	-3	LSB	-
E_A	Absolute Error	-	3	4	LSB	-
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency	-	-	4.2	MHz	AV_{DD} = 4.5~5.5 V
		-	-	2.8		AV_{DD} =2.5~5.5 V
F_S	Sample Rate (F_{ADC}/T_{CONV})	-	-	300	kSPS	AV_{DD} = 4.5~5.5 V
		-	-	200	kSPS	AV_{DD} = 2.5~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	N is sampling counter, N=0,1,2, 4,8, 16,32, 4, 128, 256,1024
T_{CONV}	Total Conversion Time	N+14			$1/F_{ADC}$	
AV_{DD}	Supply Voltage	2.5	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	600	-	μA	AV_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	3.2	-	pF	-
R_{IN}	Input Load	-	6	-	kΩ	-

Note: ADC voltage reference is same with AV_{DD}