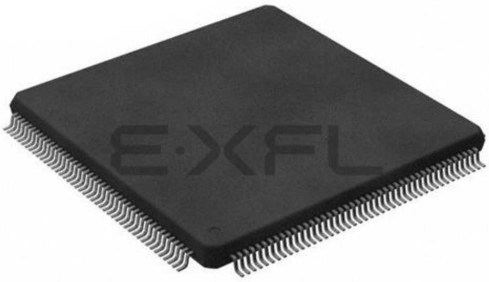


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-R4
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	117
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	208K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 5.5V
Data Converters	A/D 50x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9ef226epmc-gsk5e2

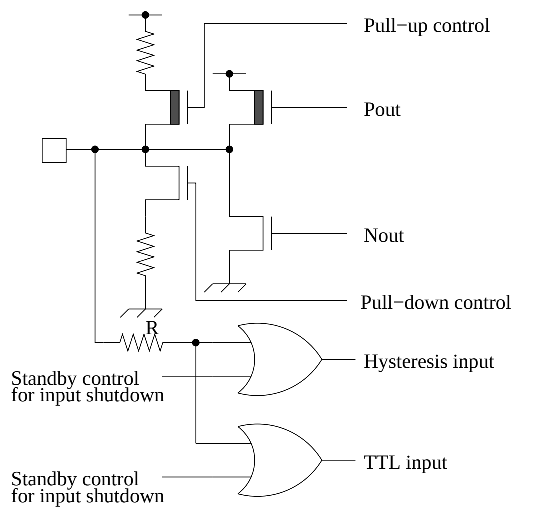
Table 2. Device Features (Continued)

Feature	Description
EEPROM Emulation Flash Memory[1]	■ 48 KB ■ Single error correction, double error detection (SECDED) ECC support ■ Support for sector erase ■ EEPROM emulation mode support ■ Support for mirroring of memory in 3 diverse memory-mapped regions ■ 6 sectors of 8KB each ■ Sector-wise access protection for write and read accesses **Note** 1. Electronically Erasable and Programmable Read-Only Memory (EEPROM).
Quad SPI	■ Supports legacy as well as the dual-bit and quad-bit modes of SPI operation ■ Supports up to four slave devices in master mode ■ Programmable transfer rate, active-level of slave-select signal, polarity, and phase of the serial clock per slave select ■ Support for memory mapped operation of external serial flash and serial SRAM devices in command sequencer mode ■ Additional direct mode support for standard SPI operation through FIFO interface
Error Collection	■ Error collection on all peripherals ■ Optional Non-Maskable Interrupt (NMI) generation capability
Low Voltage Detect	■ Low voltage detection for 5V, 3.3V, and 1.2V ■ Programmable thresholds ■ Reset generation capability on low voltage events
I/O Ports	■ All functional pins can be used as GPIO ■ Programmable analog or digital functionality selection ■ Programmable input levels (Automotive, CMOS, and TTL) ■ Programmable pull-up/pull-down and output drive
MediaLB	■ Implements ■ Supports 16 logical channels ■ Each logical channel can be programmed as synchronous, asynchronous, isochronous and control channel type and as transmit or receive ■ Loop back mode between the logical channel 0 (reception) and logical channel 1(transmission) ■ Programmable for 256Fs, 512Fs and 1024Fs transfer rates of operation at either 44.0kHz, 48.0kHz, or 48.1kHz. ■ 3-pin mode
SHE	■ Implements all commands defined by the functional specification of SHE (chapter 7) ■ Provides AES-128 encryption and decryption operations ■ Electronic cipher book (ECB) and cipher block chaining (CBC) modes ■ Supports generation of the cipher-based message authentication code (CMAC) ■ Implements Miyaguchi-Preneel compression function. ■ Provides random number generation function ■ Supports secure booting ■ Measurement during / before application start-up ■ Secure boot mode, start address and length of the bootloader are configurable by the user ■ Secure key storage implemented in EEFLASH
CRC	■ Programmable 8, 16, 24 or 32 bit input data width ■ Programmable polynomial value (Polynomial degree from 2 to 32) ■ Programmable initial seed value ■ Programmable final checksum XOR value ■ Interrupt and DMA trigger capability ■ Configurable input/output bit reflection and byte swapping ■ Supports PPU ■ Supports block/multiple data transfers (more than 32-bit)
Packages	QFP-176 (series variant)

Table 20. RICFG3

Register	Resource Input	RESSEL[3:0] PORTSEL[3:0]	Source for Resource Input							
			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
			Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
RLT0TIN (0x0800)	RLT0_TIN	RESSEL (0-7)	PORT_PIN	RLT9_TOT	RLT9_UFSET	RLT1_TOT	PPG0_PPGA	SPECIAL0_MCLKDIV4	SPECIAL0_RCCLKDIV4	-
		RESSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
		PORTSEL (0-7)	reserved	P0_47	P2_22	P1_11	P2_43	reserved	reserved	reserved
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
RLT1TIN (0x0820)	RLT1_TIN	RESSEL (0-7)	PORT_PIN	RLT0_TOT	RLT0_UFSET	RLT2_TOT	PPG1_PPGA	SPECIAL0_MCLKDIV4	SPECIAL0_RCCLKDIV4	-
		RESSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
		PORTSEL (0-7)	reserved	reserved	P2_23	P1_15	P2_39	reserved	P2_51	reserved
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
RLT2TIN (0x0840)	RLT2_TIN	RESSEL (0-7)	PORT_PIN	RLT1_TOT	RLT1_UFSET	RLT3_TOT	PPG2_PPGA	SPECIAL0_MCLKDIV4	SPECIAL0_RCCLKDIV4	-
		RESSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
		PORTSEL (0-7)	reserved	P0_43	P2_24	P1_19	P2_35	reserved	P2_21	reserved
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
RLT3TIN (0x0860)	RLT3_TIN	RESSEL (0-7)	PORT_PIN	RLT2_TOT	RLT2_UFSET	RLT4_TOT	PPG3_PPGA	SPECIAL0_MCLKDIV4	SPECIAL0_RCCLKDIV4	-
		RESSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
		PORTSEL (0-7)	reserved	P0_45	P1_30	P1_43	P1_08	reserved	P2_13	reserved
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
RLT4TIN (0x0880)	RLT4_TIN	RESSEL (0-7)	PORT_PIN	RLT3_TOT	RLT3_UFSET	RLT5_TOT	PPG4_PPGA	USART0_SOT	USART6_SOT	-
		RESSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
		PORTSEL (0-7)	reserved	P0_46	P1_31	P1_44	P1_09	reserved	P2_14	reserved
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
RLT5TIN (0x08A0)	RLT5_TIN	RESSEL (0-7)	PORT_PIN	RLT4_TOT	RLT4_UFSET	RLT6_TOT	PPG5_PPGA	USART0_SOT	USART6_SOT	-
		RESSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
		PORTSEL (0-7)	reserved	P0_40	P1_39	P2_25	P1_12	reserved	reserved	P2_50
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
RLT6TIN (0x08C0)	RLT6_TIN	RESSEL (0-7)	PORT_PIN	RLT5_TOT	RLT5_UFSET	RLT7_TOT	PPG6_PPGA	UDC0_UDOT0	UDC0_UDOT1	-
		RESSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
		PORTSEL (0-7)	reserved	P0_41	P1_40	P1_13	reserved	P2_48	reserved	reserved
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
RLT7TIN (0x08E0)	RLT7_TIN	RESSEL (0-7)	PORT_PIN	RLT6_TOT	RLT6_UFSET	RLT8_TOT	PPG7_PPGA	UDC0_UDOT0	UDC0_UDOT1	-
		RESSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
		PORTSEL (0-7)	reserved	reserved	reserved	P2_38	reserved	P2_49	reserved	reserved
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Table 25. IO Circuit Type (Continued)

<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>TTL33</td><td>
</td><td>

■ CMOS level output (programmable)

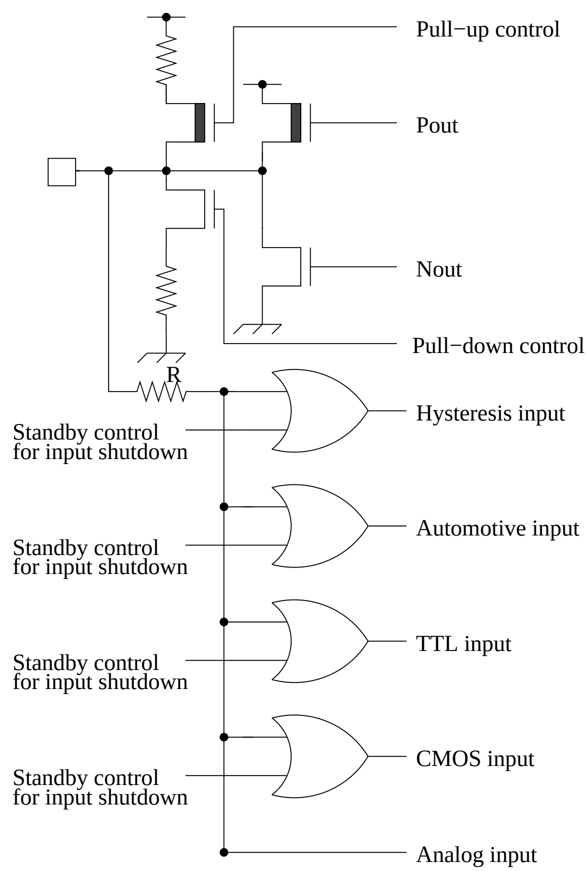
<table>
<tr><th>ODR[1:0]</th><th>I_{OL}</th><th>I_{OH}</th></tr>
<tr><td>00</td><td>+2mA</td><td>-2mA</td></tr>
<tr><td>01</td><td>+5mA</td><td>-5mA</td></tr>
<tr><td>10</td><td>+10mA</td><td>-10mA</td></tr>
<tr><td>11</td><td>+20mA</td><td>-20mA</td></tr>
</table>

■ Hysteresis input with input shutdown function

■ TTL input with input shutdown function

<table>
<tr><th>PIL</th><th>Input buffer</th><th>Levels</th></tr>
<tr><td>00</td><td>Hysteresis</td><td>20% / 80%</td></tr>
<tr><td>10</td><td>TTL</td><td>0.8V / 2V</td></tr>
</table>

■ Programmable pull-up and pull-down resistor: 33kΩ approx.

</td></tr>
<tr><td>SMC</td><td>
</td><td>

■ CMOS level output (programmable)

<table>
<tr><th>ODR[1:0]</th><th>I_{OL}</th><th>I_{OH}</th></tr>
<tr><td>00</td><td>+1mA</td><td>-1mA</td></tr>
<tr><td>01</td><td>+2mA</td><td>-2mA</td></tr>
<tr><td>10</td><td>+30mA</td><td>-30mA</td></tr>
<tr><td>11</td><td>+5mA</td><td>-5mA</td></tr>
</table>

■ Hysteresis input with input shutdown function

■ Automotive input with input shutdown function

■ TTL input with input shutdown function

■ CMOS input with input shutdown function

<table>
<tr><th>PIL</th><th>Input buffer</th><th>Levels</th></tr>
<tr><td>00</td><td>Hysteresis</td><td>20% / 80%</td></tr>
<tr><td>01</td><td>Automotive</td><td>50% / 80%</td></tr>
<tr><td>10</td><td>TTL</td><td>0.8V / 2V</td></tr>
<tr><td>11</td><td>CMOS</td><td>20% / 80%</td></tr>
</table>

■ Programmable pull-up resistor and pull down resistor: 50kΩ approx.

</td></tr>
</table>

Table 28. Modules with DMA (Continued)

DMA Request Number	DMA Request Name	DMA Request Description
244	PPG0DMA	Programmable Pulse Generator 0 DMA Request (PPG0_PCN:IRQF*)
245	PPG1DMA	Programmable Pulse Generator 1 DMA Request (PPG1_PCN:IRQF*)
246	PPG2DMA	Programmable Pulse Generator 2 DMA Request (PPG2_PCN:IRQF*)
247	PPG3DMA	Programmable Pulse Generator 3 DMA Request (PPG3_PCN:IRQF*)
248	PPG4DMA	Programmable Pulse Generator 4 DMA Request (PPG4_PCN:IRQF*)
249	PPG5DMA	Programmable Pulse Generator 5 DMA Request (PPG5_PCN:IRQF*)
250	PPG6DMA	Programmable Pulse Generator 6 DMA Request (PPG6_PCN:IRQF*)
251	PPG7DMA	Programmable Pulse Generator 7 DMA Request (PPG7_PCN:IRQF*)
252	PPG8DMA	Programmable Pulse Generator 8 DMA Request (PPG8_PCN:IRQF*)
253	PPG9DMA	Programmable Pulse Generator 9 DMA Request (PPG9_PCN:IRQF*)
254	PPG10DMA	Programmable Pulse Generator 10 DMA Request (PPG10_PCN:IRQF*)
255	PPG11DMA	Programmable Pulse Generator 11 DMA Request (PPG11_PCN:IRQF*)
256	PPG12DMA	Programmable Pulse Generator 12 DMA Request (PPG12_PCN:IRQF*)
257	PPG13DMA	Programmable Pulse Generator 13 DMA Request (PPG13_PCN:IRQF*)
258	PPG14DMA	Programmable Pulse Generator 14 DMA Request (PPG14_PCN:IRQF*)
259	PPG15DMA	Programmable Pulse Generator 15 DMA Request (PPG15_PCN:IRQF*)
308	PPG64DMA	Programmable Pulse Generator 64 DMA Request (PPG64_PCN:IRQF*)
309	PPG65DMA	Programmable Pulse Generator 65 DMA Request (PPG65_PCN:IRQF*)
310	PPG66DMA	Programmable Pulse Generator 66 DMA Request (PPG66_PCN:IRQF*)
311	PPG67DMA	Programmable Pulse Generator 67 DMA Request (PPG67_PCN:IRQF*)
312	PPG68DMA	Programmable Pulse Generator68 DMA Request (PPG68_PCN:IRQF*)
313	PPG69DMA	Programmable Pulse Generator 69 DMA Request (PPG69_PCN:IRQF*)
314	PPG70DMA	Programmable Pulse Generator 70 DMA Request (PPG70_PCN:IRQF*)
315	PPG71DMA	Programmable Pulse Generator 71 DMA Request (PPG71_PCN:IRQF*)
372	ADC0DMA	ADC0 Conversion End DMA Request (ADC0_CS1:INT* (end of conversion flag))
373	ADC0DMA2	ADC0 Scan End DMA Request (ADC0_CS3:INT2* (end of scan flag))
376	RLT0DMA	Reload Timer 0 DMA Request (RTL0_TMCSR:UF* (underflow flag))
377	RLT1DMA	Reload Timer 1 DMA Request (RTL1_TMCSR:UF* (underflow flag))
378	RLT2DMA	Reload Timer 2 DMA Request (RTL2_TMCSR:UF* (underflow flag))
379	RLT3DMA	Reload Timer 3 DMA Request (RTL3_TMCSR:UF* (underflow flag))
380	RLT4DMA	Reload Timer 4 DMA Request (RTL4_TMCSR:UF* (underflow flag))
381	RLT5DMA	Reload Timer 5 DMA Request (RTL5_TMCSR:UF* (underflow flag))
382	RLT6DMA	Reload Timer 6 DMA Request (RTL6_TMCSR:UF* (underflow flag))
383	RLT7DMA	Reload Timer 7 DMA Request (RTL7_TMCSR:UF* (underflow flag))
384	RLT8DMA	Reload Timer 8 DMA Request (RTL8_TMCSR:UF* (underflow flag))
385	RLT9DMA	Reload Timer 9 DMA Request (RTL9_TMCSR:UF* (underflow flag))
408	I2S0DMARX	I2S0 Receive DMA Request (I2S0_STATUS:RXFI* (receive FIFO full))
409	I2S0DMATX	I2S0 Transmit DMA Request (I2S0_STATUS:TXFI* (transmit FIFO empty))
410	I2S1DMARX	I2S0 Receive DMA Request (I2S1_STATUS:RXFI* (receive FIFO full))
411	I2S1DMATX	I2S0 Transmit DMA Request (I2S1_STATUS:TXFI* (transmit FIFO empty))

Table 32. Memory Layout of MEMORY_CONFIG Registers with Default Values (Continued)

Offset	+7	+6	+5	+4	+3	+2	+1	+0
0xB0400190	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400198	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB04001A0	IRQ0_IRQVA69 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB04001A8	IRQ0_IRQVA71 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA70 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001B0	IRQ0_IRQVA73 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA72 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001B8	IRQ0_IRQVA75 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA74 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001C0	IRQ0_IRQVA77 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA76 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001C8	IRQ0_IRQVA79 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA78 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001D0	IRQ0_IRQVA81 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA80 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001D8	IRQ0_IRQVA83 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA82 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001E0	IRQ0_IRQVA85 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA84 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001E8	IRQ0_IRQVA87 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA86 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001F0	IRQ0_IRQVA89 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA88 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001F8	IRQ0_IRQVA91 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA90 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400200	IRQ0_IRQVA93 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA92 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400208	IRQ0_IRQVA95 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA94 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400210	IRQ0_IRQVA97 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA96 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400218	IRQ0_IRQVA99 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA98 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400220	IRQ0_IRQVA101 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA100 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400228	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				IRQ0_IRQVA102 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400230	IRQ0_IRQVA105 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA104 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400238	IRQ0_IRQVA107 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA106 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400240	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400248	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400250	IRQ0_IRQVA113 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA112 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			

Table 35. Memory Layout of PERI0_RBUS Registers with Default Values (Continued)

Offset	+1	+0
0xB0700098	ADC0_PCTNRL2 00000000	ADC0_PCTPRL2 00000000
0xB070009A	ADC0_PCTNCT2 00000000	ADC0_PCTPCT2 00000000
0xB070009C	ADC0_PCTNRL3 00000000	ADC0_PCTPRL3 00000000
0xB070009E	ADC0_PCTNCT3 00000000	ADC0_PCTPCT3 00000000
0xB07000A0	ADC0_PCTNRL4 00000000	ADC0_PCTPRL4 00000000
0xB07000A2	ADC0_PCTNCT4 00000000	ADC0_PCTPCT4 00000000
0xB07000A4	ADC0_PCTNRL5 00000000	ADC0_PCTPRL5 00000000
0xB07000A6	ADC0_PCTNCT5 00000000	ADC0_PCTPCT5 00000000
0xB07000A8	ADC0_PCTNRL6 00000000	ADC0_PCTPRL6 00000000
0xB07000AA	ADC0_PCTNCT6 00000000	ADC0_PCTPCT6 00000000
0xB07000AC	ADC0_PCTNRL7 00000000	ADC0_PCTPRL7 00000000
0xB07000AE	ADC0_PCTNCT7 00000000	ADC0_PCTPCT7 00000000
0xB07000B0	ADC0_PCTNRL8 00000000	ADC0_PCTPRL8 00000000
0xB07000B2	ADC0_PCTNCT8 00000000	ADC0_PCTPCT8 00000000
0xB07000B4	ADC0_PCTNRL9 00000000	ADC0_PCTPRL9 00000000
0xB07000B6	ADC0_PCTNCT9 00000000	ADC0_PCTPCT9 00000000
0xB07000B8	ADC0_PCTNRL10 00000000	ADC0_PCTPRL10 00000000
0xB07000BA	ADC0_PCTNCT10 00000000	ADC0_PCTPCT10 00000000
0xB07000BC	ADC0_PCTNRL11 00000000	ADC0_PCTPRL11 00000000
0xB07000BE	ADC0_PCTNCT11 00000000	ADC0_PCTPCT11 00000000
0xB07000C0	ADC0_PCTNRL12 00000000	ADC0_PCTPRL12 00000000
0xB07000C2	ADC0_PCTNCT12 00000000	ADC0_PCTPCT12 00000000
0xB07000C4	ADC0_PCTNRL13 00000000	ADC0_PCTPRL13 00000000
0xB07000C6	ADC0_PCTNCT13 00000000	ADC0_PCTPCT13 00000000
0xB07000C8	ADC0_PCTNRL14 00000000	ADC0_PCTPRL14 00000000

Table 35. Memory Layout of PERI0_RBUS Registers with Default Values (Continued)

Offset	+1	+0
0xB0720002	I2C0_ITBA 00000000 00000000	
0xB0720004	I2C0_ITMK 00XXXX11 11111111	
0xB0720006	I2C0_ISBMA 01111111 00000000	
0xB0720008	reserved XXXXXXXX	I2C0_IODAR 00000000
0xB072000A	reserved XXXXXXXX	I2C0_ICCR 00111111
0xB072000C	I2C0_ICDIDAR 00000000 00000000	
0xB072000E	I2C0_IEICR 00000000 00000000	
0xB0720010	I2C0_DDMACFG 00000000 00000000	
0xB0720012	reserved XXXXXXXX	I2C0_IEIER 00000000
0xB0720014- B0727FFE	reserved XXXXXXXX XXXXXXXX	
0xB0728000	USART0_SCR 00000000	USART0_SMR 00000000
0xB0728002	USART0_SCSR 00000000	USART0_SMSR 00000000
0xB0728004	USART0_SCCR 00000000	reserved XXXXXXXX
0xB0728006	USART0_SSR 00001000	USART0_TDR 00000000
0xB0728008	USART0_SSSR 00000000	USART0_RDR 00000000
0xB072800A	USART0_SSCR 00000000	reserved XXXXXXXX
0xB072800C	USART0_ESCR 00000100	USART0_ECCR 000000XX
0xB072800E	USART0_ESCSR 00000000	USART0_ECCSR 00000000
0xB0728010	USART0_ESCCR 00000000	USART0_ECCCR 00000000
0xB0728012	USART0_EIER 00000000	USART0_ESIR 000010X0
0xB0728014	USART0_EIESR 00000000	USART0_ESISR 00000000
0xB0728016	USART0_EIECR 00000000	USART0_ESICR 00000000
0xB0728018	USART0_EFERH 00000000	USART0_EFERL 00000000
0xB072801A	USART0_TFCR 00000000	USART0_RFCR 00000000
0xB072801C	USART0_TFCSR 00000000	USART0_RFCSR 00000000

Table 36. Memory Layout of PERI1_RBUS Registers with Default Values (Continued)

Offset	+1	+0
0xB0849006	PPG68_RMPCFG 00000000	PPG68_OPTMSK 00000000
0xB0849008	PPG68_TRIGCLR 00000000	PPG68_STRD 00000000
0xB084900A	PPG68_EPCN1 00000000 00000000	
0xB084900C	PPG68_EPCN2 00000000 00000000	
0xB084900E	PPG68_GCN3 00000000	PPG68_GCN1 00000000
0xB0849010	PPG68_GCN5 00000000	PPG68_GCN4 00000110
0xB0849012	PPG68_PCSR XXXXXXXX XXXXXXXX	
0xB0849014	PPG68_PDUT XXXXXXXX XXXXXXXX	
0xB0849016	PPG68_PTMR 11111111 11111111	
0xB0849018	PPG68_PSDR 00000000 00000000	
0xB084901A	PPG68_PTPC 00000000 00000000	
0xB084901C	PPG68_PEDR 00000000 00000000	
0xB084901E	PPG68_DEBUG 00000000	PPG68_DMACFG 00000000
0xB0849020- B08493FE	reserved XXXXXXXX XXXXXXXX	
0xB0849400	PPG69_PCN 00000000 00000000	
0xB0849402	PPG69_SWTRIG 00000000	PPG69_IRQCLR 00000000
0xB0849404	PPG69_CNTEN 00000000	PPG69_OE 00000000
0xB0849406	PPG69_RMPCFG 00000000	PPG69_OPTMSK 00000000
0xB0849408	PPG69_TRIGCLR 00000000	PPG69_STRD 00000000
0xB084940A	PPG69_EPCN1 00000000 00000000	
0xB084940C	PPG69_EPCN2 00000000 00000000	
0xB084940E	PPG69_GCN3 00000000	PPG69_GCN1 00000000
0xB0849410	PPG69_GCN5 00000000	PPG69_GCN4 00000110
0xB0849412	PPG69_PCSR XXXXXXXX XXXXXXXX	
0xB0849414	PPG69_PDUT XXXXXXXX XXXXXXXX	
0xB0849416	PPG69_PTMR 11111111 11111111	

Table 36. Memory Layout of PERI1_RBUS Registers with Default Values (Continued)

Offset	+1	+0
0xB08F9066- B08F93FE	reserved XXXXXXXX 00000000	
0xB08F9400	RICFG1_OCU16OTD0GATE XXXXXXXX 00000000	
0xB08F9402	RICFG1_OCU16OTD0GM XXXXXXXX 00000000	
0xB08F9404	RICFG1_OCU16OTD1GATE XXXXXXXX 00000000	
0xB08F9406	RICFG1_OCU16OTD1GM XXXXXXXX 00000000	
0xB08F9408- B08F941E	reserved XXXXXXXX 00000000	
0xB08F9420	RICFG1_OCU17CMP0EXT XXXXXXXX 00000000	
0xB08F9422	RICFG1_OCU17FRTSEL XXXXXXXX 00000000	
0xB08F9424	RICFG1_OCU17OTD0GATE XXXXXXXX 00000000	
0xB08F9426	RICFG1_OCU17OTD0GM XXXXXXXX 00000000	
0xB08F9428	RICFG1_OCU17OTD1GATE XXXXXXXX 00000000	
0xB08F942A	RICFG1_OCU17OTD1GM XXXXXXXX 00000000	
0xB08F942C- B08F9BFE	reserved XXXXXXXX 00000000	
0xB08F9C00	RICFG1_USART6SCKI 00000000 XXXXXXXX	
0xB08F9C02	RICFG1_USART6SIN 00000000 XXXXXXXX	
0xB08F9C04- B08FA3FE	reserved XXXXXXXX 00000000	
0xB08FA400	RICFG1_PPG64PPGAGATE XXXXXXXX 00000000	
0xB08FA402	RICFG1_PPG64PPGAGM XXXXXXXX 00000000	
0xB08FA404	RICFG1_PPG64PPGBGATE XXXXXXXX 00000000	
0xB08FA406	RICFG1_PPG64PPGBGM XXXXXXXX 00000000	
0xB08FA408- B08FA41E	reserved XXXXXXXX 00000000	
0xB08FA420	RICFG1_PPG65PPGAGATE XXXXXXXX 00000000	
0xB08FA422	RICFG1_PPG65PPGAGM XXXXXXXX 00000000	
0xB08FA424	RICFG1_PPG65PPGBGATE XXXXXXXX 00000000	
0xB08FA426	RICFG1_PPG65PPGBGM XXXXXXXX 00000000	
0xB08FA428- B08FA43E	reserved XXXXXXXX 00000000	

Table 38. Memory Layout of PERI4_SLAVE Registers with Default Values (Continued)

Offset	+3	+2	+1	+0
0xB0B20404	I2S1_RXFDAT1 00000000 00000000 00000000 00000000			
0xB0B20408	I2S1_RXFDAT2 00000000 00000000 00000000 00000000			
0xB0B2040C	I2S1_RXFDAT3 00000000 00000000 00000000 00000000			
0xB0B20410	I2S1_RXFDAT4 00000000 00000000 00000000 00000000			
0xB0B20414	I2S1_RXFDAT5 00000000 00000000 00000000 00000000			
0xB0B20418	I2S1_RXFDAT6 00000000 00000000 00000000 00000000			
0xB0B2041C	I2S1_RXFDAT7 00000000 00000000 00000000 00000000			
0xB0B20420	I2S1_RXFDAT8 00000000 00000000 00000000 00000000			
0xB0B20424	I2S1_RXFDAT9 00000000 00000000 00000000 00000000			
0xB0B20428	I2S1_RXFDAT10 00000000 00000000 00000000 00000000			
0xB0B2042C	I2S1_RXFDAT11 00000000 00000000 00000000 00000000			
0xB0B20430	I2S1_RXFDAT12 00000000 00000000 00000000 00000000			
0xB0B20434	I2S1_RXFDAT13 00000000 00000000 00000000 00000000			
0xB0B20438	I2S1_RXFDAT14 00000000 00000000 00000000 00000000			
0xB0B2043C	I2S1_RXFDAT15 00000000 00000000 00000000 00000000			
0xB0B20440	I2S1_TXFDAT0 00000000 00000000 00000000 00000000			
0xB0B20444	I2S1_TXFDAT1 00000000 00000000 00000000 00000000			
0xB0B20448	I2S1_TXFDAT2 00000000 00000000 00000000 00000000			
0xB0B2044C	I2S1_TXFDAT3 00000000 00000000 00000000 00000000			
0xB0B20450	I2S1_TXFDAT4 00000000 00000000 00000000 00000000			
0xB0B20454	I2S1_TXFDAT5 00000000 00000000 00000000 00000000			
0xB0B20458	I2S1_TXFDAT6 00000000 00000000 00000000 00000000			
0xB0B2045C	I2S1_TXFDAT7 00000000 00000000 00000000 00000000			
0xB0B20460	I2S1_TXFDAT8 00000000 00000000 00000000 00000000			
0xB0B20464	I2S1_TXFDAT9 00000000 00000000 00000000 00000000			
0xB0B20468	I2S1_TXFDAT10 00000000 00000000 00000000 00000000			

Table 38. Memory Layout of PERI4_SLAVE Registers with Default Values (Continued)

Offset	+3	+2	+1	+0
0xB0BF9C28	read0 00000000 00000000		RICFG4_SPI1DATA1I 00000000 00000000	
0xB0BF9C2C	read0 00000000 00000000		RICFG4_SPI1MSTART 00000000 00000000	
0xB0BF9C30	read0 00000000 00000000		RICFG4_SPI1SSI 00000000 00000000	
0xB0BF9C34- B0BF9C3C	reserved 00000000 00000000 00000000 00000000			
0xB0BF9C40	read0 00000000 00000000		RICFG4_SPI2CLKI 00000000 00000000	
0xB0BF9C44	read0 00000000 00000000		RICFG4_SPI2DATA0I 00000000 00000000	
0xB0BF9C48	read0 00000000 00000000		RICFG4_SPI2DATA1I 00000000 00000000	
0xB0BF9C4C	read0 00000000 00000000		RICFG4_SPI2DATA2I 00000000 00000000	
0xB0BF9C50	read0 00000000 00000000		RICFG4_SPI2DATA3I 00000000 00000000	
0xB0BF9C54	read0 00000000 00000000		RICFG4_SPI2MSTART 00000000 00000000	
0xB0BF9C58	read0 00000000 00000000		RICFG4_SPI2SSI 00000000 00000000	
0xB0BF9C5C- B0BFFC00	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0BFFC04	BSU4_BTST 00000000 00000000 00000000 00000000			
0xB0BFFC08- B0BFFC10	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0BFFC14	BSU4_PEN1 00000000 00000000 00000000 00000000			
0xB0BFFC18	BSU4_PEN2 00000000 00000000 00000000 00000000			
0xB0BFFC1C	BSU4_PEN3 00000000 00000000 00000000 00000000			
0xB0BFFC20	BSU4_PEN4 00000000 00000000 00000000 00000000			
0xB0BFFC24	BSU4_PEN5 00000000 00000000 00000000 00000000			
0xB0BFFC28	BSU4_PEN6 00000000 00000000 00000000 00000000			
0xB0BFFC2C	BSU4_PEN7 00000000 00000000 00000000 00000000			
0xB0BFFC30	BSU4_PEN8 00000000 00000000 00000000 00000000			
0xB0BFFC34- B0BFFFFC	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

Table 39. Memory Layout of PERI5_AHB Registers with Default Values (Continued)

Offset	+3	+2	+1	+0
0xB0C0244C	DMA0_CMICIC267 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02450	DMA0_CMICIC268 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02454	DMA0_CMICIC269 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02458	DMA0_CMICIC270 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C0245C	DMA0_CMICIC271 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02460	DMA0_CMICIC272 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02464	DMA0_CMICIC273 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02468	DMA0_CMICIC274 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C0246C	DMA0_CMICIC275 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02470	DMA0_CMICIC276 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02474	DMA0_CMICIC277 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02478	DMA0_CMICIC278 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C0247C	DMA0_CMICIC279 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02480	DMA0_CMICIC280 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02484	DMA0_CMICIC281 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02488	DMA0_CMICIC282 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C0248C	DMA0_CMICIC283 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02490	DMA0_CMICIC284 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02494	DMA0_CMICIC285 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C02498	DMA0_CMICIC286 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C0249C	DMA0_CMICIC287 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C024A0	DMA0_CMICIC288 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C024A4	DMA0_CMICIC289 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C024A8	DMA0_CMICIC290 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C024AC	DMA0_CMICIC291 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C024B0	DMA0_CMICIC292 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			

Recommended Operating Conditions

Table 43. Recommended Operating Conditions

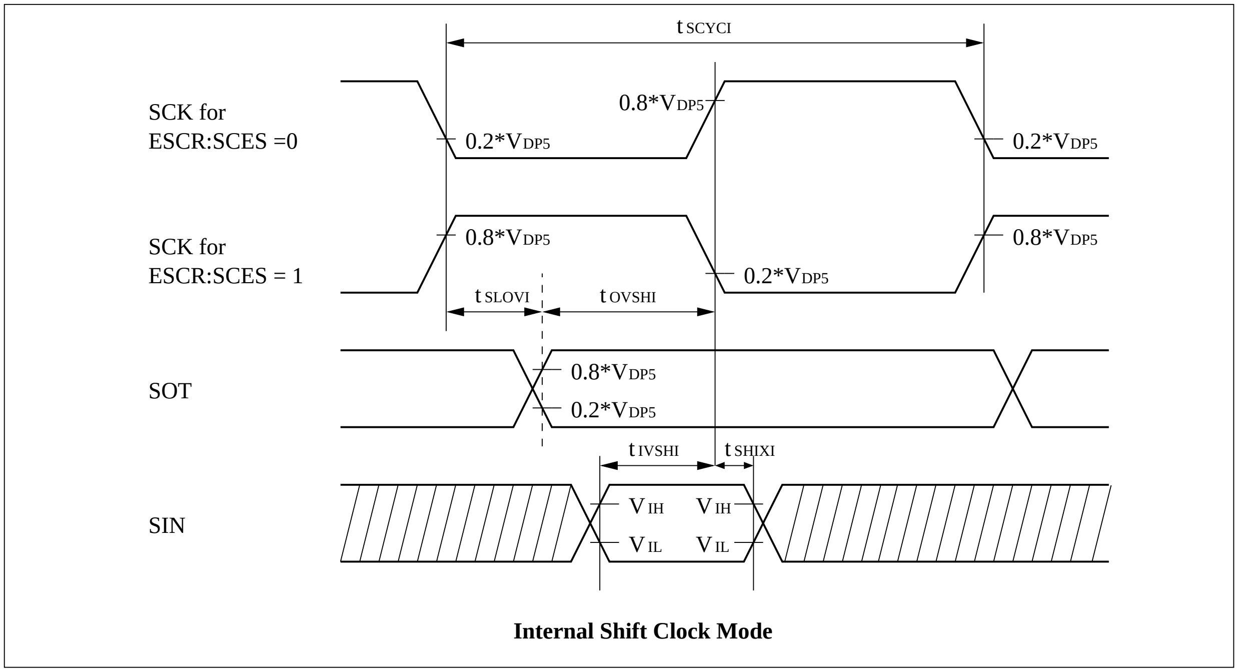
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
5V power supply voltage	V_{DP5}	3.0	3.3/5.0	5.5	V	
3.3V power supply voltage	V_{DP3}	3.0	3.3	3.6	V	
1.2V power supply voltage	V_{DD}	1.1	1.2	1.3	V	
SMC power supply voltage	DV_{CC}	4.5	5.0	5.5	V	If used as SMC
	DV_{CC}	3.0	3.3/5.0	5.5	V	If used as GPIO
Analog power supply voltage	AV_{DD5}	3.0	3.3/5.0	5.5	V	
AD Converter voltage reference	AV_{RH5}	AV_{DD5} - 0.5	-	AV_{DD5}	V	
Operation ambient temperature	T_{OP}	-40	-	105	°C	

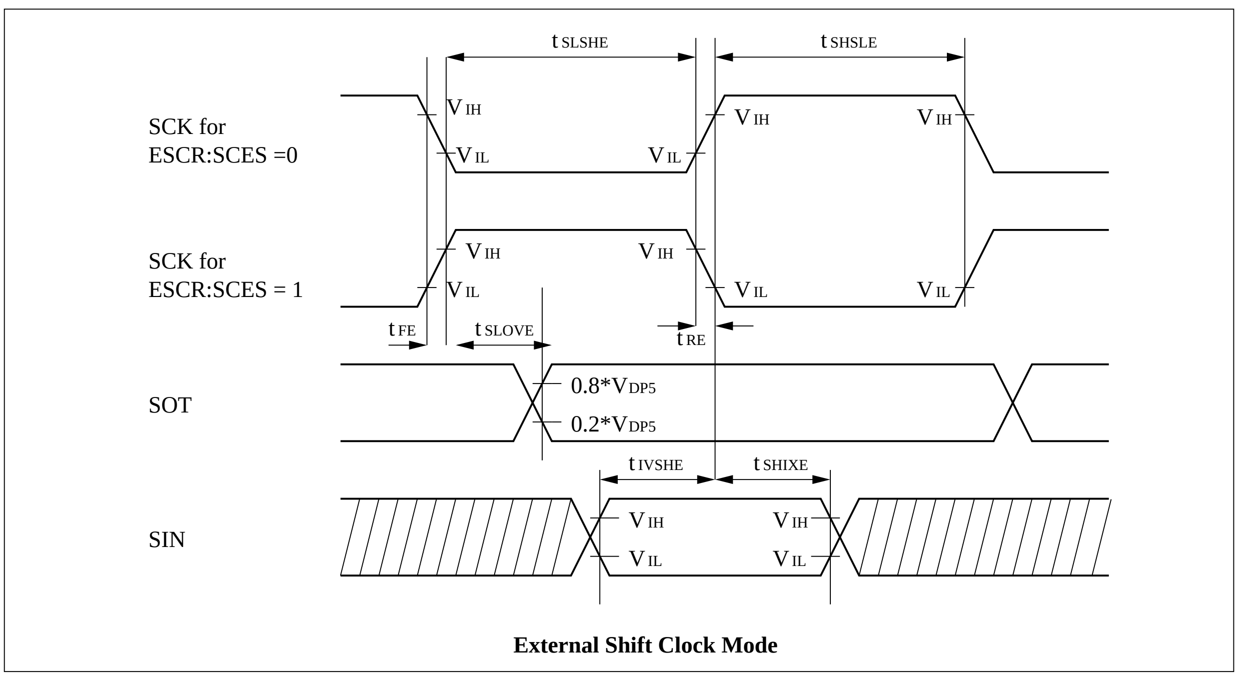
Warning: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the devices electrical characteristics are guaranteed when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operating outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Figure 9. USART Timing





I^2C Timing

(T_A = –40 °C to 105 °C, V_{DD} = 1.1V to 1.3V, V_{DP3} = 3.0V to 3.6V, V_{DP5} = AV_{DD5} = 4.5V to 5.5V[19], DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS5} = DV_{SS} = 0V)

Table 51. I^2C Timing

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}	4.0	-	0.6	-	µs
“L” width of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
“H” width of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}	4.7	-	0.6	-	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}	0	3.45	0	0.9	µs
Data set-up time SDA---↓→SCL↑¦¦-	t_{SUDAT}	250	-	100	-	ns
Set-up time for STOP condition SCL--↑→SDA-↑	t_{SUSTO}	4	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUS}	4.7	-	1.3	-	µs
Output fall time from 0.7*V_{DP5} to 0.3*V_{DP5} with a bus capacitance from 10pF to 400pF	t_{of}	20 + 0.1*C_b [21]	250	20 + 0.1*C_b [21]	250	ns
Capacitive load for each bus line	C_b	-	400	-	400	pF
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	n/a	n/a	0	1*$t_{CLK\_PERI0\_PD2}$[22]	ns

Notes

20.For use at over 100 kHz, set the CLK_PERI0_PD2 to at least 6 MHz.
21.C_b = capacitance of one bus line in pF.
22.$t_{CLK\_PERI0\_PD2}$ is the cycle time of the peripheral clock CLK_PERI0_PD2
23.I2C spec only guaranteed at VDP5 = 4.5V to 5.5V.

Figure 10. I2C Timing

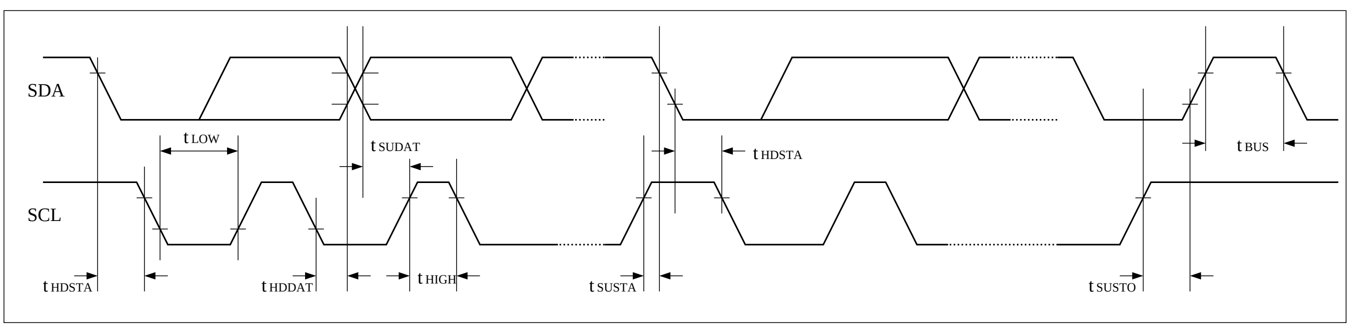


Table 53. HSSPI Interface Timing (Slave Mode)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
HSSPI clock frequency		-	-	25	MHz	
Input setup time (HSSPIn_DATAi)	$T_{IS,DATA}$	5	-	-	ns	
Input hold time (HSSPIn_DATAi)	$T_{IH,DATA}$	0	-	-	ns	
Input setup time (HSSPIn_SSELi)	$T_{IS,SSEL}$	8.2	-	-	ns	
Input hold time (HSSPIn_SSELi)	$T_{IH,SSEL}$	2	-	-	ns	
Output delay time (HSSPIn_-DATAo)	$T_{OD,DATA}$	-	-	15.5	ns	
Output hold time (HSSPIn_SSELo)	$T_{OH,DATA}$	0	-	-	ns	

SPI Timing

(T_A = –40 °C to 105 °C, V_{DD} = 1.1V to 1.3V, V_{DP3} = 3.0V to 3.6V, V_{DP5} = AV_{DD5} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V,

V_{SS} = AV_{SS5} = DV_{SS} = 0V)

For each SPI module, several combinations of I/O pins can be chosen for each SPI signal. The timing depends on the actual combination and is given below as separate values for each possible type of I/O-cell. When I/O/cells of different types are mixed, the worst case table, called “OVERALL SPI Interface timing” must be used.

In Master Mode, using the clock retiming function improves the setup and hold times for input data.

The usable maximum clock frequency depends on the transmission mode (Master to Slave / Slave to Master, using clock-retiming or not). An example for calculation is given below each table.

Table 54. OVERALL SPI Interface Timing

Parameter	Symbol	Master Mode, Non-retimed Clock		Master Mode, Retimed Clock		Slave Mode		Unit
		Min	Max	Min	Max	Min	Max	
Input setup time (SPIn_DATAi)	$T_{IS,DATA}$	24.9	-	9.9	-	9.8	-	ns
Input hold time (SPIn_DATAi)	$T_{IH,DATA}$	-6.1[24]	-	9.9	-	9.8	-	ns
Output delay time (SPIn_DATAo)	$T_{OD,DATA}$	-	12.2	-	12.2	-	41.5	ns
Output hold time (SPIn_DATAo)	$T_{OH,DATA}$	-5.3[24]	-	-5.3[24]	-	6.3	-	ns
Input setup time (SPIn_SSELi)	$T_{IS,SSEL}$	-	-	-	-	11.9	-	ns
Input hold time (SPIn_SSELi)	$T_{IH,SSEL}$	-	-	-	-	7.9	-	ns
Output delay time (SPIn_SSELo)	$T_{OD,SSEL}$	-	12.1	-	12.1	-	-	ns
Output hold time (SPIn_SSELo)	$T_{OH,SSEL}$	-4.6[24]	-	-4.6[24]	-	-	-	ns
Example for calculation of max. frequencies for communication of Master (retimed mode) and Slave:								
Transmission		Half Period Time				Max. Frequency		Unit
From Master to Slave		T/2 = $T_{OD,DATA}$ (Master) + $T_{IS,DATA}$ (Slave)				20.8		MHz
From Slave to Master		T/2 = $T_{OD,DATA}$ (Slave) + $T_{IS,DATA}$ (Master)				10.5		MHz

Note

24. A negative hold time implies that the clock edge output is delayed with respect to data output. In any case, an external device that will receive data, must use a sampling point that is outside the time interval given by Output hold time and Output delay time.

Table 66. Flash Pin Mapping to External Pins (Continued)

External Pin Number (QFP-176)	External Pin Name	Flash Macro Pin	Function
141	P0_43	EDIN[00]/EDOR[00]	Shared ECC data input/output Refer Section /
142	P0_44	EDIN[01]/EDOR[01]	
143	P0_45	EDIN[02]/EDOR[02]	
144	P0_46	EDIN[03]/EDOR[03]	
145	P0_47	EDIN[04]/EDOR[04]	
148	P0_48	EDIN[05]/EDOR[05]	
149	P0_49	EDIN[06]/EDOR[06]	
137	P0_41	ECCA	ECC write access enable 0: ECC write disable 1: ECC write enable
134	P0_24	RDYR	Internal voltage ready/busy flag at 5V 0: Busy 1: Ready
140	P0_42	RDY	FLASH internal state at PPROGRAM, ERASE and power on 0: busy 1: ready Output behaves as open drain (needs pull-up) to support programming multiple devices at once.
135	P0_25	RD64	64-bit read enable 0: 32-bit read mode 1: 64-bit read mode

■ **Parameters Affected**

All part numbers of the MBEF226 series are affected.

■ **Trigger Conditions**

1. Enabled IRQ[n] is selected for interrupt service (no other interrupt with higher priority pending and IRQ0_IRQPLn < IRQPLM) and IRQ0_IRQPLM is changed to equal or lower value than IRQ0_IRQPLn before IRQ0_IRQHS is set (point in time when CPU reads the interrupt vector address).
2. Priorities of active IRQ/NMI are changed during interrupt priority evaluation.
3. IRQ/NMI Hold Bit is cleared during interrupt priority evaluation.
4. IRQ0_IRQHC write access with 8-bit access width.

■ **Root Cause**

1. Not all inputs of priority encoder are latched during interrupt processing (period from start of priority evaluation until handover to CPU), in this case priority level mask IRQ0_IRQPLM.
2. Not all inputs of priority encoder are latched during interrupt processing (period from start of priority evaluation until handover to CPU), in this case priority level IRQ0_IRQPL0~127, resp. IRQ0_NMIPL0~7.
3. Not all inputs of priority encoder are latched during interrupt processing (period from start of priority evaluation until handover to CPU), in this case hold status IRQ0_IRQHS0~15 cleared by IRQ0_IRQHC, resp. IRQ0_NMIHS cleared by IRQ0_NMIHC.
4. Write strobes for the relevant 2 Bytes of IRQ0_IRQHC are evaluated by OR instead of AND which causes byte write access effects change on full 16 Bit.

■ **Workaround**

Refer to Workaround for IUNIT Interrupt Handling Problem on page 315.

■ **Fix Status**

Cypress is proposing software workaround specified in Workaround for IUNIT Interrupt Handling Problem on page 315. Hardware redesigns are not planned.

7. IUNIT Nesting Level Status Problem

■ **Description**

The IUNIT Nesting Level Status Register problem was found in the logic of the IUNIT on MBEF226 series. Because of this problem the IUNIT Nesting Level Status Register (IRQ0_NESTL) is not working as specified.

■ **Problem Conditions**

At least one of the following conditions must occur:

- Handover of IRQ vector address to CPU (by VIC protocol) and clearing of IRQ Hold status (by CPU executing ISR) occurs in the same clock cycle
- Handover of NMI vector address to CPU (by CPU reading the IRQ0_NMIVAS register) occurs one clock cycle before clearing of NMI Hold status (by CPU executing NMI handler).

■ **Affected Devices**

All part numbers of the MBEF226 series are affected.

■ **Root Cause**

IRQ0_NESTL:IRQNL:

If handover of IRQ vector address to CPU (by VIC protocol) and clearing of IRQ Hold status (by CPU executing ISR) occurs in the same clock cycle, then IRQ0_NESTL:IRQNL is incremented (if it is =0) or decremented (if it is !=0), but its value should not be changed.

IRQ0_NESTL:NMINL:

If handover of NMI vector address to CPU (by CPU reading the IRQ0_NMIVAS register) occurs one clock cycle before clearing of NMI Hold status (by CPU executing NMI handler) then IRQ0_NESTL:NMINL is incremented (if it is =0) or decremented (if it is !=0), but its value should not be changed.

■ **Workaround**

Do not evaluate the value returned by reading IUNIT Nesting Level Status Register (IRQ0_NESTL).

If software needs information about the current nesting level, a variable counter can be implemented which is incremented/decremented in the interrupt handler entry/exit code.

■ **Fix Status**

Cypress is proposing above software workaround. Hardware redesigns are not planned.

8. 1.2V LVD VDP3 Supply Problem

■ **Description**

The 1.2V Low Voltage Detection – VDP3 Supply problem was found in the MBEF226 series in the behavior of the 1.2V Low Voltage Detection (1.2V LVD, which is supervising the 1.2V core supply VDD) which is linked to the VDP3 supply voltage.

Because of this problem, the 1.2V LVD may not output power-good even if VDD supply is above set limit of LVD.

This may cause prevention of system startup after power-on and reset release and/or wrong 1.2V LVD behavior (Reset/Interrupt) at RUN and PSS mode.

■ **Problem Conditions**

The problem may occur at the following conditions:
- ❐ VDD is above set limits of 1.2V LVD (set by default to 0.8V lower limit at reset)
- ❐ 1.2V LVD is enabled (enabled by default at reset)
- ❐ VDP3 supply is smaller than 2.2V

■ **Affected Devices**

All part numbers of the MBEF226 series are affected.

■ **Root Cause**

The band-gap reference (BGR) of 1.2V LVD (supervising 1.2V core supply VDD) is connected to VDP3 supply.

If VDP3 supply is <2.2V then 1.2V LVD may not output power-good even if VDD supply is above set limit of LVD.

■ **Workaround**

Keep VDP3 supply ≥ 2.2V for correct operation of 1.2V LVD (at device startup and in RUN/PSS modes).

If 1.2V LVD is disabled at:
- ❐ RUN mode SYSC_RUNLVDCFGR. LVDE12 := 0, and
- ❐ PSS mode: SYSC_PSSLVDCFGR.LVDE12 := 0,

then VDP3 can be lower than 2.2V, but consider behavior as described in 3V IO Domain ESD Diode on page 292.

■ **Fix Status**

No fixes planned.

9. SHE AXI Master Address Mask Problem

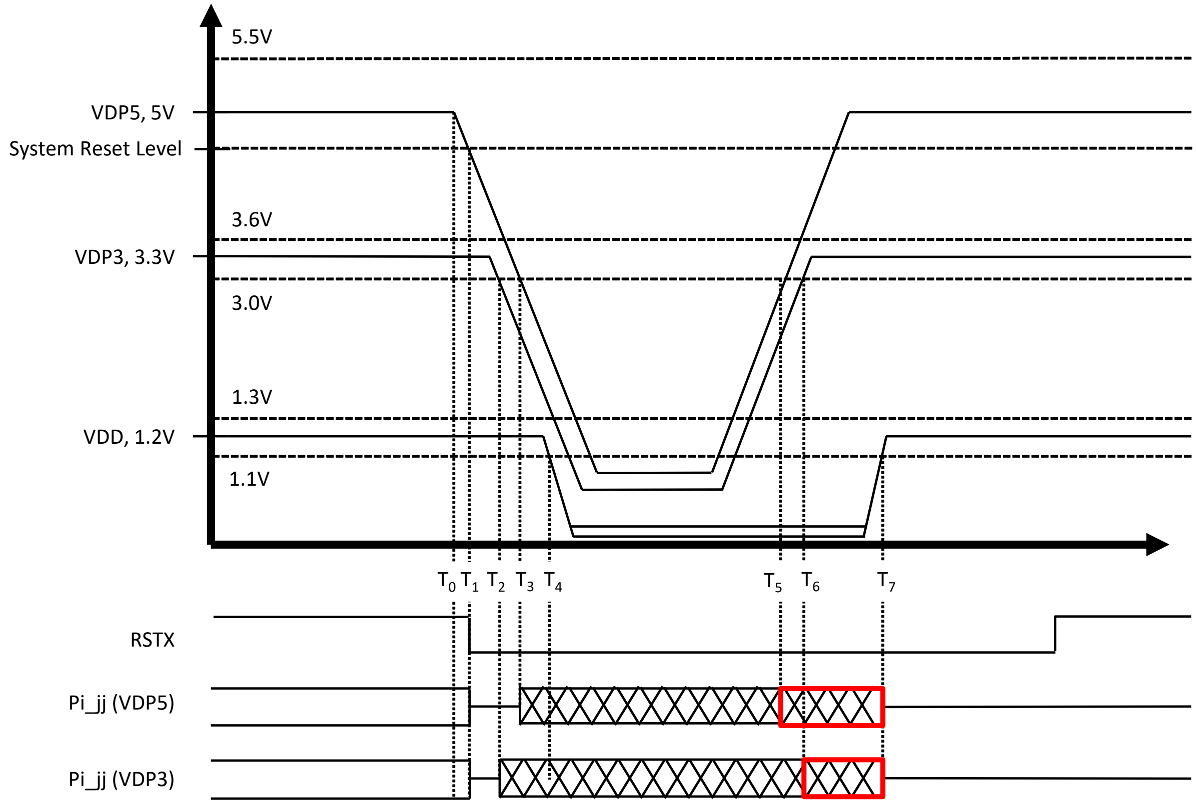
■**Problem Definition**

The SHE AXI Master Address Mask problem was found in the AXI Master Interface on the MB9EF226 series.
In case Input Channel Master is configured in a way the transfer will start in the address ranges:
- 0x00900000 - 0x009FFFFF
- 0x00FE0000 - 0x00FEFFFF

the first burst will be executed starting at the configured address. The transfer will continue after the completion of the first burst at address 0x00FF0000.
In case Input Channel Master is configured in a way the transfer will start in the address ranges
- 0x01100000 - 0x011FFFFF
- 0x017E0000 - 0x017EFFFF

the first burst will be executed starting at the configured address. The transfer will continue after the completion of the first burst at address 0x017F0000.
In case Input Channel Master is configured in a way the transfer will start outside the address ranges
- 0x00900000 - 0x009FFFFF
- 0x00FE0000 - 0x00FEFFFF

Figure 34. Undefined Port Pin Pi_jj State while VDP3/VDP5 is Powered, but VDD is not



Thereafter, also VDD is decreasing, being below the recommended operating conditions at T_4. If VDD is reaching a critical low value, the port pins Pi_jj enter undefined state. When VDP3 and VDP5 are rising again, the port pins Pi_jj remain in undefined state. At T_5 VDP5 is back in recommended operating conditions and at T_6 VDP3 is also back. Even though RSTX is still asserted, the port pins Pi_jj show the undefined state instead of the intended high-Z state. This failure case is indicated by the red rectangles.

Only when at T_7 VDD has reached a certain level (in this example: minimum value of recommended operating conditions) they are switched back to high-Z state caused by the still asserted RSTX.

Changed behavior of fixed devices in boundary scan test in user mode

Fixed devices behave differently in boundary scan test as described in following. If boundary scan test is enabled in user mode using a sequence of JTAG commands, then driving RSTX pin low during the boundary scan will force all output device pins to go to High-Z state. This also applies to the JTAG_TDO pin. Previously no output pin state change would have occurred.

Behavior of the boundary scan test if enabled through the board test mode (MODE pin = ‘1’) is not affected by the fix.

Multiple Analog Switches of SMC Port Pins in Conducting State

When the port pins Pi_jj enter undefined state as described above, also the states of the analog switches to connect the Stepper Motor Controller (SMC) port pins to the A/D converter may be undefined. Other A/D converter switches than the ones of the SMC IOs are not affected. As the state is undefined, several switches of the SMC port pins may be in the conducting state at once and create chip internal connections between the SMC port pins. Depending on the voltage levels on the SMC port pins, internal currents may flow.