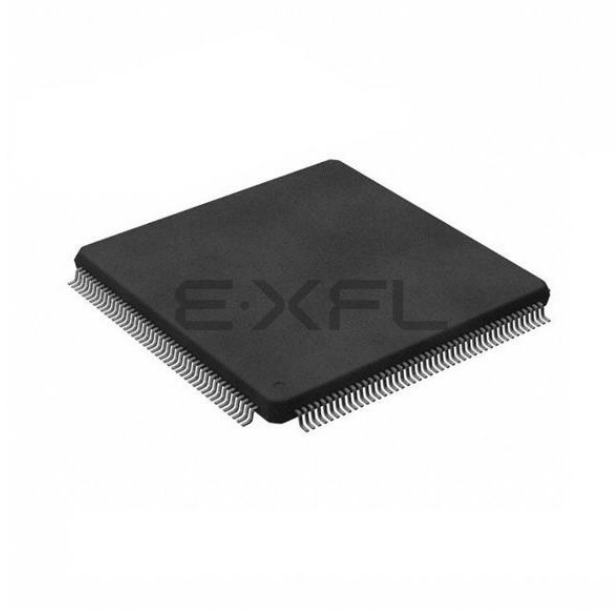

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-R4
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	117
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	208K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 5.5V
Data Converters	A/D 50x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9ef226lpmc-gsk5e2

Table 16. Port Multiplexing (Continued)

Register (Offset)	Resource Functional Output									Possible Resource Function Input
	Port	POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7	
PCFGR209 (0x0112)	P2_09	GPIO2_09o	GFX0_DISP9			PPG1_PPGB	OCU0_OTD1		PPG9_PPGA	GPIO2_09i, EIC0_INT30, FRT19_FRCK, ICU18_IN1
PCFGR210 (0x0114)	P2_10	GPIO2_10o	GFX0_DISP10			PPG2_PPGB	OCU1_OTD0		PPG10_PPGA	GPIO2_10i EIC0_INT31 FRT0_FRCK ICU19_IN0
PCFGR211 (0x0116)	P2_11	GPIO2_11o	GFX0_DISP11			PPG3_PPGB	OCU1_OTD1		PPG11_PPGA	GPIO2_11i, EIC0_INT14, FRT1_FRCK, ICU19_IN1
PCFGR212 (0x0118)	P2_12	GPIO2_12o	GFX0_DISP12			PPG4_PPGB	OCU16_OTD0		PPG12_PPGA	GPIO2_12i, EIC0_INT15, FRT2_FRCK, ICU2_IN0
PCFGR213 (0x011A)	P2_13	GPIO2_13o	GFX0_DISP13			PPG5_PPGB	OCU16_OTD1		PPG13_PPGA	GPIO2_13i, USART0_SIN, EIC0_INT11, EIC0_INT16, FRT3_FRCK, ICU2_IN1, RLT3_TIN
PCFGR214 (0x011C)	P2_14	GPIO2_14o	GFX0_DISP14		USART0_SCKo		OCU17_OTD0			GPIO2_14i, USART0_SCKi, EIC0_INT17, FRT16_FRCK, ICU3_IN0, RLT4_TIN
PCFGR215 (0x011E)	P2_15	GPIO2_15o	GFX0_DISP15		USART0_SOT		OCU17_OTD1			GPIO2_15i, EIC0_INT18, FRT17_FRCK, ICU3_IN1
PCFGR216 (0x0120)	P2_16	GPIO2_16o	GFX0_DISP16		OCU17_OTD0	PPG6_PPGB			PPG14_PPGA	GPIO2_16i, EIC0_INT19, FRT18_FRCK, ICU3_IN0
PCFGR217 (0x0122)	P2_17	GPIO2_17o	GFX0_DISP17		OCU17_OTD1	PPG7_PPGB			PPG15_PPGA	GPIO2_17i, EIC0_INT20, FRT19_FRCK, ICU3_IN1
PCFGR218 (0x0124)	P2_18	GPIO2_18o	GFX0_DISP18	SPI2_SSo				RLT0_TOT		GPIO2_18i, SPI2_SSi, EIC0_INT21, EIC0_INT05
PCFGR219 (0x0126)	P2_19	GPIO2_19o	GFX0_DISP19	SPI2_-DATA1o				RLT1_TOT		GPIO2_19i, SPI2_-DATA1i, EIC0_INT22
PCFGR220 (0x0128)	P2_20	GPIO2_20o	GFX0_DISP20	SPI2_-DATA0o	OCU0_OTD0	PPG64_PPGB		RLT2_TOT	PPG0_PPGA	GPIO2_20i, SPI2_-DATA0i, EIC0_INT23
PCFGR221 (0x012A)	P2_21	GPIO2_21o	GFX0_DISP21	SPI2_CLKo	OCU0_OTD1	PPG65_PPGB		RLT5_TOT	PPG1_PPGA	GPIO2_21i, SPI2_CLKi, EIC0_INT24, RLT2_TIN
PCFGR222 (0x012C)	P2_22	GPIO2_22o	GFX0_DISP22	SPI0_CLKo	OCU1_OTD0	PPG66_PPGB	SPI2_DATA2o		PPG2_PPGA	GPIO2_22i, SPI0_CLKi, SPI2_-DATA2i, EIC0_INT25, RLT0_TIN
PCFGR223 (0x012E)	P2_23	GPIO2_23o	GFX0_DISP23	SPI0_-DATA1o	OCU1_OTD1	PPG67_PPGB	SPI2_DATA3o	SPI2_SSO3	PPG3_PPGA	GPIO2_23i, SPI0_-DATA1i, SPI2_-DATA3i, EIC0_INT26, RLT1_TIN
PCFGR224 (0x0130)	P2_24	GPIO2_24o	GFX0_DISP24	SPI0_-DATA0o	OCU16_OTD0	PPG68_PPGB	SG0_SGO	SPI2_SSO2	PPG4_PPGA	GPIO2_24i, SPI0_-DATA0i, EIC0_INT27, ICU19_IN0, RLT2_TIN
PCFGR225 (0x0132)	P2_25	GPIO2_25o	GFX0_DISP25	SPI0_SSo	OCU16_OTD1	PPG69_PPGB	SG0_SGA	SPI2_SSO1	PPG5_PPGA	GPIO2_25i, SPI0_SSi, EIC0_INT28, EIC0_INT03, ICU19_IN1, RLT5_TIN

Table 18. RICFG0 (Continued)

Register	Resource Input	RESSEL[3:0]/ PORTSEL[3:0]	Source for Resource Input							
			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
PPG1PPGBGATE(0x1C24)	PPG1_PPGBGATE	RESSEL (0-7)	SPECIAL0_VDD	RLT1_TOT	RLT2_TOT	RLT3_TOT	RLT4_TOT	RLT5_TOT	RLT6_TOT	RLT7_TOT
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
PPG1PPGBGM(0x1C26)	PPG1_PPGBGM	RESSEL (0-7)	SPECIAL0_GND	SPECIAL0_VDD	reserved	reserved	reserved	reserved	reserved	reserved
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
PPG2PPGAGATE(0x1C40)	PPG2_PPGAGATE	RESSEL (0-7)	SPECIAL0_VDD	RLT1_TOT	RLT2_TOT	RLT3_TOT	RLT4_TOT	RLT5_TOT	RLT6_TOT	RLT7_TOT
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
PPG2PPGAGM(0x1C42)	PPG2_PPGAGM	RESSEL (0-7)	SPECIAL0_GND	SPECIAL0_VDD	reserved	reserved	reserved	reserved	reserved	reserved
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
PPG2PPGBGATE(0x1C44)	PPG2_PPGBGATE	RESSEL (0-7)	SPECIAL0_VDD	RLT1_TOT	RLT2_TOT	RLT3_TOT	RLT4_TOT	RLT5_TOT	RLT6_TOT	RLT7_TOT
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
PPG2PPGBGM(0x1C46)	PPG2_PPGBGM	RESSEL (0-7)	SPECIAL0_GND	SPECIAL0_VDD	reserved	reserved	reserved	reserved	reserved	reserved
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
PPG3PPGAGATE(0x1C60)	PPG3_PPGAGATE	RESSEL (0-7)	SPECIAL0_VDD	RLT1_TOT	RLT2_TOT	RLT3_TOT	RLT4_TOT	RLT5_TOT	RLT6_TOT	RLT7_TOT
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-
PPG3PPGAGM(0x1C62)	PPG3_PPGAGM	RESSEL (0-7)	SPECIAL0_GND	SPECIAL0_VDD	reserved	reserved	reserved	reserved	reserved	reserved
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	-	-	-	-	-	-	-	-
		PORTSEL (8-15)	-	-	-	-	-	-	-	-

Table 22. RICFG7 (Continued)

Register	Resource Input	RESSEL[3:0]/PORTSEL[3:0]	Source for Resource Input							
			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
			Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
EIC0INT08 (0x1020)	EIC0_INT08	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	reserved	P0_25	reserved	P0_42	P0_48	reserved	P1_34	P1_00
		PORTSEL (8-15)	P2_41	reserved	reserved	P2_48	P2_49	P2_50	reserved	reserved
EIC0INT09 (0x1024)	EIC0_INT09	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	reserved	P0_24	reserved	P0_43	P0_48	reserved	P1_36	P1_02
		PORTSEL (8-15)	P2_41	reserved	reserved	P2_49	P2_50	P2_51	reserved	reserved
EIC0INT10 (0x1028)	EIC0_INT10	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	reserved	P0_24	reserved	P0_42	P0_49	reserved	P1_38	P1_16
		PORTSEL (8-15)	P2_40	reserved	reserved	reserved	reserved	reserved	reserved	reserved
EIC0INT11 (0x102C)	EIC0_INT11	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	reserved	reserved	reserved	P0_40	P0_45	P1_30	P1_43	P0_42
		PORTSEL (8-15)	P1_08	reserved	reserved	reserved	P2_50	P2_13	reserved	reserved
EIC0INT12 (0x1030)	EIC0_INT12	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	reserved	reserved	reserved	P0_40	P0_45	P1_39	P0_47	P1_12
		PORTSEL (8-15)	reserved	reserved	reserved	P2_50	reserved	reserved	reserved	reserved
EIC0INT13 (0x1034)	EIC0_INT13	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	reserved	P1_37	P1_02	P1_16	reserved	reserved	reserved	reserved
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
EIC0INT14 (0x1038)	EIC0_INT14	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	reserved	reserved	P1_50	P1_17	P2_11	reserved	reserved	reserved
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
EIC0INT15 (0x103C)	EIC0_INT15	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	reserved	P0_41	P1_51	P1_18	P2_12	reserved	reserved	reserved
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
EIC0INT16 (0x1040)	EIC0_INT16	RESSEL (0-7)	-	-	-	-	-	-	-	-
		RESSEL (8-15)	-	-	-	-	-	-	-	-
		PORTSEL (0-7)	reserved	P0_46	P1_52	P1_19	P2_13	reserved	reserved	reserved
		PORTSEL (8-15)	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Table 26. Interrupt Table (Continued)

Interrupt Line Number	Interrupt Name	Interrupt Description
70	EIC0IRQ1	External Interrupt 1 (EIC0_EIRR:ER1 is set when an interrupt condition is detected at the corresponding input pin)
71	EIC0IRQ2	External Interrupt 2 (EIC0_EIRR:ER2 is set when an interrupt condition is detected at the corresponding input pin)
72	EIC0IRQ3	External Interrupt 3 (EIC0_EIRR:ER3 is set when an interrupt condition is detected at the corresponding input pin)
73	EIC0IRQ4	External Interrupt 4 (EIC0_EIRR:ER4 is set when an interrupt condition is detected at the corresponding input pin)
74	EIC0IRQ5	External Interrupt 5 (EIC0_EIRR:ER5 is set when an interrupt condition is detected at the corresponding input pin)
75	EIC0IRQ6	External Interrupt 6 (EIC0_EIRR:ER6 is set when an interrupt condition is detected at the corresponding input pin)
76	EIC0IRQ7	External Interrupt 7 (EIC0_EIRR:ER7 is set when an interrupt condition is detected at the corresponding input pin)
77	EIC0IRQ8	External Interrupt 8 (EIC0_EIRR:ER8 is set when an interrupt condition is detected at the corresponding input pin)
78	EIC0IRQ9	External Interrupt 9 (EIC0_EIRR:ER9 is set when an interrupt condition is detected at the corresponding input pin)
79	EIC0IRQ10	External Interrupt 10 (EIC0_EIRR:ER10 is set when an interrupt condition is detected at the corresponding input pin)
80	EIC0IRQ11	External Interrupt 11 (EIC0_EIRR:ER11 is set when an interrupt condition is detected at the corresponding input pin)
81	EIC0IRQ12	External Interrupt 12 (EIC0_EIRR:ER12 is set when an interrupt condition is detected at the corresponding input pin)
82	EIC0IRQ13	External Interrupt 13 (EIC0_EIRR:ER13 is set when an interrupt condition is detected at the corresponding input pin)
83	EIC0IRQ14	External Interrupt 14 (EIC0_EIRR:ER14 is set when an interrupt condition is detected at the corresponding input pin)
84	EIC0IRQ15	External Interrupt 15 (EIC0_EIRR:ER15 is set when an interrupt condition is detected at the corresponding input pin)
85	EIC0IRQ16	External Interrupt 16 (EIC0_EIRR:ER16 is set when an interrupt condition is detected at the corresponding input pin)
86	EIC0IRQ17	External Interrupt 17 (EIC0_EIRR:ER17 is set when an interrupt condition is detected at the corresponding input pin)
87	EIC0IRQ18	External Interrupt 18 (EIC0_EIRR:ER18 is set when an interrupt condition is detected at the corresponding input pin)
88	EIC0IRQ19	External Interrupt 19 (EIC0_EIRR:ER19 is set when an interrupt condition is detected at the corresponding input pin)
89	EIC0IRQ20	External Interrupt 20 (EIC0_EIRR:ER20 is set when an interrupt condition is detected at the corresponding input pin)
90	EIC0IRQ21	External Interrupt 21 (EIC0_EIRR:ER21 is set when an interrupt condition is detected at the corresponding input pin)
91	EIC0IRQ22	External Interrupt 22 (EIC0_EIRR:ER22 is set when an interrupt condition is detected at the corresponding input pin)
92	EIC0IRQ23	External Interrupt 23 (EIC0_EIRR:ER23 is set when an interrupt condition is detected at the corresponding input pin)
93	EIC0IRQ24	External Interrupt 24 (EIC0_EIRR:ER24 is set when an interrupt condition is detected at the corresponding input pin)
94	EIC0IRQ25	External Interrupt 25 (EIC0_EIRR:ER25 is set when an interrupt condition is detected at the corresponding input pin)
95	EIC0IRQ26	External Interrupt 26 (EIC0_EIRR:ER26 is set when an interrupt condition is detected at the corresponding input pin)
96	EIC0IRQ27	External Interrupt 27 (EIC0_EIRR:ER27 is set when an interrupt condition is detected at the corresponding input pin)
97	EIC0IRQ28	External Interrupt 28 (EIC0_EIRR:ER28 is set when an interrupt condition is detected at the corresponding input pin)
98	EIC0IRQ29	External Interrupt 29 (EIC0_EIRR:ER29 is set when an interrupt condition is detected at the corresponding input pin)
99	EIC0IRQ30	External Interrupt 30 (EIC0_EIRR:ER30 is set when an interrupt condition is detected at the corresponding input pin)
100	EIC0IRQ31	External Interrupt 31 (EIC0_EIRR:ER31 is set when an interrupt condition is detected at the corresponding input pin)
101	RTCIRQ	Real Time Clock Interrupt (check RTC_WINS:[6:0] for detailed Real Time Clock interrupt cause)
102	SG0IRQ	Sound Generator 0 Interrupt (SG0_CR1:ZAINT (zero amplitude interrupt), SG0_CR1:TCINT (tone pulse count interrupt), SG0_CR1:AMINT (amplitude match interrupt))
104	FRT0IRQ	Free Running Timer 0 Interrupt (FRT0_TCCS:IVF (compare clear match/counter overflow), FRT0_ETCCS:IRQZF (counter zero detection))
105	FRT1IRQ	Free Running Timer 1 Interrupt (FRT1_TCCS:IVF (compare clear match/counter overflow), FRT1_ETCCS:IRQZF (counter zero detection))
106	FRT2IRQ	Free Running Timer 2 Interrupt (FRT2_TCCS:IVF (compare clear match/counter overflow), FRT2_ETCCS:IRQZF (counter zero detection))
107	FRT3IRQ	Free Running Timer 3 Interrupt (FRT3_TCCS:IVF (compare clear match/counter overflow), FRT3_ETCCS:IRQZF (counter zero detection)

DMA Overview

Table 28. Modules with DMA

DMA Request Number	DMA Request Name	DMA Request Description
0	EXTDMA0	External DMA Request 0 (external pin DMA0_DREQ0)
1	EXTDMA1	External DMA Request 1 (external pin DMA0_DREQ0)
8	EIC0DMA0	External Interrupt 0 DMA Request (EIC0_DRFR:DRF0)
9	EIC0DMA1	External Interrupt 1 DMA Request (EIC0_DRFR:DRF1)
10	EIC0DMA2	External Interrupt 2 DMA Request (EIC0_DRFR:DRF2)
11	EIC0DMA3	External Interrupt 3 DMA Request (EIC0_DRFR:DRF3)
12	EIC0DMA4	External Interrupt 4 DMA Request (EIC0_DRFR:DRF4)
13	EIC0DMA5	External Interrupt 5 DMA Request (EIC0_DRFR:DRF5)
14	EIC0DMA6	External Interrupt 6 DMA Request (EIC0_DRFR:DRF6)
15	EIC0DMA7	External Interrupt 7 DMA Request (EIC0_DRFR:DRF7)
16	EIC0DMA8	External Interrupt 8 DMA Request (EIC0_DRFR:DRF8)
17	EIC0DMA9	External Interrupt 9 DMA Request (EIC0_DRFR:DRF9)
18	EIC0DMA10	External Interrupt 10 DMA Request (EIC0_DRFR:DRF10)
19	EIC0DMA11	External Interrupt 11 DMA Request (EIC0_DRFR:DRF11)
20	EIC0DMA12	External Interrupt 12 DMA Request (EIC0_DRFR:DRF12)
21	EIC0DMA13	External Interrupt 13 DMA Request (EIC0_DRFR:DRF13)
22	EIC0DMA14	External Interrupt 14 DMA Request (EIC0_DRFR:DRF14)
23	EIC0DMA15	External Interrupt 15 DMA Request (EIC0_DRFR:DRF15)
24	EIC0DMA16	External Interrupt 16 DMA Request(EIC0_DRFR:DRF16)
25	EIC0DMA17	External Interrupt 17 DMA Request (EIC0_DRFR:DRF17)
26	EIC0DMA18	External Interrupt 18 DMA Request (EIC0_DRFR:DRF18)
27	EIC0DMA19	External Interrupt 19 DMA Request (EIC0_DRFR:DRF19)
28	EIC0DMA20	External Interrupt 20 DMA Request (EIC0_DRFR:DRF20)
29	EIC0DMA21	External Interrupt 21 DMA Request (EIC0_DRFR:DRF21)
30	EIC0DMA22	External Interrupt 22 DMA Request (EIC0_DRFR:DRF22)
31	EIC0DMA23	External Interrupt 23 DMA Request (EIC0_DRFR:DRF23)
32	EIC0DMA24	External Interrupt 24 DMA Request (EIC0_DRFR:DRF24)
33	EIC0DMA25	External Interrupt 25 DMA Request (EIC0_DRFR:DRF25)
34	EIC0DMA26	External Interrupt 26 DMA Request (EIC0_DRFR:DRF26)
35	EIC0DMA27	External Interrupt 27 DMA Request (EIC0_DRFR:DRF27)
36	EIC0DMA28	External Interrupt 28 DMA Request (EIC0_DRFR:DRF28)
37	EIC0DMA29	External Interrupt 29 DMA Request (EIC0_DRFR:DRF29)
38	EIC0DMA30	External Interrupt 30 DMA Request (EIC0_DRFR:DRF30)
39	EIC0DMA31	External Interrupt 31 DMA Request (EIC0_DRFR:DRF31)
40	SG0DMA	Sound Generator 0 DMA Request (SG0_CR1:AMINT* (amplitude match flag) SG0_CR1:TCINT* (tone pulse count match flag) SG0_CR1:ZAINT* (zero amplitude flag))
44	HSSPI0DMARX	HSSPI0 Receive DMA Request (HSSPI0_RXF:RFMTS*(RX FIFO fill level more than threshold))

Table 32. Memory Layout of MEMORY_CONFIG Registers with Default Values (Continued)

Offset	+7	+6	+5	+4	+3	+2	+1	+0
0xB04008E8	IRQ0_IRQPL15 00000000 00011111 00011111 00000000				IRQ0_IRQPL14 00000000 00000000 00000000 00011111			
0xB04008F0	IRQ0_IRQPL17 00011111 00011111 00011111 00000000				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB04008F8	IRQ0_IRQPL19 00011111 00011111 00011111 00011111				IRQ0_IRQPL18 00011111 00011111 00011111 00011111			
0xB0400900	IRQ0_IRQPL21 00011111 00011111 00011111 00011111				IRQ0_IRQPL20 00011111 00011111 00011111 00011111			
0xB0400908	IRQ0_IRQPL23 00011111 00011111 00011111 00011111				IRQ0_IRQPL22 00011111 00011111 00011111 00011111			
0xB0400910	IRQ0_IRQPL25 00000000 00011111 00011111 00011111				IRQ0_IRQPL24 00011111 00011111 00011111 00011111			
0xB0400918	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				IRQ0_IRQPL26 00011111 00011111 00011111 00011111			
0xB0400920	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				IRQ0_IRQPL28 00011111 00011111 00011111 00011111			
0xB0400928	IRQ0_IRQPL31 00011111 00011111 00011111 00011111				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400930	IRQ0_IRQPL33 00011111 00011111 00011111 00011111				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400938	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				IRQ0_IRQPL34 00011111 00011111 00011111 00011111			
0xB0400940	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				IRQ0_IRQPL36 00011111 00011111 00011111 00011111			
0xB0400948	IRQ0_IRQPL39 00011111 00011111 00000000 00000000				IRQ0_IRQPL38 00000000 00011111 00011111 00011111			
0xB0400950	IRQ0_IRQPL41 00011111 00011111 00011111 00011111				IRQ0_IRQPL40 00000000 00000000 00000000 00011111			
0xB0400958	IRQ0_IRQPL43 00011111 00011111 00011111 00011111				IRQ0_IRQPL42 00011111 00011111 00011111 00011111			
0xB0400960	IRQ0_IRQPL45 00011111 00011111 00011111 00011111				IRQ0_IRQPL44 00011111 00011111 00011111 00011111			
0xB0400968	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				IRQ0_IRQPL46 00011111 00011111 00011111 00011111			
0xB0400970	IRQ0_IRQPL49 00011111 00011111 00000000 00000000				IRQ0_IRQPL48 00011111 00011111 00000000 00000000			
0xB0400978	IRQ0_IRQPL51 00000000 00011111 00000000 00000000				IRQ0_IRQPL50 00011111 00011111 00000000 00000000			
0xB0400980	IRQ0_IRQPL53 00011111 00011111 00011111 00011111				IRQ0_IRQPL52 00011111 00011111 00011111 00011111			
0xB0400988	IRQ0_IRQPL55 00011111 00011111 00011111 00011111				IRQ0_IRQPL54 00011111 00011111 00011111 00011111			
0xB0400990	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400998	IRQ0_IRQPL59 00011111 00011111 00011111 00011111				IRQ0_IRQPL58 00011111 00011111 00011111 00011111			
0xB04009A0 - 0xB0400AA8	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400AB0	IRQ0_NMIR 00000000 00000000 00000000 00000000				IRQ0_NMIS 00000000 00000000 00000000 00000000			

Table 32. Memory Layout of MEMORY_CONFIG Registers with Default Values (Continued)

Offset	+7	+6	+5	+4	+3	+2	+1	+0
0xB0400C48	read0 00000000 00000000 00000000 00000000				IRQ0_IRQHC 00000000 00000000 00000000 00000000			
0xB0400C50	IRQ0_IRQHS1 00000000 00000000 00000000 00000000				IRQ0_IRQHS0 00000000 00000000 00000000 00000000			
0xB0400C58	IRQ0_IRQHS3 00000000 00000000 00000000 00000000				IRQ0_IRQHS2 00000000 00000000 00000000 00000000			
0xB0400C60	IRQ0_IRQHS5 00000000 00000000 00000000 00000000				IRQ0_IRQHS4 00000000 00000000 00000000 00000000			
0xB0400C68	IRQ0_IRQHS7 00000000 00000000 00000000 00000000				IRQ0_IRQHS6 00000000 00000000 00000000 00000000			
0xB0400C70	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400C78	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400C80	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400C88	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400C90	read0 00000000 00000000 00000000 00000000				IRQ0_IRQPLM 00000000 00000000 00000000 00100000			
0xB0400C98	read0 00000000 00000000 00000000 00000000				IRQ0_CSR 00000000 00000001 00000000 00000000			
0xB0400CA0	read0 00000000 00000000 00000000 00000000				IRQ0_NESTL 00000000 00000000 00000000 00000000			
0xB0400CA8	IRQ0_NMIPS 00000000 00000000 00000000 00000000				IRQ0_NMIRS 00000000 00000000 00000000 00000000			
0xB0400CB0	IRQ0_IRQRS1 00000000 00000000 00000000 00000000				IRQ0_IRQRS0 00000000 00000000 00000000 00000000			
0xB0400CB8	IRQ0_IRQRS3 00000000 00000000 00000000 00000000				IRQ0_IRQRS2 00000000 00000000 00000000 00000000			
0xB0400CC0	IRQ0_IRQRS5 00000000 00000000 00000000 00000000				IRQ0_IRQRS4 00000000 00000000 00000000 00000000			
0xB0400CC8	IRQ0_IRQRS7 00000000 00000000 00000000 00000000				IRQ0_IRQRS6 00000000 00000000 00000000 00000000			
0xB0400CD0	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				read0 00000000 00000000 00000000 00000000			
0xB0400CD8	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400CE0	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400CE8	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400CF0	IRQ0_IRQPS1 00000000 00000000 00000000 00000000				IRQ0_IRQPS0 00000000 00000000 00000000 00000000			
0xB0400CF8	IRQ0_IRQPS3 00000000 00000000 00000000 00000000				IRQ0_IRQPS2 00000000 00000000 00000000 00000000			
0xB0400D00	IRQ0_IRQPS5 00000000 00000000 00000000 00000000				IRQ0_IRQPS4 00000000 00000000 00000000 00000000			
0xB0400D08	IRQ0_IRQPS7 00000000 00000000 00000000 00000000				IRQ0_IRQPS6 00000000 00000000 00000000 00000000			

Table 34. Memory Layout of MCU_CONFIG Registers with Default Values (Continued)

Offset	+3	+2	+1	+0
0xB0628020	EICU0_SPLR6 00000000 00000000 00000000 00000000			
0xB0628024	EICU0_SPLR7 00000000 00000000 00000000 00000000			
0xB0628028- B06F7FFC	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB06F8000	read0 00000000 00000000		RICFG7_GFX0DCLKI 00000000 00000000	
0xB06F8004- B06F8FFC	reserved 00000000 00000000 00000000 00000000			
0xB06F9000	read0 00000000 00000000		RICFG7_EIC0INT00 00000000 00000000	
0xB06F9004	read0 00000000 00000000		RICFG7_EIC0INT01 00000000 00000000	
0xB06F9008	read0 00000000 00000000		RICFG7_EIC0INT02 00000000 00000000	
0xB06F900C	read0 00000000 00000000		RICFG7_EIC0INT03 00000000 00000000	
0xB06F9010	read0 00000000 00000000		RICFG7_EIC0INT04 00000000 00000000	
0xB06F9014	read0 00000000 00000000		RICFG7_EIC0INT05 00000000 00000000	
0xB06F9018	read0 00000000 00000000		RICFG7_EIC0INT06 00000000 00000000	
0xB06F901C	read0 00000000 00000000		RICFG7_EIC0INT07 00000000 00000000	
0xB06F9020	read0 00000000 00000000		RICFG7_EIC0INT08 00000000 00000000	
0xB06F9024	read0 00000000 00000000		RICFG7_EIC0INT09 00000000 00000000	
0xB06F9028	read0 00000000 00000000		RICFG7_EIC0INT10 00000000 00000000	
0xB06F902C	read0 00000000 00000000		RICFG7_EIC0INT11 00000000 00000000	
0xB06F9030	read0 00000000 00000000		RICFG7_EIC0INT12 00000000 00000000	
0xB06F9034	read0 00000000 00000000		RICFG7_EIC0INT13 00000000 00000000	
0xB06F9038	read0 00000000 00000000		RICFG7_EIC0INT14 00000000 00000000	
0xB06F903C	read0 00000000 00000000		RICFG7_EIC0INT15 00000000 00000000	
0xB06F9040	read0 00000000 00000000		RICFG7_EIC0INT16 00000000 00000000	
0xB06F9044	read0 00000000 00000000		RICFG7_EIC0INT17 00000000 00000000	
0xB06F9048	read0 00000000 00000000		RICFG7_EIC0INT18 00000000 00000000	
0xB06F904C	read0 00000000 00000000		RICFG7_EIC0INT19 00000000 00000000	

Table 35. Memory Layout of PERI0_RBUS Registers with Default Values (Continued)

Offset	+1	+0
0xB0720002	I2C0_ITBA 00000000 00000000	
0xB0720004	I2C0_ITMK 00XXXX11 11111111	
0xB0720006	I2C0_ISBMA 01111111 00000000	
0xB0720008	reserved XXXXXXXX	I2C0_IODAR 00000000
0xB072000A	reserved XXXXXXXX	I2C0_ICCR 00111111
0xB072000C	I2C0_ICDIDAR 00000000 00000000	
0xB072000E	I2C0_IEICR 00000000 00000000	
0xB0720010	I2C0_DDMACFG 00000000 00000000	
0xB0720012	reserved XXXXXXXX	I2C0_IEIER 00000000
0xB0720014- B0727FFE	reserved XXXXXXXX XXXXXXXX	
0xB0728000	USART0_SCR 00000000	USART0_SMR 00000000
0xB0728002	USART0_SCSR 00000000	USART0_SMSR 00000000
0xB0728004	USART0_SCCR 00000000	reserved XXXXXXXX
0xB0728006	USART0_SSR 00001000	USART0_TDR 00000000
0xB0728008	USART0_SSSR 00000000	USART0_RDR 00000000
0xB072800A	USART0_SSCR 00000000	reserved XXXXXXXX
0xB072800C	USART0_ESCR 00000100	USART0_ECCR 000000XX
0xB072800E	USART0_ESCSR 00000000	USART0_ECCSR 00000000
0xB0728010	USART0_ESCCR 00000000	USART0_ECCCR 00000000
0xB0728012	USART0_EIER 00000000	USART0_ESIR 000010X0
0xB0728014	USART0_EIESR 00000000	USART0_ESISR 00000000
0xB0728016	USART0_EIECR 00000000	USART0_ESICR 00000000
0xB0728018	USART0_EFERH 00000000	USART0_EFERL 00000000
0xB072801A	USART0_TFCR 00000000	USART0_RFCR 00000000
0xB072801C	USART0_TFCSR 00000000	USART0_RFCSR 00000000

Table 35. Memory Layout of PERI0_RBUS Registers with Default Values (Continued)

Offset	+1	+0
0xB073840C	PPG1_EPCN2 00000000 00000000	
0xB073840E	PPG1_GCN3 00000000	PPG1_GCN1 00000000
0xB0738410	PPG1_GCN5 00000000	PPG1_GCN4 00000110
0xB0738412	PPG1_PCSR XXXXXXXX XXXXXXXX	
0xB0738414	PPG1_PDUT XXXXXXXX XXXXXXXX	
0xB0738416	PPG1_PTMR 11111111 11111111	
0xB0738418	PPG1_PSDR 00000000 00000000	
0xB073841A	PPG1_PTPC 00000000 00000000	
0xB073841C	PPG1_PEDR 00000000 00000000	
0xB073841E	PPG1_DEBUG 00000000	PPG1_DMACFG 00000000
0xB0738420- B07387FE	reserved XXXXXXXX XXXXXXXX	
0xB0738800	PPG2_PCN 00000000 00000000	
0xB0738802	PPG2_SWTRIG 00000000	PPG2_IRQCLR 00000000
0xB0738804	PPG2_CNTEN 00000000	PPG2_OE 00000000
0xB0738806	PPG2_RMPCFG 00000000	PPG2_OPTMSK 00000000
0xB0738808	PPG2_TRIGCLR 00000000	PPG2_STRD 00000000
0xB073880A	PPG2_EPCN1 00000000 00000000	
0xB073880C	PPG2_EPCN2 00000000 00000000	
0xB073880E	PPG2_GCN3 00000000	PPG2_GCN1 00000000
0xB0738810	PPG2_GCN5 00000000	PPG2_GCN4 00000110
0xB0738812	PPG2_PCSR XXXXXXXX XXXXXXXX	
0xB0738814	PPG2_PDUT XXXXXXXX XXXXXXXX	
0xB0738816	PPG2_PTMR 11111111 11111111	
0xB0738818	PPG2_PSDR 00000000 00000000	
0xB073881A	PPG2_PTPC 00000000 00000000	
0xB073881C	PPG2_PEDR 00000000 00000000	

Table 35. Memory Layout of PERI0_RBUS Registers with Default Values (Continued)

Offset	+1	+0
0xB07E81D6	PPC_PCFGR343 0XX00000 00000000	
0xB07E81D8	PPC_PCFGR344 0XX00000 00000000	
0xB07E81DA	PPC_PCFGR345 0XX00000 00000000	
0xB07E81DC	PPC_PCFGR346 0XX00000 00000000	
0xB07E81DE	PPC_PCFGR347 0XX00000 00000000	
0xB07E81E0	PPC_PCFGR348 0XX00000 00000000	
0xB07E81E2	PPC_PCFGR349 0XX00000 00000000	
0xB07E81E4	PPC_PCFGR350 0XX00000 00000000	
0xB07E81E6	PPC_PCFGR351 0XX00000 00000000	
0xB07E81E8	PPC_PCFGR352 0XX00000 00000000	
0xB07E81EA	PPC_PCFGR353 0XX00000 00000000	
0xB07E81EC	PPC_PCFGR354 0XX00000 00000000	
0xB07E81EE	PPC_PCFGR355 0XX00000 00000000	
0xB07E81F0	PPC_PCFGR356 0XX00000 00000000	
0xB07E81F2	PPC_PCFGR357 0XX00000 00000000	
0xB07E81F4	PPC_PCFGR358 0XX00000 00000000	
0xB07E81F6	PPC_PCFGR359 0XX00000 00000000	
0xB07E81F8	PPC_PCFGR360 0XX00000 00000000	
0xB07E81FA	PPC_PCFGR361 0XX00000 00000000	
0xB07E81FC	PPC_PCFGR362 0XX00000 00000000	
0xB07E81FE	PPC_PCFGR363 0XX00000 00000000	
0xB07E8200- B07EFFFE	reserved XXXXXXXX XXXXXXXX	
0xB07F0000	BECU0_CTRL 00000000 00000000	
0xB07F0002	BECU0_CTRH 00000000 00000000	
0xB07F0004	BECU0_ADDRL 00000000 00000000	
0xB07F0006	BECU0_ADDRH 00000000 00000000	

Table 36. Memory Layout of PERI1_RBUS Registers with Default Values (Continued)

Offset	+1	+0
0xB080801C	CAN0_IF1MCTR 00000000 0XXX0000	
0xB080801E	reserved XXXXXXXX XXXXXXXX	
0xB0808020	CAN0_IF1DTA1 00000000 00000000	
0xB0808022	CAN0_IF1DTA2 00000000 00000000	
0xB0808024	CAN0_IF1DTB1 00000000 00000000	
0xB0808026	CAN0_IF1DTB2 00000000 00000000	
0xB0808028- B080803E	reserved XXXXXXXX XXXXXXXX	
0xB0808040	CAN0_IF2CREQ 0XXXXXXX 00000001	
0xB0808042	CAN0_IF2CMSK XXXXXXXX 00000000	
0xB0808044	CAN0_IF2MSK1 11111111 11111111	
0xB0808046	CAN0_IF2MSK2 11X11111 11111111	
0xB0808048	CAN0_IF2ARB1 00000000 00000000	
0xB080804A	CAN0_IF2ARB2 00000000 00000000	
0xB080804C	CAN0_IF2MCTR 00000000 00000000	
0xB080804E	reserved XXXXXXXX XXXXXXXX	
0xB0808050	CAN0_IF2DTA1 00000000 00000000	
0xB0808052	CAN0_IF2DTA2 00000000 00000000	
0xB0808054	CAN0_IF2DTB1 00000000 00000000	
0xB0808056	CAN0_IF2DTB2 00000000 00000000	
0xB0808058- B080807E	reserved XXXXXXXX XXXXXXXX	
0xB0808080	CAN0_TREQR1 00000000 00000000	
0xB0808082	CAN0_TREQR2 00000000 00000000	
0xB0808084	CAN0_TREQR3 00000000 00000000	
0xB0808086	CAN0_TREQR4 00000000 00000000	
0xB0808088- B080808E	reserved XXXXXXXX XXXXXXXX	
0xB0808090	CAN0_NEWDT1 00000000 00000000	

Table 36. Memory Layout of PERI1_RBUS Registers with Default Values (Continued)

Offset	+1	+0
0xB08FFC1E	reserved XXXXXXXX XXXXXXXX	
0xB08FFC20	BSU1_PEN4L 00000000 00000000	
0xB08FFC22	reserved XXXXXXXX XXXXXXXX	
0xB08FFC24	BSU1_PEN5L 00000000 00000000	
0xB08FFC26	reserved XXXXXXXX XXXXXXXX	
0xB08FFC28	BSU1_PEN6L XXXXXXXX 00000000	
0xB08FFC2A	reserved XXXXXXXX XXXXXXXX	
0xB08FFC2C	BSU1_PEN7L XXXXXXXX 00000000	
0xB08FFC2E	reserved XXXXXXXX XXXXXXXX	
0xB08FFC30	BSU1_PEN8L XXXXXXXX 00000000	
0xB08FFC32	reserved XXXXXXXX XXXXXXXX	
0xB08FFC34	BSU1_PEN9L 00000000 00000000	
0xB08FFC36	BSU1_PEN9H 00000000 00000000	
0xB08FFC38	BSU1_PEN10L 00000000 00000000	
0xB08FFC3A	BSU1_PEN10H 00000000 00000000	
0xB08FFC3C	BSU1_PEN11L 00000000 00000000	
0xB08FFC3E	BSU1_PEN11H XXXXXXXX 00000000	
0xB08FFC40- B09FFFFE	reserved XXXXXXXX XXXXXXXX	

Table 38. Memory Layout of PERI4_SLAVE Registers with Default Values (Continued)

Offset	+3	+2	+1	+0
0xB0B2004C	I2S0_TXFDAT3 00000000 00000000 00000000 00000000			
0xB0B20050	I2S0_TXFDAT4 00000000 00000000 00000000 00000000			
0xB0B20054	I2S0_TXFDAT5 00000000 00000000 00000000 00000000			
0xB0B20058	I2S0_TXFDAT6 00000000 00000000 00000000 00000000			
0xB0B2005C	I2S0_TXFDAT7 00000000 00000000 00000000 00000000			
0xB0B20060	I2S0_TXFDAT8 00000000 00000000 00000000 00000000			
0xB0B20064	I2S0_TXFDAT9 00000000 00000000 00000000 00000000			
0xB0B20068	I2S0_TXFDAT10 00000000 00000000 00000000 00000000			
0xB0B2006C	I2S0_TXFDAT11 00000000 00000000 00000000 00000000			
0xB0B20070	I2S0_TXFDAT12 00000000 00000000 00000000 00000000			
0xB0B20074	I2S0_TXFDAT13 00000000 00000000 00000000 00000000			
0xB0B20078	I2S0_TXFDAT14 00000000 00000000 00000000 00000000			
0xB0B2007C	I2S0_TXFDAT15 00000000 00000000 00000000 00000000			
0xB0B20080	I2S0_CNTREG 00000000 00000000 00000000 01100000			
0xB0B20084	I2S0_MCR0REG 00000000 00000000 00000000 00000000			
0xB0B20088	I2S0_MCR1REG 00000000 00000000 00000000 00000000			
0xB0B2008C	I2S0_MCR2REG 00000000 00000000 00000000 00000000			
0xB0B20090	I2S0_OPRREG 00000000 00000000 00000000 00000000			
0xB0B20094	I2S0_SRST 00000000 00000000 00000000 00000000			
0xB0B20098	I2S0_INTCNT 01111111 00111111 00000000 00000000			
0xB0B2009C	I2S0_STATUS 00000000 00000000 00000000 00000000			
0xB0B200A0	I2S0_DMAACT 00000000 00000000 00000000 00000000			
0xB0B200A4	I2S0_DEBUG 00000000 00000000 00000000 00000000			
0xB0B200A8	I2S0_MIDREG 00000000 00000000 00000000 00000000			
0xB0B200AC- B0B203FC	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0B20400	I2S1_RXFDAT0 00000000 00000000 00000000 00000000			

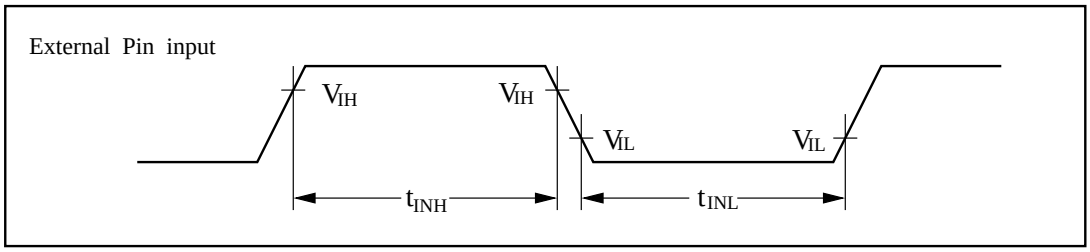
Table 39. Memory Layout of PERI5_AHB Registers with Default Values (Continued)

Offset	+3	+2	+1	+0
0xB0C00E5C	DMA0_DASHDW57 00000000 00000000 00000000 00000000			
0xB0C00E60- B0C00E7C	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C00E80	DMA0_A58 00000000 00001111 00000000 00000000			
0xB0C00E84	DMA0_B58 00000000 00000000 00110011 01111111			
0xB0C00E88	DMA0_SA58 00000000 00000000 00000000 00000000			
0xB0C00E8C	DMA0_DA58 00000000 00000000 00000000 00000000			
0xB0C00E90	DMA0_C58 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C00E94	DMA0_D58 00000000 XXXXXXXX 00000000 XXXXXXXX			
0xB0C00E98	DMA0_SASHDW58 00000000 00000000 00000000 00000000			
0xB0C00E9C	DMA0_DASHDW58 00000000 00000000 00000000 00000000			
0xB0C00EA0- B0C00EBC	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C00EC0	DMA0_A59 00000000 00001111 00000000 00000000			
0xB0C00EC4	DMA0_B59 00000000 00000000 00110011 01111111			
0xB0C00EC8	DMA0_SA59 00000000 00000000 00000000 00000000			
0xB0C00ECC	DMA0_DA59 00000000 00000000 00000000 00000000			
0xB0C00ED0	DMA0_C59 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C00ED4	DMA0_D59 00000000 XXXXXXXX 00000000 XXXXXXXX			
0xB0C00ED8	DMA0_SASHDW59 00000000 00000000 00000000 00000000			
0xB0C00EDC	DMA0_DASHDW59 00000000 00000000 00000000 00000000			
0xB0C00EE0- B0C00EFC	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C00F00	DMA0_A60 00000000 00001111 00000000 00000000			
0xB0C00F04	DMA0_B60 00000000 00000000 00110011 01111111			
0xB0C00F08	DMA0_SA60 00000000 00000000 00000000 00000000			
0xB0C00F0C	DMA0_DA60 00000000 00000000 00000000 00000000			
0xB0C00F10	DMA0_C60 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C00F14	DMA0_D60 00000000 XXXXXXXX 00000000 XXXXXXXX			

Table 39. Memory Layout of PERI5_AHB Registers with Default Values (Continued)

Offset	+3	+2	+1	+0
0xB0C08028	MPUXDMA0_SADDR2 00000000 00000000 00000000 00000000			
0xB0C0802C	MPUXDMA0_EADDR2 00000000 00000000 00000000 01111111			
0xB0C08030	MPUXDMA0_CTRL3 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C08034	MPUXDMA0_SADDR3 00000000 00000000 00000000 00000000			
0xB0C08038	MPUXDMA0_EADDR3 00000000 00000000 00000000 01111111			
0xB0C0803C	MPUXDMA0_CTRL4 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C08040	MPUXDMA0_SADDR4 00000000 00000000 00000000 00000000			
0xB0C08044	MPUXDMA0_EADDR4 00000000 00000000 00000000 01111111			
0xB0C08048	MPUXDMA0_CTRL5 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C0804C	MPUXDMA0_SADDR5 00000000 00000000 00000000 00000000			
0xB0C08050	MPUXDMA0_EADDR5 00000000 00000000 00000000 01111111			
0xB0C08054	MPUXDMA0_CTRL6 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C08058	MPUXDMA0_SADDR6 00000000 00000000 00000000 00000000			
0xB0C0805C	MPUXDMA0_EADDR6 00000000 00000000 00000000 01111111			
0xB0C08060	MPUXDMA0_CTRL7 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C08064	MPUXDMA0_SADDR7 00000000 00000000 00000000 00000000			
0xB0C08068	MPUXDMA0_EADDR7 00000000 00000000 00000000 01111111			
0xB0C0806C	MPUXDMA0_CTRL8 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C08070	MPUXDMA0_SADDR8 00000000 00000000 00000000 00000000			
0xB0C08074	MPUXDMA0_EADDR8 00000000 00000000 00000000 01111111			
0xB0C08078	MPUXDMA0_UNLOCK 00000000 00000000 00000000 00000000			
0xB0C0807C	MPUXDMA0_MID 00000000 00000000 00000000 00000000			
0xB0C08080- B0CFFC00	reserved XXXXXXXX XXXXXXXX XXXXXXXX 0000000X			
0xB0CFFC04	BSU5_BTST 00000000 00000000 00000000 00000000			
0xB0CFFC08- B0CFFFFC	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

Figure 7. External Input Timing



Slew Rate High Current Outputs

(T_A = –40 °C to 105 °C, V_{DD} = 1.1V to 1.3V, V_{DP3} = 3.0V to 3.6V, V_{DP5} = AV_{DD5} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS5} = DV_{SS} = 0V)

Table 49. Slew Rate High Current Outputs

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Output rise/fall time	t_{R30} t_{F30}	I/O circuit type SMC	Output driving strength set to “30mA”	15 at C_{LOAD} = 0 pF	–	ns	–

Figure 8. Slew Rate High Current Output Timing

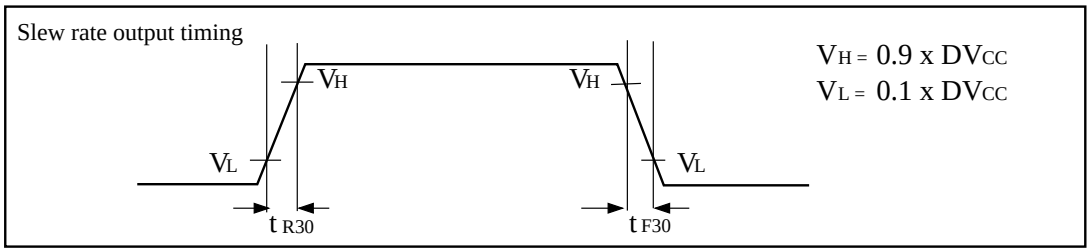


Table 66. Flash Pin Mapping to External Pins (Continued)

External Pin Number (QFP-176)	External Pin Name	Flash Macro Pin	Function
100	P1_01	FA[00]	Flash address. Refer to Table 69 on page 281 for additional details regarding use of FA[21].
101	P1_02	FA[01]	
102	P1_03	FA[02]	
103	P1_04	FA[03]	
104	P1_05	FA[04]	
105	P1_06	FA[05]	
106	P1_07	FA[06]	
109	P1_08	FA[07]	
110	P1_09	FA[08]	
111	P1_10	FA[09]	
112	P1_11	FA[10]	
113	P1_12	FA[11]	
114	P1_13	FA[12]	
115	P1_14	FA[13]	
116	P1_15	FA[14]	
119	P1_16	FA[15]	
120	P1_17	FA[16]	
121	P1_18	FA[17]	
122	P1_19	FA[18]	
123	P1_20	FA[19]	
124	P1_21	FA[20]	
125	P1_22	FA[21]	
126	P1_23	FA[22]	
150	P2_32	DIN[00]/DOR[00]	Shared data input/output. Refer Section /
151	P2_33	DIN[01]/DOR[01]	
152	P2_34	DIN[02]/DOR[02]	
153	P2_35	DIN[03]/DOR[03]	
154	P2_36	DIN[04]/DOR[04]	
155	P2_37	DIN[05]/DOR[05]	
158	P2_38	DIN[06]/DOR[06]	
159	P2_39	DIN[07]/DOR[07]	
160	P2_40	DIN[08]/DOR[08]	
161	P2_41	DIN[09]/DOR[09]	
162	P2_42	DIN[10]/DOR[10]	
163	P2_43	DIN[11]/DOR[11]	
164	P2_48	DIN[12]/DOR[12]	
165	P2_49	DIN[13]/DOR[13]	
168	P2_50	DIN[14]/DOR[14]	
169	P2_51	DIN[15]/DOR[15]	

Reference Documents

Document Type	Definition	Primary User	Document Code
MB9EF226 Datasheet	The function and its characteristics are specified quantitatively.	Investigator and hardware engineer	002-05678
FCR4 Cluster Hardware manual	The function and its operation of FCR4 cluster series are described.	Software engineer	002-09388
Iris-SDL Hardware manual	The function and its operation of GPU core platform are described.	Software engineer	002-09380
ARM Cortex™-R4 Technical Reference manual	ARM documentation set for the ARM Cortex-R4 processor core platform	Software engineer	Revision: r1p4
Application note	The reference software, sample application, the reference board design and so on are explained.	Software and hardware engineer	Under consideration

Notes
42. Refer all documents for the system development.
43. Primary user is a most likely engineer for whom the document is the most useful.
44. FCR4 Hardware manual is expected to be used as dictionary of platform specification.
45. The IRIS-SDL manual describes the implemented graphics IP.
46. The ARM Technical Reference manual describes the Cortex™-R4 architecture of core, bus, trace and debug interface.

4. IRQ Hold Clear - use following sequence to clear the bit:

```
IRQ0_UNLOCK = <unlock-key>
IRQ0_CSR = 0;              // setting IRQEN bit to '0'
IRQ0_CSR;                  // dummy read to generate wait cycles
                           // until IRQ is latched in IUNIT, resp.
                           // state machine returned to idle state
IRQ0_IRQHC = <IRQ-Nr>      // clear Hold-bit of IRQ
IRQ0_CSR = 1;              // setting IRQEN bit to '1'
IRQ0_UNLOCK = <lock-key>
```

   NMI Hold Clear - use following workaround:

   NMI handling shall be implemented according to workarounds in CI707-00026-E_FCR4_IRQ_Unit_register_read_timing_issue (will not use any potential wrong NMI register values, as reading is prohibited anyway).

5. Perform write access to IRQ0_IRQHC only with 16-bit or 32-bit access width.

Limitation Details Undefined Port Pin State while Core Supply (VDD) is Unavailable

When the port pins (Pi_jj) are powered (i.e. depending on the IO Pin type, VDP3 or VDP5 is applied) and the core supply voltage VDD is out of the recommended operating conditions, then two issues occur:

1. the port pins (Pi_jj) may drive any state, i.e. they may show any of the following states high/low, pull-up, pull-down or high-Z instead of the intended state high-Z.
2. the states of the analog switches to connect the Stepper Motor Controller (SMC) port pins to the A/D converter may be undefined. Several switches may be in the conducting state at once and create connections between the SMC port pins. Depending on the voltage levels on the SMC port pins internal currents may flow.

This is described in more detail in the next two sections.

Undefined Port Pin State

As can be seen in Figure 34, port pins Pi_jj in VDP3 and VDP5 power domain may enter undefined state while the 1.2V core supply VDD is below the recommended operating conditions.

As an example, the figure shows a system in which a VDP5 power drop is starting at T_0.

At T_1 an external supply voltage monitor asserts RSTX. This switches the port pins Pi_jj to high-Z state.

At T_2, VDP3, which was also decreasing, is out of recommended operating conditions. The port pins Pi_jj should stay in the high-Z state down to a lower VDP3 voltage. However, as they are operated outside recommended operating conditions, this is shown as X.

At T_3 VDP5 is out of recommended operating conditions. The port pins Pi_jj should stay in the high-Z state down to a lower VDP5 voltage. However, as they are operated outside recommended operating conditions, this is shown as X.