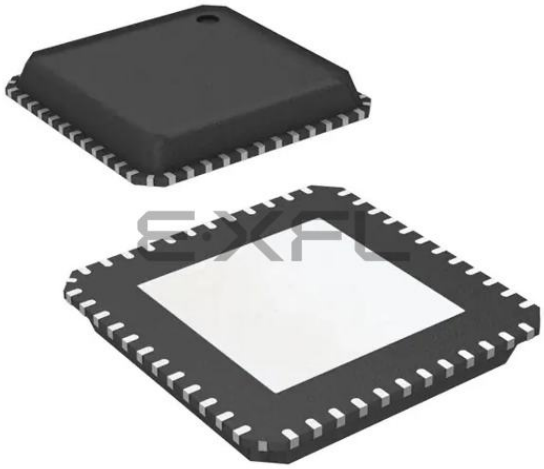

Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (64kB)
Controller Series	-
RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9877qxa20xuma1

2 Block Diagram

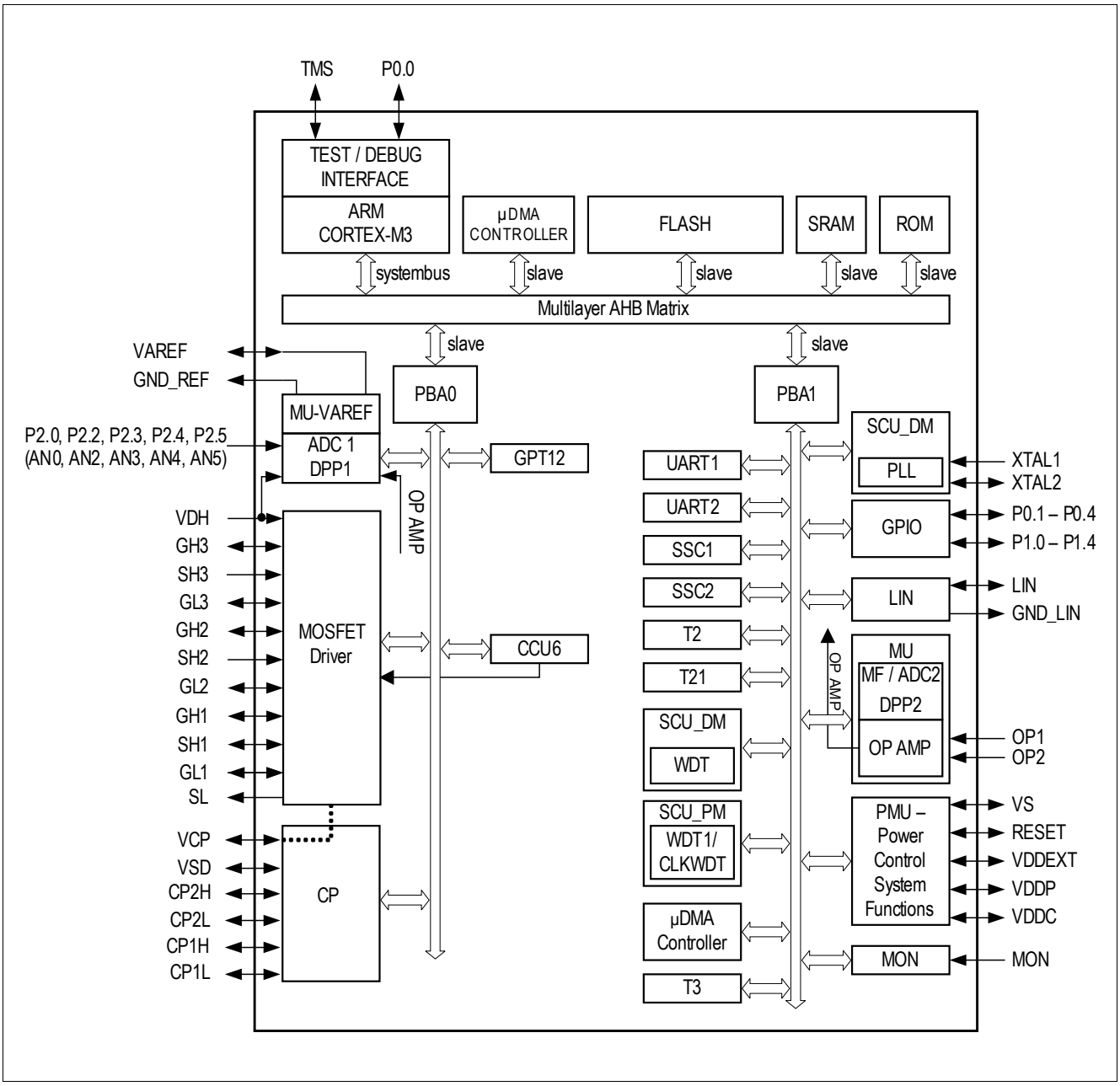

Figure 1 Block Diagram TLE9877QXA20

1) May not be switched off due to safety reasons
2) MC PLL clock disabled, MC supply reduced to 1.1 V

Wake-Up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for the monitor input, by LIN or by cyclic wake-up.

5.3.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which provides the supply for the microcontroller core, the digital peripherals and other internal analog 1.5 V functions (e.g. ADC2) of the chip. To further reduce the current consumption of the MCU during Stop Mode the output voltage can be lowered to 1.1 V.

Features

- 1.5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with reset
- Pull Down Current Source at the output for Sleep Mode only (typ. 100 µA)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

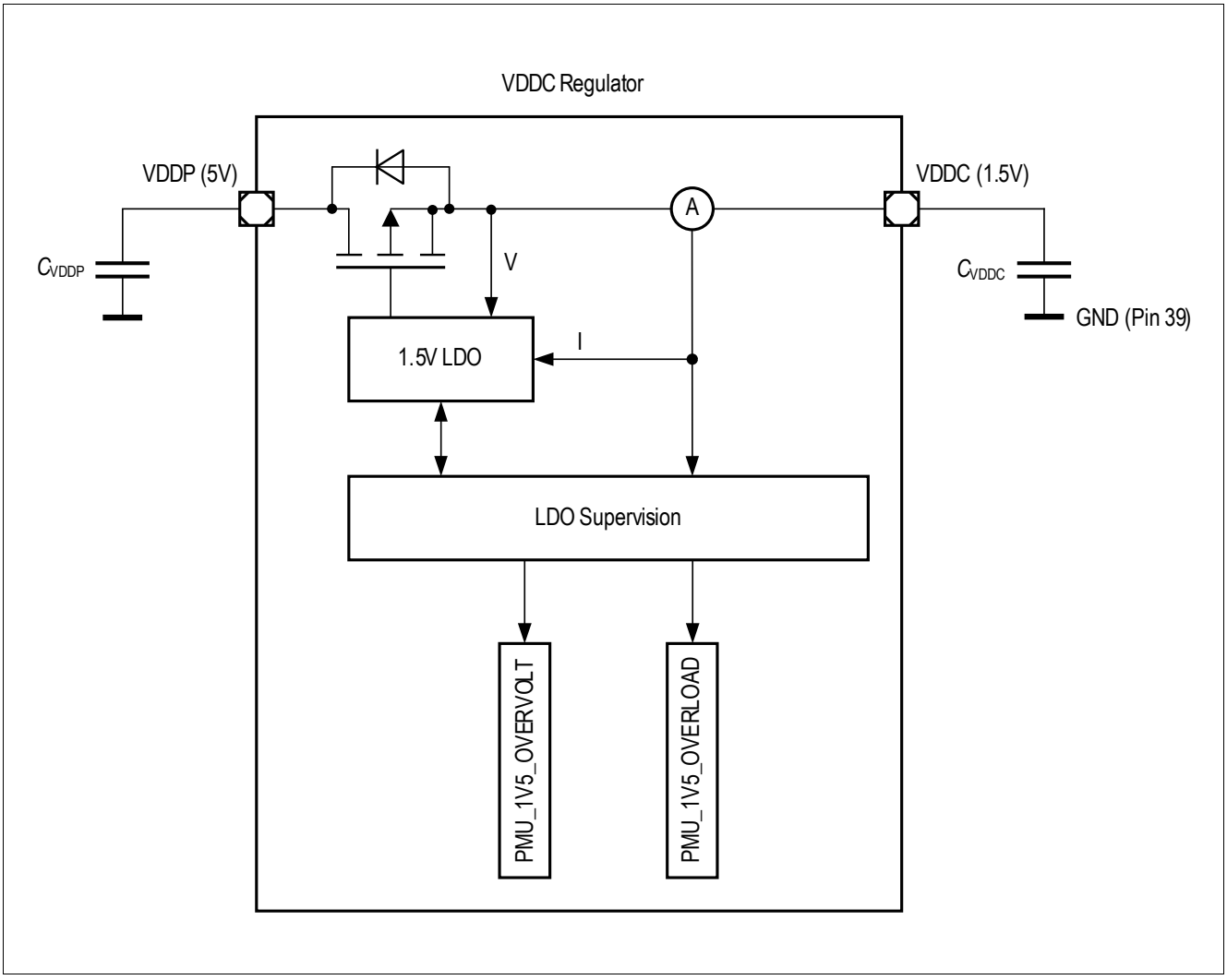

Figure 6 Module Block Diagram of VDDC Voltage Regulator

5.3.3 External Voltage Regulator 5.0V (VDDEXT)

This module represents the 5 V voltage regulator, which serves as a supply for external circuits. It can be used e.g. to supply an external sensor, LEDs or potentiometers.

Features

- Switchable +5 V, low-drop voltage regulator
- Switch-on overcurrent blanking time in order to drive small capacitive loads
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Pull Down current source at the output for Sleep Mode only (typ. 100 µA)
- Cyclic sense option together with GPIOs

The output capacitor C_{VDDEXT} is mandatory to ensure a proper regulator functionality.

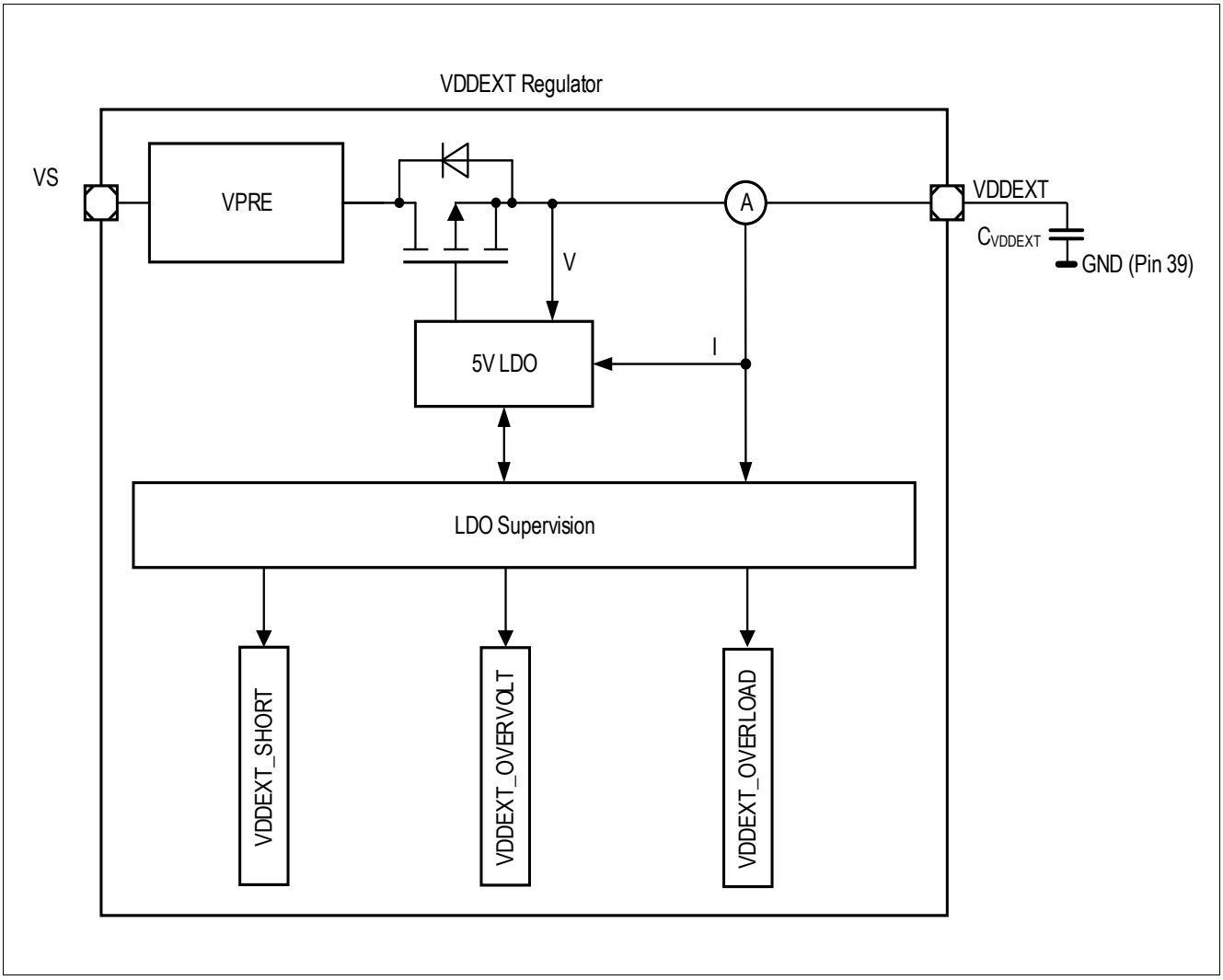

Figure 7 Module Block Diagram of External Voltage Regulator

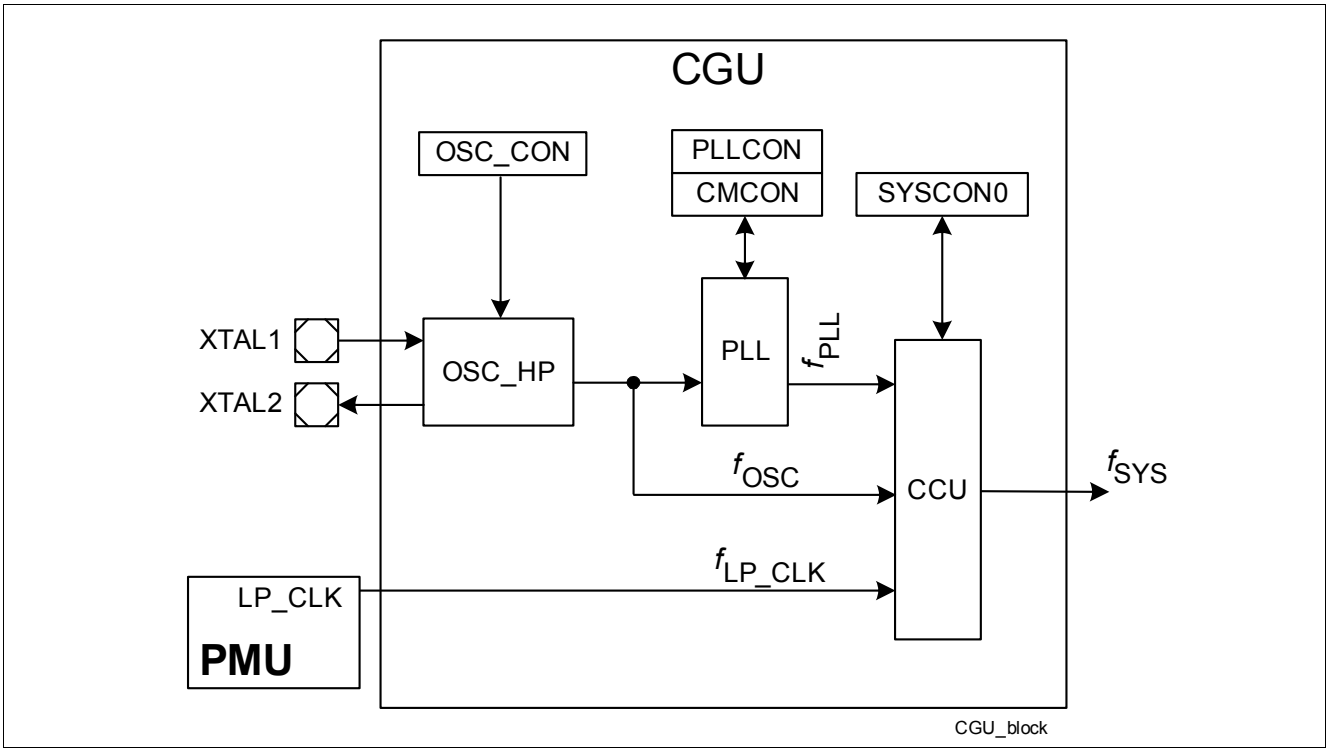

Figure 9 Clock Generation Unit Block Diagram

The following sections describe the different parts of the CGU.

6.3.1 Low Precision Clock

The clock source LP_CLK is a low-precision RC oscillator (LP-OSC) with a nominal frequency of 18 MHz that is enabled by hardware as an independent clock source for the TLE9877QXA20 startup after reset and during the power-down wake-up sequence. f_{LP_CLK} is not user configurable.

6.3.2 High Precision Oscillator Circuit (OSC_HP)

The high precision oscillator circuit, designed to work with both an external crystal oscillator or an external stable clock source, consists of an inverting amplifier with XTAL1 as the input, and XTAL2 as the output.

Figure 10 shows the recommended external circuitry for both operating modes, External Crystal Mode and External Input Clock Mode.

6.3.2.1 External Input Clock Mode

When supplying the clock signal directly, not using an external crystal and bypassing the oscillator, the input frequency needs to be equal or greater than 4 MHz if the PLL VCO part is used.

When using an external clock signal it must be connected to XTAL1. XTAL2 is left open (unconnected).

6.3.2.2 External Crystal Mode

When using an external crystal, its frequency can be within the range of 4 MHz to 25 MHz. An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. It normally consists of the two load capacitances C1 and C2. A series damping resistor could be required for some crystals. The exact values and the corresponding operating ranges depend on the crystal and have to be determined and optimized in cooperation with the crystal vendor using the negative resistance method. The following load cap values can be used as starting point for the evaluation:

7 System Control Unit - Power Modules (SCU-PM)

7.1 Features

- Clock Watchdog Unit (CWU): supervision of all clocks with NMI signaling relevant to power modules
- Interrupt Control Unit (ICU): all interrupt flags and status flags with system relevance
- Power Control Unit (PCU): takes over control when device enters and exits Sleep and Stop Mode
- External Watchdog (WDT1): independent system watchdog for monitoring system activity

7.2 Introduction

7.2.1 Block Diagram

The System Control Unit of the power modules consists of the sub-modules in the figure shown below:

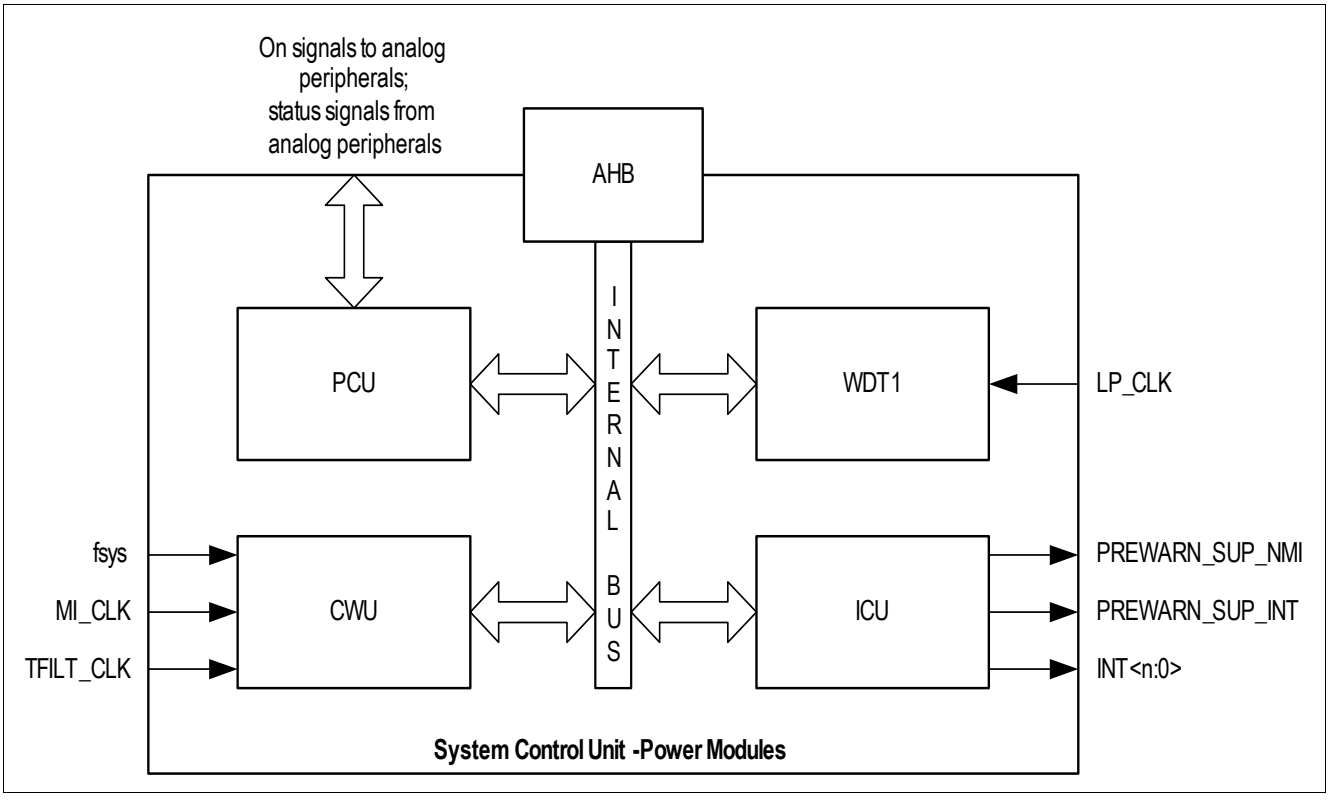

Figure 11 Block diagram of System Control Unit - Power Modules

AHB (Advanced High-Performance Bus)

CWU (Clock Watchdog Unit)

- f_{sys} system frequency: PLL output
- MI_CLK measurement interface clock (analog clock): derived from fsys using division factors 1/2/3/4
- TFILT_CLK clock used for digital filters: derived from fsys using configurable division factors

Table 7 NMI Interrupt Table

Service Request	Node	Description
Oscillator Watchdog NMI	NMI	Oscillator Watchdog / MI_CLK Watchdog Timer Overflow
NVM Map Error NMI	NMI	NVM Map Error
ECC Error NMI	NMI	RAM / NVM Uncorrectable ECC Error
Supply Prewarning NMI	NMI	Supply Prewarning

14.3.3 Port 2

14.3.3.1 Port 2 Functions

Table 10 Port 2 Input Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.0	Input	GPI	P2_DATA.P0	
		INP1	CCPOS0_3	CCU6
		INP2	-	-
		INP3	T12HR_2	CCU6
		INP4	EXINT0_0	SCU
		INP5	CC61_2	CCU6
		ANALOG	AN0	ADC
			XTAL (in)	XTAL
P2.2	Input	GPI	P2_DATA.P2	
		INP1	CCPOS2_3	CCU6
		INP2	T13HR_2	CCU6
		INP3	–	
		INP4	CC62_2	CCU6
		ANALOG	AN2	ADC
		OUT	XTAL (out)	XTAL
P2.3	Input	GPI	P2_DATA.P3	
		INP1	CCPOS1_0	CCU6
		INP2	CTRAP#_1	CCU6
		INP3	T21EX_2	Timer 21
		INP4	CC60_1	CCU6
		INP5	EXINT0_3	SCU
		ANALOG	AN3	ADC
P2.4	Input	GPI	P2_DATA.P4	
		INP1	$\overline{\text{CTRAP\#}}$_0	CCU6
		INP2	T2EUDB	GPT12T2
		INP3	MRST_1_1	SSC1
		INP4	EXINT1_3	SCU
		ANALOG	AN4	ADC
P2.5	Input	GPI	P2_DATA.P5	
		INP1	RXD2_1	UART2
		INP2	T3EUDB	GPT12T3
		INP3	MRST_2_1	SSC2
		INP4	T2_1	Timer 2
		ANALOG	AN5	ADC

19.3 UART Modes

The UART can be used in four different modes. In mode 0, it operates as an 8-bit shift register. In mode 1, it operates as an 8-bit serial port. In modes 2 and 3, it operates as a 9-bit serial port. The only difference between mode 2 and mode 3 is the baud rate, which is fixed in mode 2 but variable in mode 3. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator.

The different modes are selected by setting bits SM0 and SM1 to their corresponding values, as shown in Table 13.

Table 13 UART Modes

SM0	SM1	Operating Mode	Baud Rate
0	0	Mode 0: 8-bit shift register	$f_{PCLK}/2$
0	1	Mode 1: 8-bit shift UART	Variable
1	0	Mode 2: 9-bit shift UART	$f_{PCLK}/64$
1	1	Mode 3: 9-bit shift UART	Variable

The UART1 is connected to the integrated LIN transceiver, and to GPIO for test purpose. The UART2 is connected to GPIO only.

21 High-Speed Synchronous Serial Interface (SSC1/SSC2)

21.1 Features

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: Least Significant Bit (LSB) or Most Significant Bit (MSB) shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a transmitter empty condition
  - On a “receiver full” condition
  - On an error condition (receive, phase, baud rate, transmission error)

22.2.1.1 Block Diagram BEMF Comparator

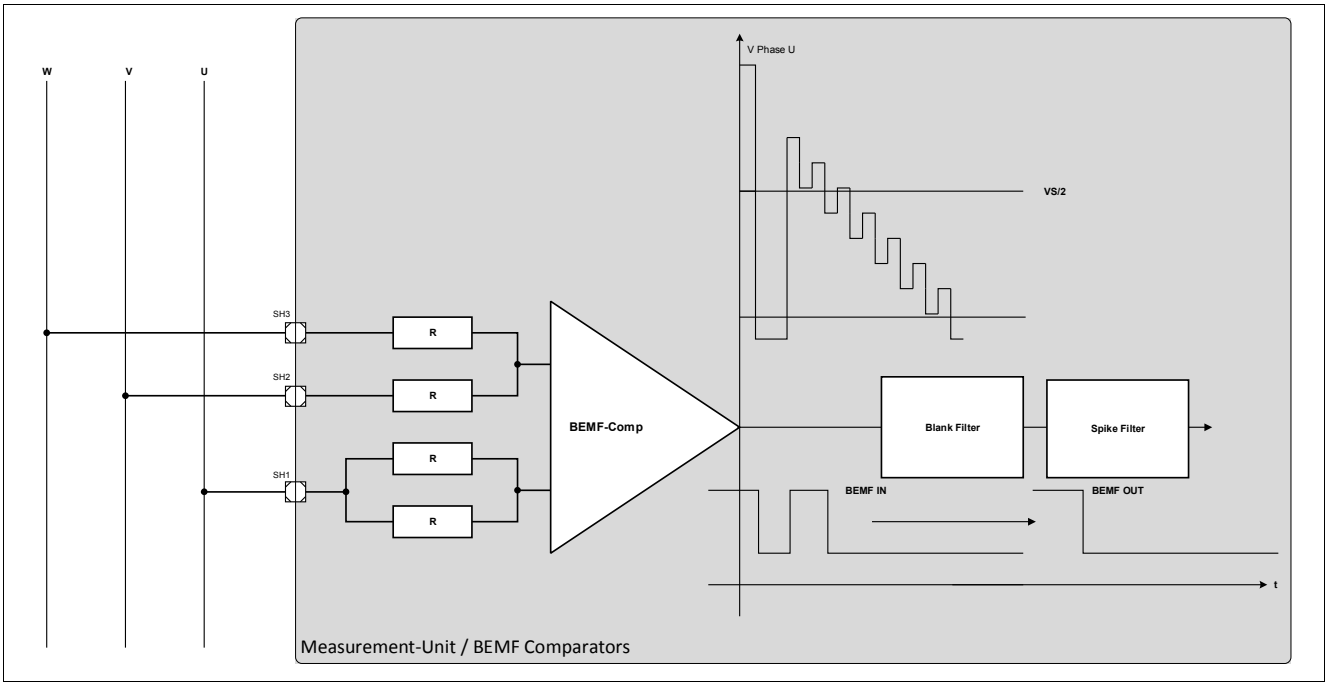

Figure 26 3 Times BEMF Comparator

23.2.2 Measurement Core Module Modes Overview

The basic function of this unit, is the digital signal processing of several analog digitized measurement signals by means of filtering, level comparison and interrupt generation. The Measurement Core module processes ten channels in a quasi parallel process.

As shown in the figure above, the ADC2 postprocessing unit consists of a channel controller (Sequencer), an 10-channel demultiplexer and the signal processing block, which filters and compares the sampled ADC2 values for each channel individually. The channel control block controls the multiplexer sequencing on the analog side before the ADC2 and on the digital domain after the ADC2. As described in the following section, the channel sequence can be controlled in a flexible way, which allows a certain degree of channel prioritization.

This capability can be used e.g. to set a higher priority to supply voltage channels compared to the other channel measurements. The Measurement Core Module offers additionally two different post-processing measurement modes for over-/undervoltage detection and for two-level threshold detection.

The channel controller (sequencer) runs in one of the following modes:

“Normal Sequencer Mode” – channels are selected according to the 10 sequence registers which contain individual enablers for each of the 10 channels.

“Exceptional Interrupt Measurement” – following a hardware event, a high priority channel is inserted into the current sequence. The current actual measurement is not destroyed.

“Exceptional Sequence Measurement” – following a hardware event, a complete sequence is inserted after the current measurement is finished. The current sequence is interrupted by the exception sequence.

24 10-Bit Analog Digital Converter (ADC1)

24.1 Features

The principal features of the ADC1 are:

- Up to 8 analog input channels (channel 7 reserved for future use)
- Flexible results handling
  - 8-bit and 10-bit resolution
- Flexible source selection due to sequencer
  - insert one exceptional sequence (ESM)
  - insert one interrupt measurement into the current sequence (EIM), single or up to 128 times
  - software mode
- Conversion sample time (separate for each channel) adjustable to adapt to sensors and reference
- Standard external reference (VAREF) to support ratiometric measurements and different signal scales
- DMA support, transfer ADC conversion results via DMA into RAM
- Support of suspend and power saving modes
- Result data protection for slow CPU access (wait-for-read mode)
- Programmable clock divider
- Integrated sample and hold circuitry

24.2 Introduction

The TLE9877QXA20 includes a high-performance 10-bit Analog-to-Digital Converter (ADC1) with eight multiplexed analog input channels. The ADC1 uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC1 are available at AN0, AN2 - AN5.

29.2.2 PMU Core Supply (VDDC) Parameters

This chapter describes all electrical parameters which are observable on SoC level. For this purpose only the core-supply VDDC and the transition times between the system modes are specified here.

Table 23 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Required decoupling capacitance	C_{VDDC1}	0.1	–	1	µF	1)2) ESR < 1Ω; the specified capacitor value is a typical value.	P_2.2.1
Required buffer capacitance for stability (load jumps)	C_{VDDC2}	0.33	–	1	µF	2)the specified capacitor value is a typical value.	P_2.2.17
Output voltage including line regulation @ Active Mode	V_{DDCOUT}	1.44	1.5	1.56	V	I_{load} < 40mA	P_2.2.2
Reduced output voltage including line regulation @ Stop Mode	$V_{DDCOUT\_Stop\_Red}$	0.95	1.1	1.3	V	with internal VDDC load only: $I_{load\_internal}$ < 1.5mA	P_2.2.23
Load Regulation @ Active Mode	V_{DDCLOR}	-50	–	50	mV	2 ... 40mA; C =430nF	P_2.2.3
Line regulation @ Active Mode	V_{DDCLIR}	-25	–	25	mV	V_{DDP} = 2.5 ... 5.5V	P_2.2.4
Overvoltage detection	V_{DDCOV}	1.59	1.62	1.68	V	Overvoltage leads to SUPPLY_NMI	P_2.2.5
Overvoltage detection filter time	t_{FILT_VDDCOV}	–	735	–	µs	1)3)	P_2.2.18
Voltage OK detection range[4)]	ΔV_{DDCOK}	- 280	–	+ 280	mV	1)	P_2.2.19
Voltage stable detection range[5)]	ΔV_{DDCSTB}	- 110	–	+ 110	mV	1)	P_2.2.20
Undervoltage reset	V_{DDVUV}	1.136	1.20	1.264	V	–	P_2.2.6
Overcurrent diagnostic	I_{VDDCOC}	45	–	100	mA	–	P_2.2.7
Overcurrent diagnostic filter time	t_{FILT_VDDCOC}	–	27	–	µs	1)3)	P_2.2.21
Overcurrent diagnostic shutdown time	$t_{FILT\_VDDCOC\_SD}$	–	290	–	µs	1)3)6)	P_2.2.22

1) Not subject to production test, specified by design.
2) Ceramic capacitor.
3) This filter time and its variation is derived from the time base $t_{LP\_CLK} = 1 / f_{LP\_CLK}$.
4) The absolute voltage value is the sum of parameters $V_{DDC} + \Delta V_{DDCSTB}$.
5) The absolute voltage value is the sum of parameters $V_{DDC} + \Delta V_{DDCOK}$.
6) After $t_{FILT\_VDDCOC\_SD}$ is passed and the overcurrent condition is still present the device will enter sleep mode.

29.5 Parallel Ports (GPIO)

29.5.1 Description of Keep and Force Current

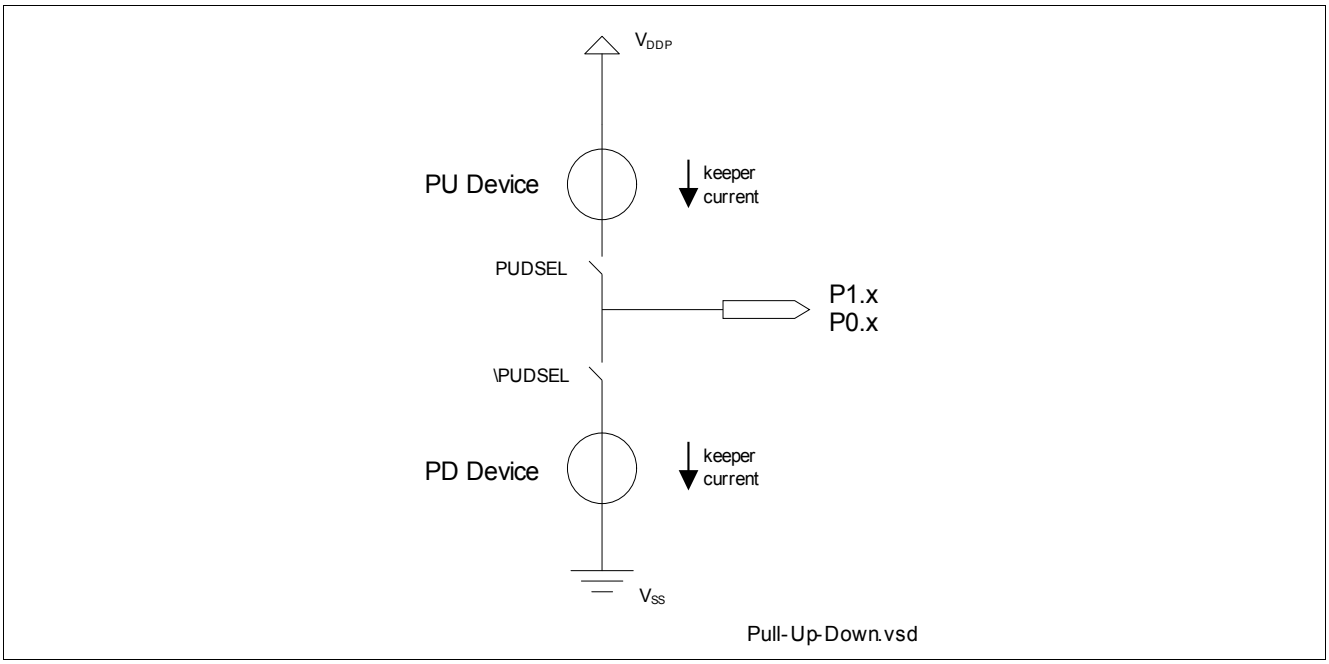

Figure 34 Pull-Up/Down Device

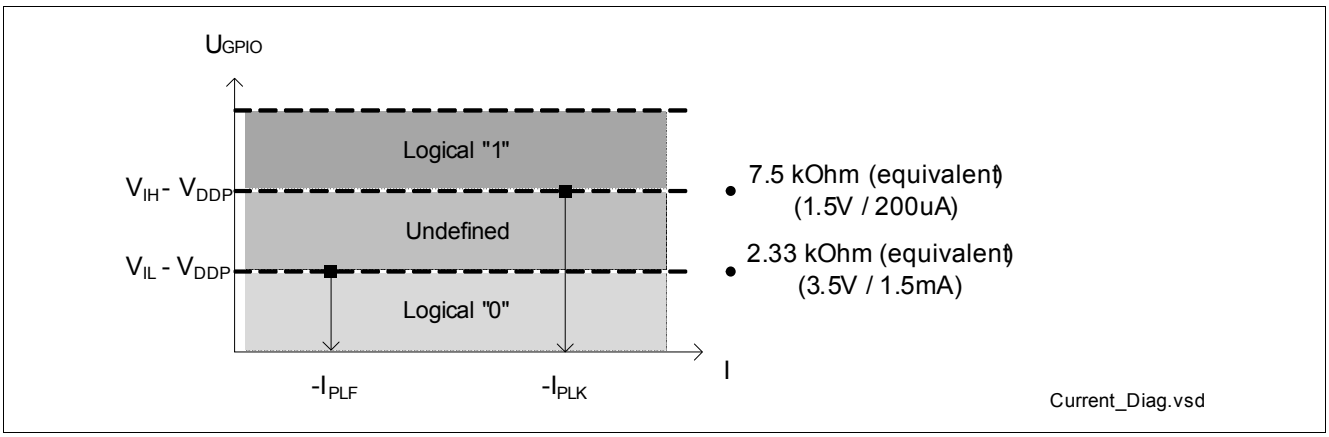

Figure 35 Pull-Up Keep and Forced Current

Table 32 DC Characteristics Port 2 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Pull level force current	I_{PLF}	-750	–	+750	µA	3) $V_{PIN} \le V_{IL}$ (up) $V_{PIN} \ge V_{IH}$ (dn)	P_5.2.6
Pin capacitance (digital inputs/outputs)	C_{IO}	–	–	10	pF	2)	P_5.2.7

1) Tested at V_{DDP} = 5V, specified for 4.5V < V_{DDP} < 5.5V.

2) Not subject to production test, specified by design.

3) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \ge V_{IH}$ for a pull-up; $V_{PIN} \le V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \le V_{IL}$ for a pull-up; $V_{PIN} \ge V_{IH}$ for a pull-down.

29.6 LIN Transceiver

29.6.1 Electrical Characteristics

Table 33 Electrical Characteristics LIN Transceiver

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Bus Receiver Interface							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	0.53 x V_S	V	SAE J2602	P_6.1.1
Receiver dominant state	V_{BUSdom}	-27	–	0.4 × V_S	V	LIN Spec 2.2 (Par. 17)	P_6.1.2
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	0.47 x V_S	0.55 × V_S	0.6 × V_S	V	SAE J2602	P_6.1.3
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	1.15 × V_S	V	[1] LIN Spec 2.2 (Par. 18)	P_6.1.4
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	[2] LIN Spec 2.2 (Par. 19)	P_6.1.5
Receiver hysteresis	V_{HYS}	0.07 V_S	0.12 × V_S	0.175 × V_S	V	[3] LIN Spec 2.2 (Par. 20)	P_6.1.6
Wake-up threshold voltage	$V_{BUS,wk}$	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_6.1.7
Dominant time for bus wake-up (internal analog filter delay)	$t_{WK,bus}$	3	–	15	µs	The overall dominant time for bus wake-up is a sum of $t_{WK,bus}$ + adjustable digital filter time. The digital filter time can be adjusted by PMU.CNF_WAKE_FILTER.CNF_LIN_FT;	P_6.1.8
Bus Transmitter Interface							
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high Level	P_6.1.9
Bus dominant output voltage	$V_{BUS,do}$	–	–	0.22 × V_S	V	Driver Dominant Voltage R_L = 500 Ohm	P_6.1.78

29.7 High-Speed Synchronous Serial Interface

29.7.1 SSC Timing Parameters

The table below provides the SSC timing in the TLE9877QXA20.

Table 34 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SCLK clock period	t_0	1) 2 * T_{SSC}	–	–		2) V_{DDP} > 2.7 V	P_7.1.1
MTSR delay from SCLK	t_1	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.2
MRST setup to SCLK	t_2	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.3
MRST hold from SCLK	t_3	15	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.4

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. If f_{CPU} = 20 MHz, t_0 = 100 ns. T_{CPU} is the CPU clock period.
2) Not subject to production test, specified by design.

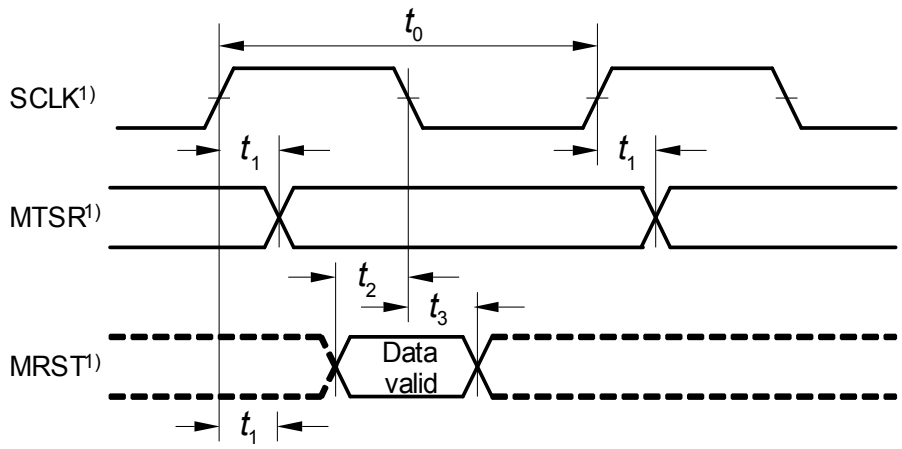

Figure 37 SSC Master Mode Timing

29.9.2 Electrical Characteristics ADC1 (10-Bit)

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 40 A/D Converter Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Analog reference supply	V_{AREF}	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	1)	P_9.2.1
Analog reference ground	V_{AGND}	V_{SS} - 0.05	–	1.5	V	–	P_9.2.2
Analog input voltage range	V_{AIN}	V_{AGND}	–	V_{AREF}	V	2)	P_9.2.3
Analog clock frequency	f_{ADCI}	5	–	24	MHz	3)	P_9.2.4
Conversion time for 10-bit result	t_{C10}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	–	1)4)	P_9.2.5
Conversion time for 8-bit result	t_{C8}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	–	1)	P_9.2.6
Wakeup time from analog powerdown, fast mode	t_{WAF}	–	–	4	µs	1)	P_9.2.7
Wakeup time from analog powerdown, slow mode	t_{WAS}	–	–	15	µs	1)5)	P_9.2.8
Total unadjusted error (8 bit)	TUE_{8B}	-2	±1	+2	counts	6)7)Reference is internal V_{AREF}	P_9.2.9
Total unadjusted error (10 bit)	TUE_{10B}	-12	±6	+12	counts	7)8)Reference is internal V_{AREF}	P_9.2.22
DNL error	EA_{DNL}	-3	±0.8	+3	counts	–	P_9.2.10
INL error	$EA_{INL\_int\_VAREF}$	-5	±0.8	+5	counts	Reference is internal V_{AREF}	P_9.2.11
Gain error	$EA_{GAIN\_int\_VAREF}$	-10	±0.4	+10	counts	Reference is internal V_{AREF}	P_9.2.12
Offset error	EA_{OFF}	-2	±0.5	+2	counts	–	P_9.2.13
Total capacitance of an analog input	C_{AINT}	–	–	10	pF	1)5)9)	P_9.2.14
Switched capacitance of an analog input	C_{AINS}	–	–	4	pF	1)5)9)	P_9.2.15
Resistance of the analog input path	R_{AIN}	–	–	2	kΩ	1)5)9)	P_9.2.16

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Resistor between SHx and GND	R_{SHGN}	30	40	50	kΩ	[1)3)] This resistance is the resistance between GHx and GND connected through a diode to SHx. As a consequence, the voltage at SHx can rise up to 0,6V typ. before it is discharged through the resistor.	P_12.1.10
Low RDSON mode (boosted discharge mode)	R_{ONCCP}	–	9	12	Ω	V_{VSD} = 13.5 V, V_{VCP} = V_{VSD} + 14.0 V; I_{CHARGE} = I_{DISCHG} = 31(max); 50mA forced into Gx, Sx grounded	P_12.1.50
Resistance between VDH and VSD	I_{BSH}	–	4	–	kΩ	[1)]	P_12.1.24
Input propagation time (LS on)	$t_{P(ILN)min}$	–	1.5	3	µs	[1)] C_{Load} = 10 nF, I_{Charge} =3(min), 25% of V_{Gxx1}	P_12.1.37
Input propagation time (LS off)	$t_{P(ILF)min}$	–	1.5	3	µs	[1)] C_{Load} = 10 nF, $I_{Discharge}$ =3(min), 75% of V_{Gxx1}	P_12.1.38
Input propagation time (HS on)	$t_{P(IHN)min}$	–	1.5	3	µs	[1)] C_{Load} = 10 nF, I_{Charge} =3(min) 25% of V_{Gxx1}	P_12.1.39
Input propagation time (HS off)	$t_{P(IHF)min}$	–	1.5	3	µs	[1)] C_{Load} = 10 nF, $I_{Disharge}$ =3(min), 75% of V_{Gxx1}	P_12.1.40
Input propagation time (LS on)	$t_{P(ILN)max}$	–	200	350	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.26
Input propagation time (LS off)	$t_{P(ILF)max}$	–	200	300	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.27
Input propagation time (HS on)	$t_{P(IHN)max}$	–	200	350	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.28
Input propagation time (HS off)	$t_{P(IHF)max}$	–	200	300	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.29