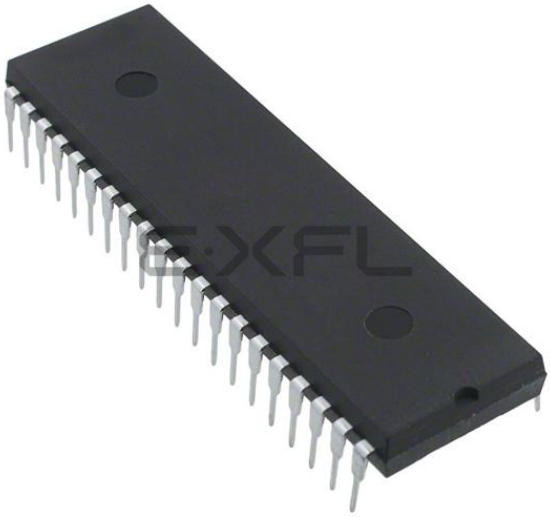


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	60MHz
Connectivity	SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51ed2-3csim

Enhanced Features

In comparison to the original 80C52, the AT89C51RD2/ED2 implements some new features, which are

- **X2 option**
- **Dual Data Pointer**
- **Extended RAM**
- **Programmable Counter Array (PCA)**
- **Hardware Watchdog**
- **SPI interface**
- **4-level interrupt priority system**
- **Power-off flag**
- **ONCE mode**
- **ALE disabling**
- **Some enhanced features are also located in the UART and the Timer 2**

X2 Feature

The AT89C51RD2/ED2 core needs only 6 clock periods per machine cycle. This feature called 'X2' provides the following advantages:

- **Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.**
- **Save power consumption while keeping same CPU power (oscillator power saving).**
- **Save power consumption by dividing dynamically the operating frequency by 2 in operating and idle modes.**
- **Increase CPU power by 2 while keeping same crystal frequency.**

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

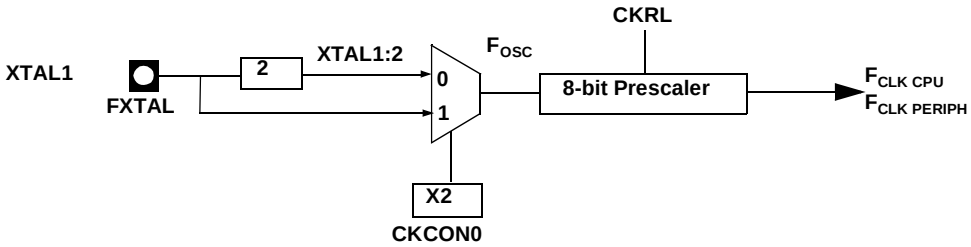
Description

The clock for the whole circuit and peripherals is first divided by two before being used by the CPU core and the peripherals.

This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%.

Figure 5 shows the clock generation block diagram. X2 bit is validated on the rising edge of the XTAL1÷2 to avoid glitches when switching from X2 to STD mode. Figure 6 shows the switching mode waveforms.

Figure 5. **Clock Generation Diagram**



Serial I/O Port

The serial I/O port in the AT89C51RD2/ED2 is compatible with the serial I/O port in the 80C52.
It provides both synchronous and asynchronous communication modes. It operates as a Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

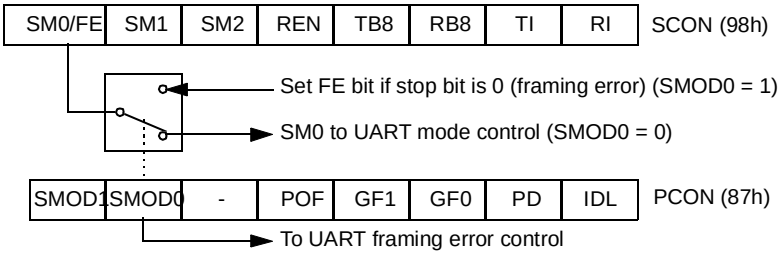
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 22).

Figure 22. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 33.) bit is set.
Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 23. and Figure 24.).

Figure 23. UART Timings in Mode 1

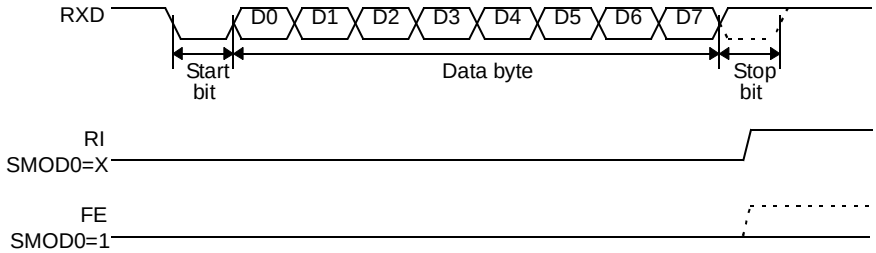
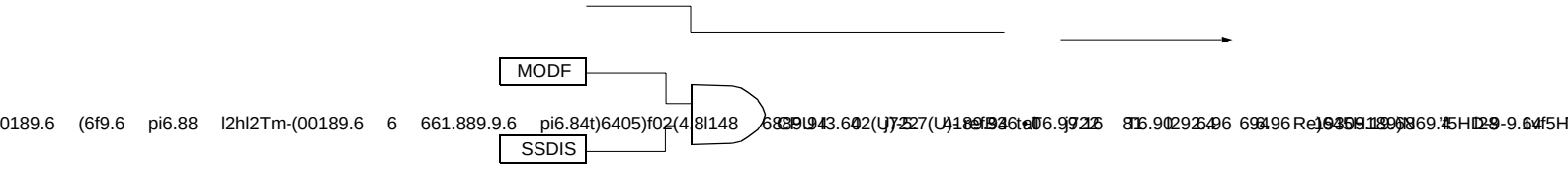


Figure 35. SPI Interrupt Requests Generation



Registers

There are three registers in the Module that provide control, status and data storage functions. These registers are describes in the following paragraphs.

Serial Peripheral Control Register (SPCON)

- The Serial Peripheral Control Register does the following:
- Selects one of the Master clock rates
- Configure the SPI Module as Master or Slave
- Selects serial clock polarity and phase
- Enables the SPI Module
- Frees the SS pin for a general-purpose

Table 48 describes this register and explains the use of each bit

Table 48. SPCON Register

SPCON - Serial Peripheral Control Register (0C3H)

Bit Number	Bit Mnemonic	Description
1	**-**	Reserved **The value read from this bit is indeterminate. Do not set this bit.**
0	**-**	Reserved **The value read from this bit is indeterminate. Do not set this bit.**

Reset Value = 00X0 XXXXb

Not Bit addressable

Serial Peripheral DATa Register (SPDAT)

The Serial Peripheral Data Register (Table 50) is a read/write buffer for the receive data register. A write to SPDAT places data directly into the shift register. No transmit buffer is available in this model.

A Read of the SPDAT returns the value located in the receive buffer and not the content of the shift register.

Table 50. **SPDAT Register**

SPDAT - Serial Peripheral Data Register (0C5H)

7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	R1	R0

Reset Value = Indeterminate

R7:R0: Receive data bits

SPCON, SPSTA and SPDAT registers may be read and written at any time while there is no on-going exchange. However, special care should be taken when writing to them while a transmission is on-going:

- **Do not change SPR2, SPR1 and SPR0**
- **Do not change CPHA and CPOL**
- **Do not change MSTR**
- **Clearing SPEN would immediately disable the peripheral**
- **Writing to the SPDAT will cause an overflow.**

The PCA interrupt vector is located at address 0033H, the SPI interrupt vector is located at address 004BH and Keyboard interrupt vector is located at address 003BH. All other vectors addresses are the same as standard C52 devices.

Table 51. **Priority Level Bit Values**

IPH.x	IPL.x	Interrupt Level Priority
0	**0**	**0 (Lowest)**
0	**1**	**1**
1	**0**	**2**
1	**1**	**3 (Highest)**

A low-priority interrupt can be interrupted by a high priority interrupt, but not by anoth low-priority interrupt. A high-priority interrupt can't be interrupted by any other interru source.

If two interrupt requests of different priority levels are received simultaneously, th request of higher priority level is serviced. If interrupt requests of the same priority lev are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determine by the polling sequence.

ONCE^{fi} Mode (ON-Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using AT89C51RD2/ED2 without removing the circuit from the board. The ONCE mode is invoked by driving cer tain pins of the AT89C51RD2/ED2; the following sequence must be exercised:

- **Pull ALE low while the device is in reset (RST high) and PSEN high.**
- **Hold ALE low as RST is deactivated.**

While the AT89C51RD2/ED2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit. Table 63 shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 63. **External Pin Status During ONCE Mode**

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	Port I2	XTALA1/2	XTALB1/2
Weak pull-up	**Weak pull-up**	**Float**	**Weak pull-up**	**Weak pull-up**	**Weak pull-up**	**Float**	**Active**	**Active**

Table 57. IPL1 Register

IPL1 - Interrupt Priority Register (B2h)

7	6	5	4	3	2	1	0
-	-	-	-	-	SPIL	TWIL	KBDL

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	SPIL	**SPI interrupt Priority bit** Refer to SPIH for priority level.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	KBDL	**Keyboard interrupt Priority bit** Refer to KBDH for priority level.

Reset Value = XXXX X000b
Bit addressable