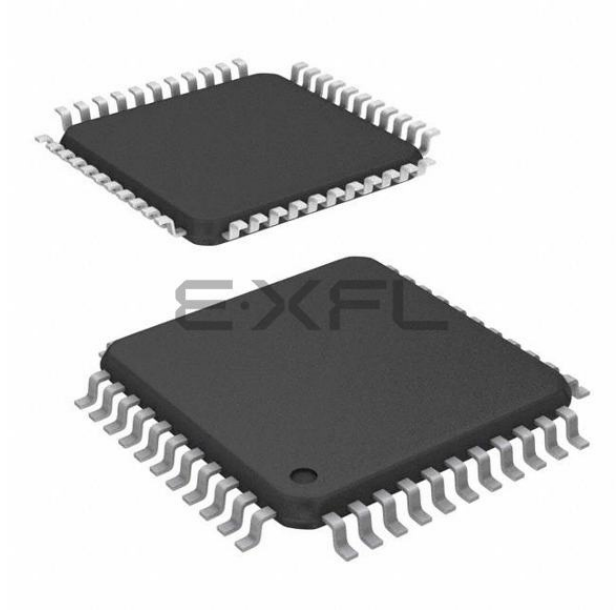

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	60MHz
Connectivity	SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-VQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51rd2-rlrim

The CMOD register includes three additional bits associated with the PCA (See Figure 16 and Table 22).

- The CIDL bit which allows the PCA to stop during idle mode.
- The WDTE bit which enables or disables the watchdog function on module 4.
- The ECF bit which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

Figure 16. PCA Timer/Counter

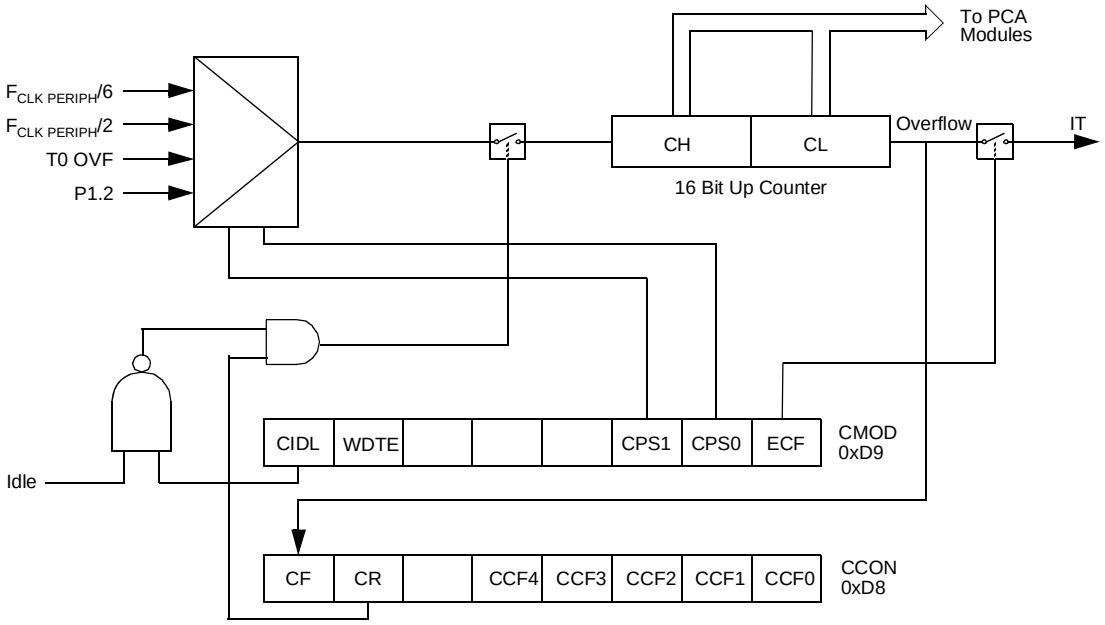


Table 22. CMOD Register

CMOD - PCA Counter Mode Register (D9h)

7	6	5	4	3	2	1	0
CIDL	**WDTE**	**-**	**-**	**-**	**CPS1**	**CPS0**	**ECF**

Bit Number	Bit Mnemonic	Description
7	CIDL	**Counter Idle Control** Cleared to program the PCA Counter to continue functioning during idle Mode. Set to program PCA to be gated off during idle.
6	WDTE	**Watchdog Timer Enable** Cleared to disable Watchdog Timer function on PCA Module 4. Set to enable Watchdog Timer function on PCA Module 4.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	CPS1	**PCA Count Pulse Select**
1	CPS0	CPS1 CPS0 Selected PCA input 0 0 Internal clock $F_{CLK\ PERIPH}/6$ 0 1 Internal clock $F_{CLK\ PERIPH}/2$ 1 0 Timer 0 Overflow 1 1 External clock at ECI/P1.2 pin (max rate = $F_{CLK\ PERIPH}/4$)
0	ECF	**PCA Enable Counter Overflow Interrupt** Cleared to disable CF bit in CCON to inhibit an interrupt. Set to enable CF bit in CCON to generate an interrupt.

Reset Value = 00XX X000b
Not bit addressable

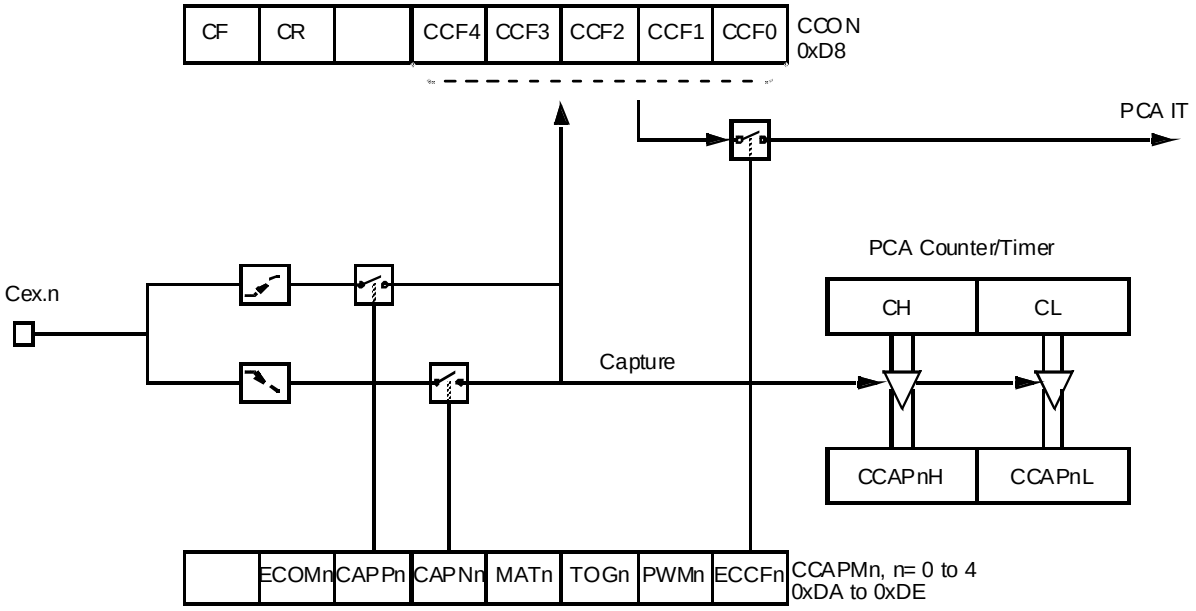
The CCON register contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 23).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 18).

Figure 18. PCA Capture Mode



16-bit Software Timer/ Compare Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (See Figure 19).

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.

Table 38. SBUF Register

SBUF - Serial Buffer Register for UART (99h)

7	6	5	4	3	2	1	0

Reset Value = XXXX XXXXb

Table 39. BRL Register

BRL - Baud Rate Reload Register for the internal baud rate generator, UART (9Ah)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Registers

Table 43. KBF Register

KBF-Keyboard Flag Register (9Eh)

7	6	5	4	3	2	1	0
KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0

Bit Number	Bit Mnemonic	Description
7	KBF7	**Keyboard line 7 flag** Set by hardware when the Port line 7 detects a programmed level. It generates a Keyboard interrupt request if the KBKBIE.7 bit in KBIE register is set. Must be cleared by software.
6	KBF6	**Keyboard line 6 flag** Set by hardware when the Port line 6 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.6 bit in KBIE register is set. Must be cleared by software.
5	KBF5	**Keyboard line 5 flag** Set by hardware when the Port line 5 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.5 bit in KBIE register is set. Must be cleared by software.
4	KBF4	**Keyboard line 4 flag** Set by hardware when the Port line 4 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.4 bit in KBIE register is set. Must be cleared by software.
3	KBF3	**Keyboard line 3 flag** Set by hardware when the Port line 3 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.3 bit in KBIE register is set. Must be cleared by software.
2	KBF2	**Keyboard line 2 flag** Set by hardware when the Port line 2 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.2 bit in KBIE register is set. Must be cleared by software.
1	KBF1	**Keyboard line 1 flag** Set by hardware when the Port line 1 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.1 bit in KBIE register is set. Must be cleared by software.
0	KBF0	**Keyboard line 0 flag** Set by hardware when the Port line 0 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.0 bit in KBIE register is set. Must be cleared by software.

Reset Value = 0000 0000b

This register is read only access, all flags are automatically cleared by reading the register.

Table 45. KBLS Register

KBLS-Keyboard Level Selector Register (9Ch)

7	6	5	4	3	2	1	0
KBLS7	KBLS6	KBLS5	KBLS4	KBLS3	KBLS2	KBLS1	KBLS0

Bit Number	Bit Mnemonic	Description
7	KBLS7	**Keyboard line 7 Level Selection bit** Cleared to enable a low level detection on Port line 7. Set to enable a high level detection on Port line 7.
6	KBLS6	**Keyboard line 6 Level Selection bit** Cleared to enable a low level detection on Port line 6. Set to enable a high level detection on Port line 6.
5	KBLS5	**Keyboard line 5 Level Selection bit** Cleared to enable a low level detection on Port line 5. Set to enable a high level detection on Port line 5.
4	KBLS4	**Keyboard line 4 Level Selection bit** Cleared to enable a low level detection on Port line 4. Set to enable a high level detection on Port line 4.
3	KBLS3	**Keyboard line 3 Level Selection bit** Cleared to enable a low level detection on Port line 3. Set to enable a high level detection on Port line 3.
2	KBLS2	**Keyboard line 2 Level Selection bit** Cleared to enable a low level detection on Port line 2. Set to enable a high level detection on Port line 2.
1	KBLS1	**Keyboard line 1 Level Selection bit** Cleared to enable a low level detection on Port line 1. Set to enable a high level detection on Port line 1.
0	KBLS0	**Keyboard line 0 Level Selection bit** Cleared to enable a low level detection on Port line 0. Set to enable a high level detection on Port line 0.

Reset Value = 0000 0000b

Serial Port Interface (SPI)

The Serial Peripheral Interface Module (SPI) allows full-duplex, synchronous, serial communication between the MCU and peripheral devices, including other MCUs.

Features

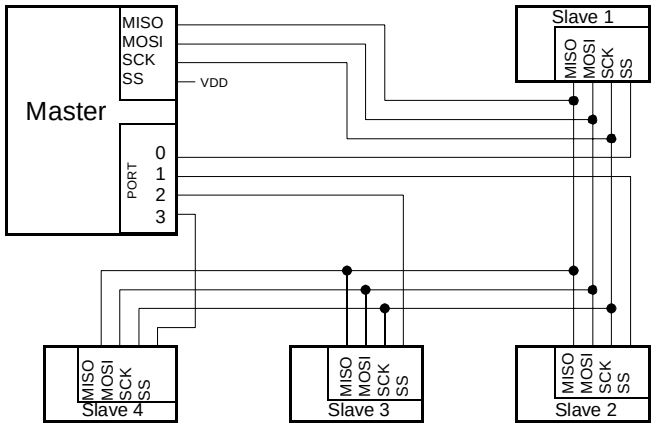
Features of the SPI Module include the following:

- Full-duplex, three-wire synchronous transfers
- Master or Slave operation
- Eight programmable Master clock rates
- Serial clock with programmable polarity and phase
- Master Mode fault error flag with MCU interrupt capability
- Write collision flag protection

Signal Description

Figure 29 shows a typical SPI bus configuration using one Master controller and many Slave peripherals. The bus is made of three wires connecting all the devices.

Figure 29. SPI Master/Slaves Interconnection



The Master device selects the individual Slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins of the Slave devices.

Master Output Slave Input (MOSI)

This 1-bit signal is directly connected between the Master Device and a Slave Device. The MOSI line is used to transfer data in series from the Master to the Slave. Therefore, it is an output signal from the Master, and an input signal to a Slave. A Byte (8-bit word) is transmitted most significant bit (MSB) first, least significant bit (LSB) last.

Master Input Slave Output (MISO)

This 1-bit signal is directly connected between the Slave Device and a Master Device. The MISO line is used to transfer data in series from the Slave to the Master. Therefore, it is an output signal from the Slave, and an input signal to the Master. A Byte (8-bit word) is transmitted most significant bit (MSB) first, least significant bit (LSB) last.

SPI Serial Clock (SCK)

This signal is used to synchronize the data movement both in and out of the devices through their MOSI and MISO lines. It is driven by the Master for eight clock cycles which allows to exchange one Byte on the serial lines.

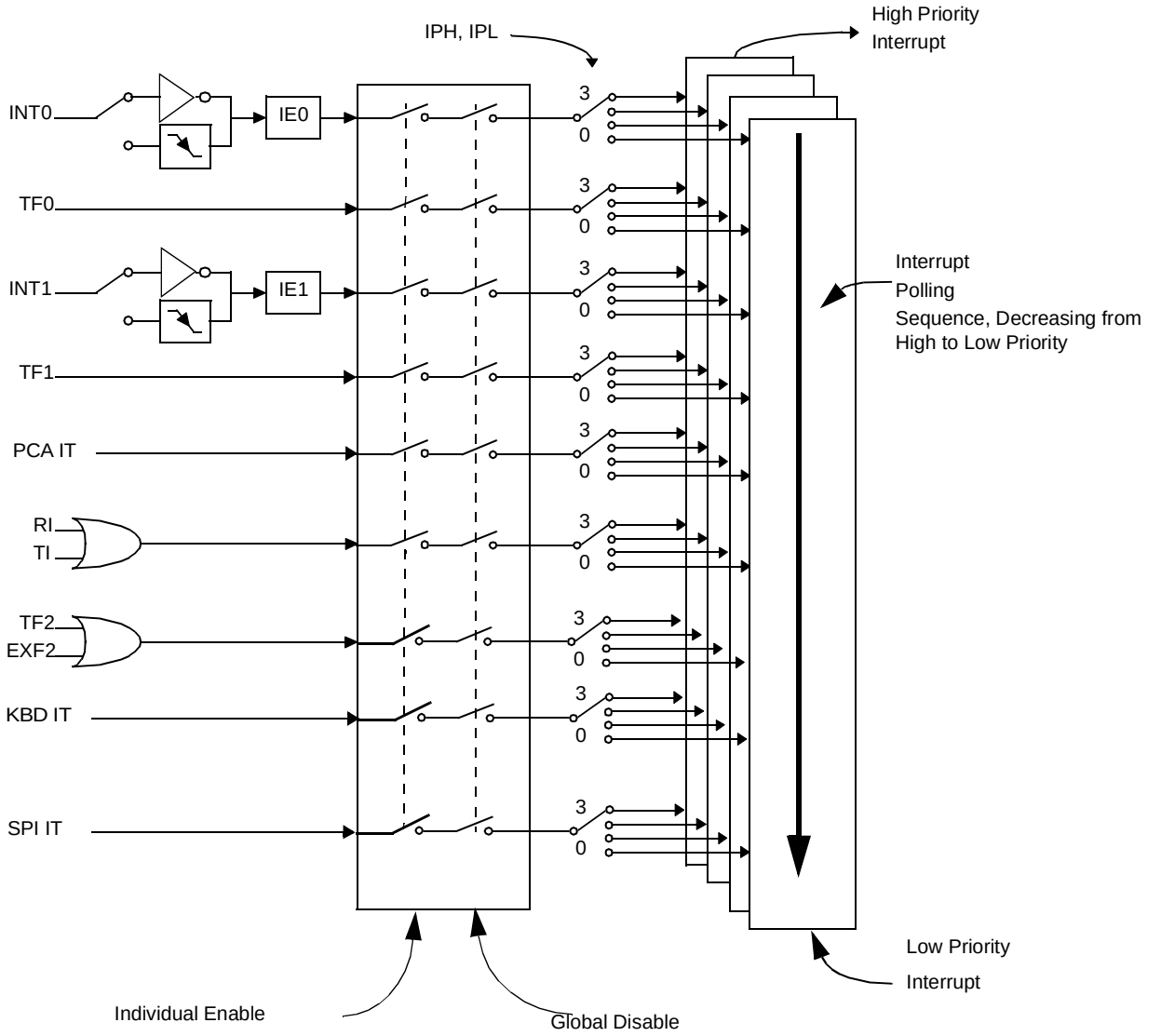
Slave Select ($\overline{SS}$)

Each Slave peripheral is selected by one Slave Select pin ($\overline{SS}$). This signal must stay low for any message for a Slave. It is obvious that only one Master ($\overline{SS}$ high level) can

Interrupt System

The AT89C51RD2/ED2 has a total of 9 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (timers 0, 1 and 2), the serial port interrupt, SPI interrupt, Keyboard interrupt and the PCA global interrupt. These interrupts are shown in Figure 36.

Figure 36. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (Table 54 and Table 56). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (Table 57) and in the Interrupt Priority High register (Table 55 and Table 56) shows the bit values and priority levels associated with each combination.

Table 62. WDTPRG Register

WDTPRG - Watchdog Timer Out Register (0A7h)

7	6	5	4	3	2	1	0
-	-	-	-	-	S2	S1	S0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is undetermined. Do not try to set this bit.
6	-	
5	-	
4	-	
3	-	
2	S2	**WDT Time-out select bit 2**
1	S1	**WDT Time-out select bit 1**
0	S0	**WDT Time-out select bit 0**
		S2 S1 S0 Selected Time-out 0 0 0 (2^{14} - 1) machine cycles, 16. 3 ms @ F_{OSCA} =12 MHz 0 0 1 (2^{15} - 1) machine cycles, 32.7 ms @ F_{OSCA}=12 MHz 0 1 0 (2^{16} - 1) machine cycles, 65. 5 ms @ F_{OSCA}=12 MHz 0 1 1 (2^{17} - 1) machine cycles, 131 ms @ F_{OSCA}=12 MHz 1 0 0 (2^{18} - 1) machine cycles, 262 ms @ F_{OSCA}=12 MHz 1 0 1 (2^{19} - 1) machine cycles, 542 ms @ F_{OSCA}=12 MHz 1 1 0 (2^{20} - 1) machine cycles, 1.05 ms @ F_{OSCA}=12 MHz 1 1 1 (2^{21} - 1) machine cycles, 2.09 ms @ F_{OSCA}=12 MHz

Reset Value = XXXX X000

WDT during Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode the user does not need to service the WDT. There are 2 methods of exiting Power-down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the AT89C51RD2/ED2 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is better to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the AT89C51RD2/ED2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

EEPROM Data Memory

This feature is available only for the AT89C51ED2 device.

The 2K bytes on-chip EEPROM memory block is located at addresses 0000h to 07FFh of the XRAM/ERAM memory space and is selected by setting control bits in the EECON register.

A read or write access to the EEPROM memory is done with a MOVX instruction.

Write Data

Data is written by byte to the EEPROM memory block as for an external RAM memory.

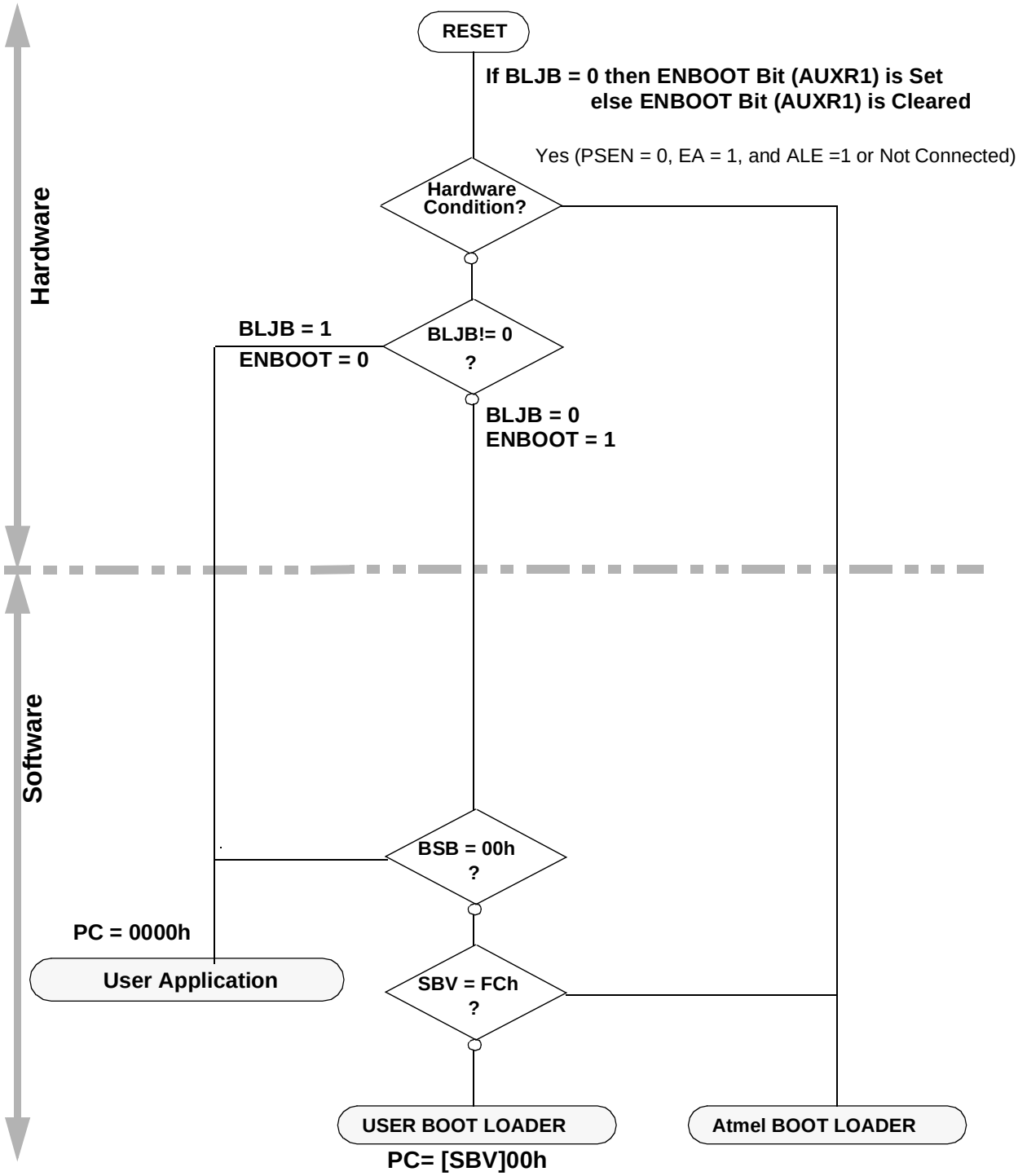
The following procedure is used to write to the EEPROM memory:

- Check EEBUSY flag
- If the user application interrupts routines use XRAM memory space: Save and disable interrupts.
- Load DPTR with the address to write
- Store A register with the data to be written
- Set bit EEE of EECON register
- Execute a MOVX @DPTR, A
- Clear bit EEE of EECON register
- Restore interrupts.
- EEBUSY flag in EECON is then set by hardware to indicate that programming is in progress and that the EEPROM segment is not available for reading or writing.
- The end of programming is indicated by a hardware clear of the EEBUSY flag.

Figure 38 represents the optimal write sequence to the on-chip EEPROM data memory.

Boot Process

Figure 44. Bootloader Process



Functional Description

Software Security Bits (SSB)

The SSB protects any Flash access from ISP command.
The command "Program Software Security Bit" can only write a higher priority level.

There are three levels of security:

- level 0: ***NO_SECURITY*** (FFh)

This is the default level.
From level 0, one can write level 1 or level 2.

- level 1: ***WRITE_SECURITY*** (FEh)

For this level it is impossible to write in the Flash memory, BSB and SBV.
The Bootloader returns 'P' on write access.
From level 1, one can write only level 2.

- level 2: ***RD_WR_SECURITY*** (FCh

The level 2 forbids all read and write accesses to/from the Flash/EEPROM memory.

The Bootloader returns 'L' on read or write access.

Only a full chip erase in parallel mode (using a programmer) or ISP command can reset the software security bits.

From level 2, one cannot read and write anything.

Table 73. Software Security Byte Behavior

	Level 0	Level 1	Level 2
Flash/EEPROM	Any access allowed	Read-only access allowed	Any access not allowed
Fuse Bit	Any access allowed	Read-only access allowed	Any access not allowed
BSB & SBV	Any access allowed	Read-only access allowed	Any access not allowed
SSB	Any access allowed	Write level 2 allowed	Read-only access allowed
Manufacturer Info	Read-only access allowed	Read-only access allowed	Read-only access allowed
Bootloader Info	Read-only access allowed	Read-only access allowed	Read-only access allowed
Erase Block	Allowed	Not allowed	Not allowed
Full Chip Erase	Allowed	Allowed	Allowed
Blank Check	Allowed	Allowed	Allowed

Full Chip Erase

The ISP command "Full Chip Erase" erases all user Flash memory (fills with FFh) and sets some bytes used by the bootloader at their default values:

- BSB = FFh
- SBV = FCh
- SSB = FFh

The Full Chip Erase does not affect the bootloader.

Checksum Error

When a checksum error is detected, send ‘X’ followed with CR&LF.

Flow Description

Overview

An initialization step must be performed after each Reset. After microcontroller reset, the bootloader waits for an autobaud sequence (see section ‘Autobaud Performances’).

When the communication is initialized, the protocol depends on the record type requested by the host.

FLIP, a software utility to implement ISP programming with a PC, is available from the Atmel web site.

Communication Initialization

The host initializes the communication by sending a ’U’ character to help the bootloader to compute the baudrate (autobaud).

Figure 46. Initialization

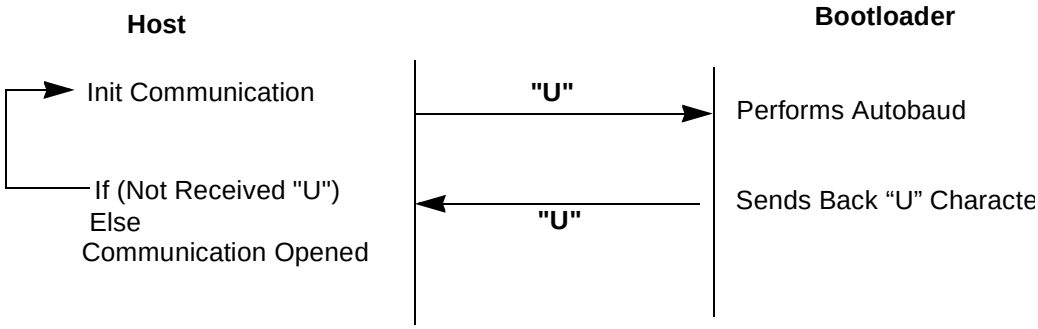
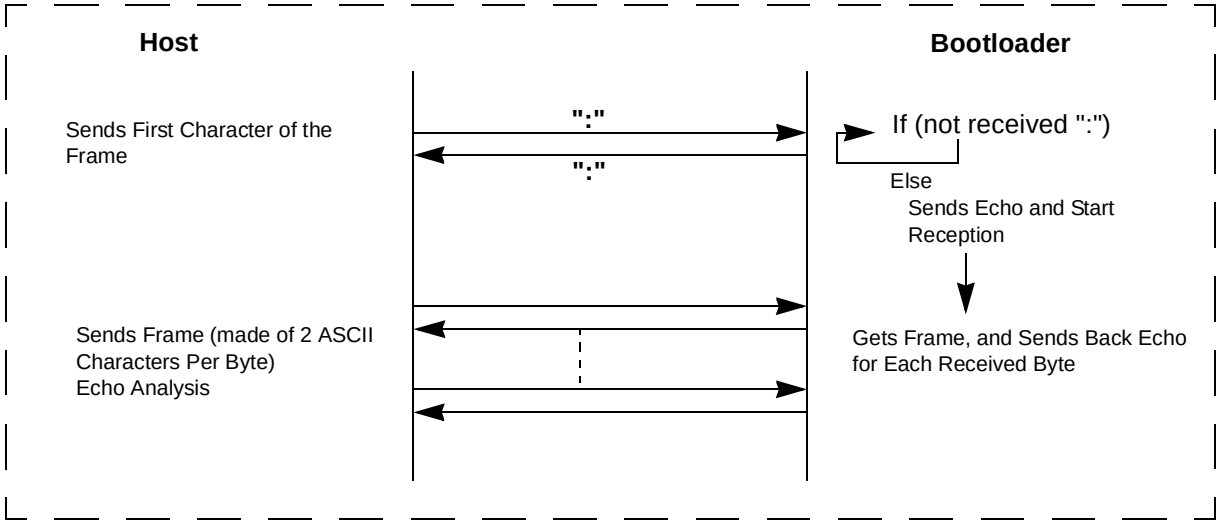


Figure 47. Command Flow

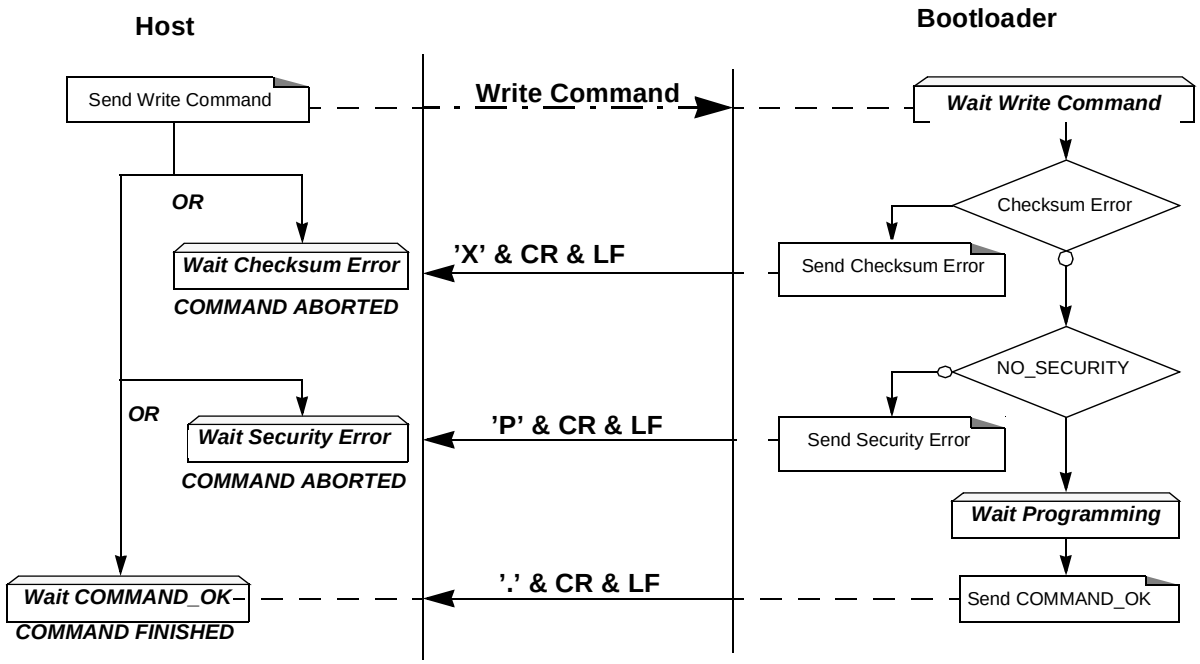


Write/Program Commands Description

This flow is common to the following frames:

- Flash/EEPROM Programming Data Frame
- EOF or Atmel Frame (only Programming Atmel Frame)
- Config Byte Programming Data Frame
- Baud Rate Frame

Figure 48. Write/Program Flow



Example

Programming Data (write 55h at address 0010h in the Flash)

```
HOST          : 01 0010 00 55 9A
BOOTLOADER    : 01 0010 00 55 9A . CR LF
```

Programming Atmel function (write SSB to level 2)

```
HOST          : 02 0000 03 05 01 F5
BOOTLOADER    : 02 0000 03 05 01 F5. CR LF
```

Writing Frame (write BSB to 55h)

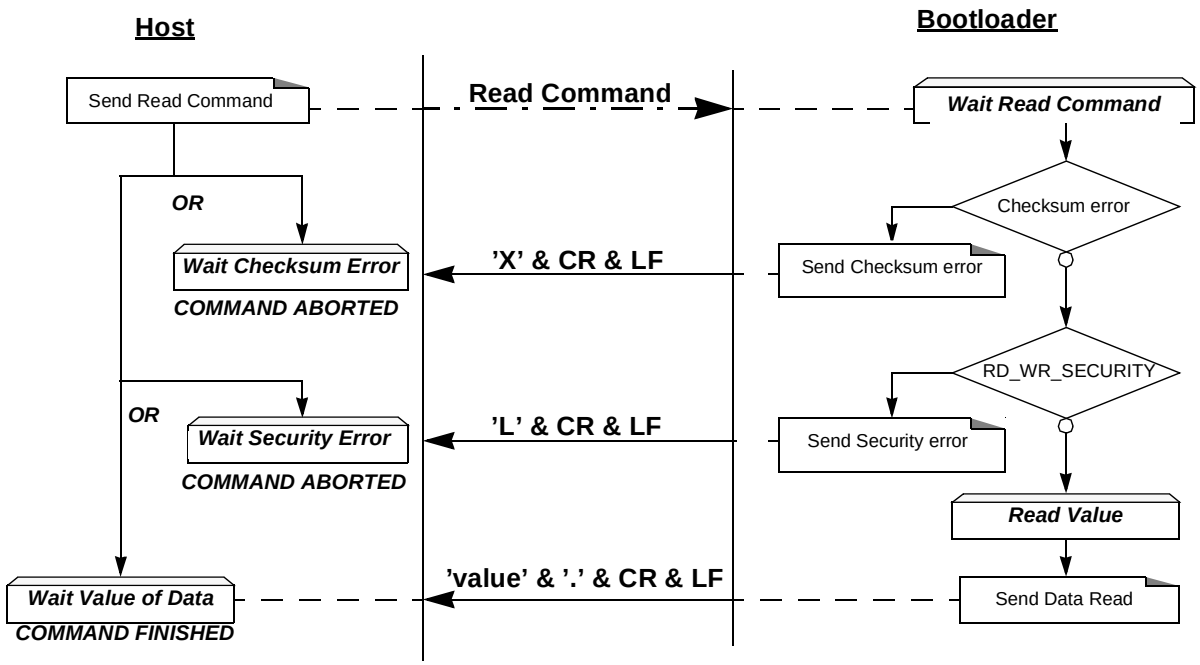
```
HOST          : 03 0000 03 06 00 55 9F
BOOTLOADER    : 03 0000 03 06 00 55 9F . CR LF
```

Read Function Description

This flow is similar for the following frames:

- Reading Frame
- EOF Frame/ Atmel Frame (only reading Atmel Frame)

Figure 51. Read Flow



Example

Read function (read SBV)

HOST : 02 0000 05 07 02 F0

BOOTLOADER : 02 0000 05 07 02 F0 Value . CR LF

Atmel Read function (read Bootloader version)

HOST : 02 0000 01 02 00 FB

BOOTLOADER : 02 0000 01 02 00 FB Value . CR LF

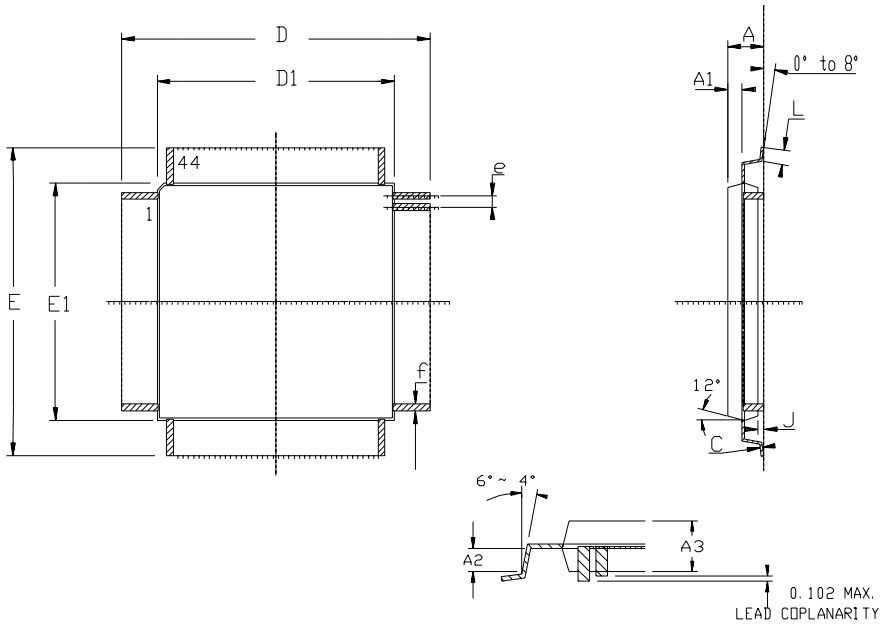
Ordering Information

Table 86. Possible Order Entries

Part Number	Data EEPROM	Supply Voltage	Temperature Range	Package	Packing	Product Marking
AT89C51RD2-SLSIM	No	2.7V - 5.5V	Industrial	PLCC44	Stick	AT89C51RD2-IM
AT89C51RD2-RLTIM				VQFP44	Tray	AT89C51RD2-IM
AT89C51RD2-RDTIM(1)				VQFP64	Tray	AT89C51RD2-IM
AT89C51RD2-SMSIM(1)				PLCC68	Stick	AT89C51RD2-IM
AT89C51ED2-SLSIM	Yes			PLCC44	Stick	AT89C51ED2-IM
AT89C51ED2-RLTIM				VQFP44	Tray	AT89C51ED2-IM
AT89C51ED2-3CSIM				PDIL40	Stick	AT89C51ED2-IM
AT89C51ED2- SMSIM				PLCC68	Stick	AT89C51ED2-IM
AT89C51ED2-RDTIM				VQFP64	Tray	AT89C51ED2-IM
AT89C51RD2-SLSUM	No	2.7V - 5.5V	Industrial & Green	PLCC44	Stick	AT89C51RD2-UM
AT89C51RD2-RLTUM				VQFP44	Tray	AT89C51RD2-UM
AT89C51RD2-RDTUM(1)				VQFP64	Tray	AT89C51RD2-UM
AT89C51RD2-SMSUM(1)				PLCC68	Stick	AT89C51RD2-UM
AT89C51ED2-SLSUM	Yes			PLCC44	Stick	AT89C51ED2-UM
AT89C51ED2-RLTUM				VQFP44	Tray	AT89C51ED2-UM
AT89C51ED2-3CSUM				PDUL40	Stick	AT89C51ED2-UM
AT89C51ED2- SMSUM				PLCC68	Stick	AT89C51ED2-UM
AT89C51ED2-RDTUM				VQFP64	Tray	AT89C51ED2-UM

Note: 1. For PLCC68 and VQFP64 packages, please contact Atmel sales office for availability.

VQFP44



	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025 REF	
A3	1.35	1.45	.053	.057
D	11.90	12.10	.468	.476
D1	9.90	10.10	.390	.398
E	11.90	12.10	.468	.476
E1	9.90	10.10	.390	.398
J	0.05	-	.002	-
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
f	0.35 BSC		.014 BSC	

Datasheet Change Log for AT89C51RD2/ED2

Changes from 4235A - 04/03 to 4135B - 06/03

1. V_{IH} min changed from 0.2 V_{CC} + 1.1 to 0.2 V_{CC} + 0.9.
2. Added POR/PFD and reset specific sections.
3. Added DIL40 package.
4. Added Flash write programming time specification.

Changes from 4235B - 06/03 to 4235C - 08/03

1. Changed maximum frequency to 60 MHz in X1 mode and 30 MHz in X2 mode for Vcc = 4.5V to 5.5V and internal code execution.
2. Added PDIL40 Packaging for AT89C51ED2.

Changes from 4235C - 08/03 to 4235D - 12/03

1. Improved explanations throughout the document.

Changes from 4235D - 12/03 to 4235E - 04/04

1. Improved explanations throughout the document.

Changes from 4235E - 04/04 to 4235F - 09/04

1. Improved explanations in Flash and EEPROM sections.

Changes from 4235F - 09/04 to 4235G 08/05

1. Added ‘Industrial & Green” product versions.

Changes from 4235G 08/05 to 4235H - 10/06

1. Correction to PDIL figure on page 9.