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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	-
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4072fbd80e

Table 2. Ordering options *…continued*

Type number	Flash (kB)	SRAM (kB)	EEPROM (B)	EMC bus width (bit)	LCD	Ethernet	USB	CAN	UART	QEI	SD/MMC	Comparator	FPU	Package
LPC4078FBD144	512	96	4032	8	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP144
LPC4078FBD100	512	96	4032	-	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP100
LPC4078FBD80	512	96	4032	-	no	yes	H/O/D	2	5	yes	no	yes	yes	LQFP80
LPC4076														
LPC4076FET180	256	80	2048	16	no	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA180
LPC4076FBD144	256	80	2048	8	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP144
LPC4074														
LPC4074FBD144	128	40	2048	-	no	no	D	2	4	no	no	no	no	LQFP144
LPC4074FBD80	128	40	2048	-	no	no	D	2	4	no	no	no	no	LQFP80
LPC4072														
LPC4072FET80	64	24	2048	-	no	no	D	2	4	no	no	no	no	TFBGA80
LPC4072FBD80	64	24	2048	-	no	no	D	2	4	no	no	no	no	LQFP80

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[23]	18	H1	F5	13	9	-	-	[5]	I; PU	I/O	**P0[23] —** General purpose digital input/output pin.
										I	**ADC0_IN[0] —** A/D converter 0, input 0. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
										I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P0[24]	16	G2	E1	11	8	-	-	[5]	I; PU	I/O	**P0[24] —** General purpose digital input/output pin.
										I	**ADC0_IN[1] —** A/D converter 0, input 1. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
										I	**T3_CAP1 —** Capture input for Timer 3, channel 1.
P0[25]	14	F1	E4	10	7	7	D1	[5]	I; PU	I/O	**P0[25] —** General purpose digital input/output pin.
										I	**ADC0_IN[2] —** A/D converter 0, input 2. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
										O	**U3_TXD —** Transmitter output for UART3.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[20]	70	U7	K6	49	34	27	J5	[3]	I; PU	I/O	**P1[20] —** General purpose digital input/output pin.
										O	**USB_TX_DP1 —** D+ transmit data for USB port 1 (OTG transceiver).
										O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
										I	**QEI_PHA —** Quadrature Encoder Interface PHA input.
										I	**MC_FB0 —** Motor control PWM channel 0 feedback input.
										I/O	**SSP0_SCK —** Serial clock for SSP0.
										O	**LCD_VD[6] —** LCD data.
										O	**LCD_VD[10] —** LCD data.
P1[21]	72	R8	N6	50	35	-	-	[3]	I; PU	I/O	**P1[21] —** General purpose digital input/output pin.
										O	**USB_TX_DM1 —** D− transmit data for USB port 1 (OTG transceiver).
										O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
										I/O	**SSP0_SSEL —** Slave Select for SSP0.
										I	**$\overline{\text{MC\_ABORT}}$ —** Motor control PWM, active low fast abort.
										-	**R —** Function reserved.
										O	**LCD_VD[7] —** LCD data.
										O	**LCD_VD[11] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[0] to P2[31]										I/O	**Port 2:** Port 2 is a 32 bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block.
P2[0]	154	B17	D12	107	75	60	B10	[3]	I; PU	I/O	**P2[0] —** General purpose digital input/output pin.
										O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
										O	**U1_TXD —** Transmitter output for UART1.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_PWR —** LCD panel power enable.
P2[1]	152	E14	C14	106	74	59	B8	[3]	I; PU	I/O	**P2[1] —** General purpose digital input/output pin.
										O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
										I	**U1_RXD —** Receiver input for UART1.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_LE —** Line end signal.
P2[2]	150	D15	E11	105	73	58	B9	[3]	I; PU	I/O	**P2[2] —** General purpose digital input/output pin.
										O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
										I	**U1_CTS —** Clear to Send input for UART1.
										O	**T2_MAT3 —** Match output for Timer 2, channel 3.
										-	**R —** Function reserved.
										O	**TRACEDATA[3] —** Trace data, bit 3.
										-	**R —** Function reserved.
										O	**LCD_DCLK —** LCD panel clock.

7.11.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.12 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral and can be accessed through the AHB master. The GPDMA controller allows data transfers between the various on-chip SRAM areas and supports the SD/MMC card interface, all SSPs, the I^2S, all UARTs, the A/D Converter, and the D/A Converter peripherals. DMA can also be triggered by selected timer match conditions. Memory-to-memory transfers and transfers to or from GPIO are supported.

7.12.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.

The I^2S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I^2S connection has one master, which is always the master, and one slave. The I^2S interface on the LPC408x/7x provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.26.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz (16, 22.05, 32, 44.1, 48) kHz.
- Configurable word select period in master mode (separately for I^2S input and output).
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I^2S input and I^2S output.

7.27 CAN controller and acceptance filters

The LPC408x/7x contain one CAN controller with two channels.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.27.1 Features

- Dual-channel CAN controller and bus.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.

7.36.4.4 Deep power-down mode

The Deep power-down mode can only be entered from the RTC block. In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

To optimize power conservation, the user has the additional option of turning off or retaining power to the 32 kHz oscillator. It is also possible to use external circuitry to turn off power to the on-chip regulator via the $V_{DD(REG)(3V3)}$ pins and/or the I/O power via the $V_{DD(3V3)}$ pins after entering Deep Power-down mode. Power must be restored before device operation can be restarted.

The LPC408x/7x can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

7.36.4.5 Wake-up Interrupt Controller (WIC)

The WIC allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep-sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC. This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

7.36.5 Peripheral power control

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

7.36.6 Power domains

The LPC408x/7x provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup registers.

On the LPC408x/7x, I/O pads are powered by $V_{DD(3V3)}$, while $V_{DD(REG)(3V3)}$ powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC408x/7x application, a design can use two power options to manage power consumption.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

Table 8. Thermal characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature		-	-	125	°C

Table 9. Thermal resistance (LQFP packages)

T_{amb} = −40 °C to +85 °C unless otherwise specified.

		Thermal resistance value (°C/W): ±15 %		
		LQFP80	**LQFP144**	**LQFP208**
θja				
	JEDEC (4.5 in × 4 in)			
	0 m/s	41	31	27
	1 m/s	35	28	25
	2.5 m/s	32	26	24
	Single-layer (4.5 in × 3 in)			
	0 m/s	61	43	35
	1 m/s	47	35	31
	2.5 m/s	43	33	29
θjc		7.8	9.2	10.5
θjb		11.6	13.5	15.2

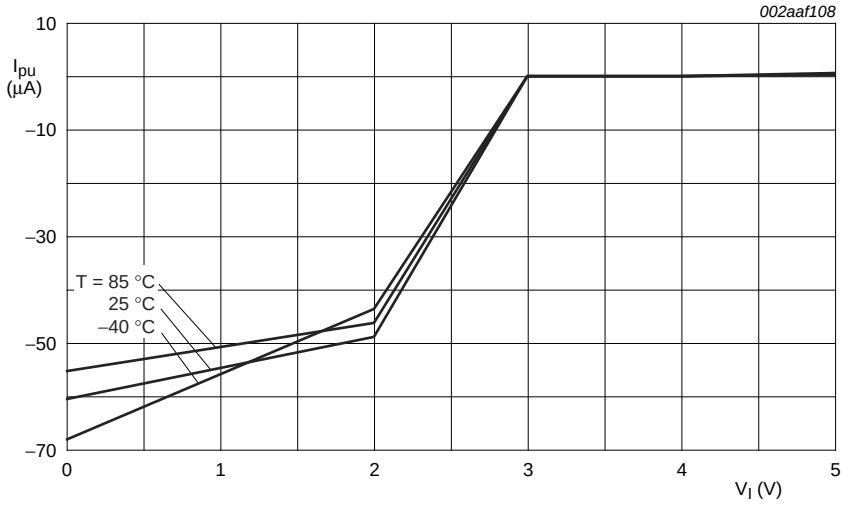
Table 10. Thermal resistance value (TFBGA packages)

T_{amb} = −40 °C to +85 °C unless otherwise specified.

		Thermal resistance value (°C/W): ±15 %	
		TFBGA180	**TFBGA208**
θja			
	JEDEC (4.5 in × 4 in)		
	0 m/s	47	43
	1 m/s	39	37
	2.5 m/s	35	33
	8-layer (4.5 in × 3 in)		
	0 m/s	39	37
	1 m/s	35	33
	2.5 m/s	31	30
θjc		8.5	7.4
θjb		13	16

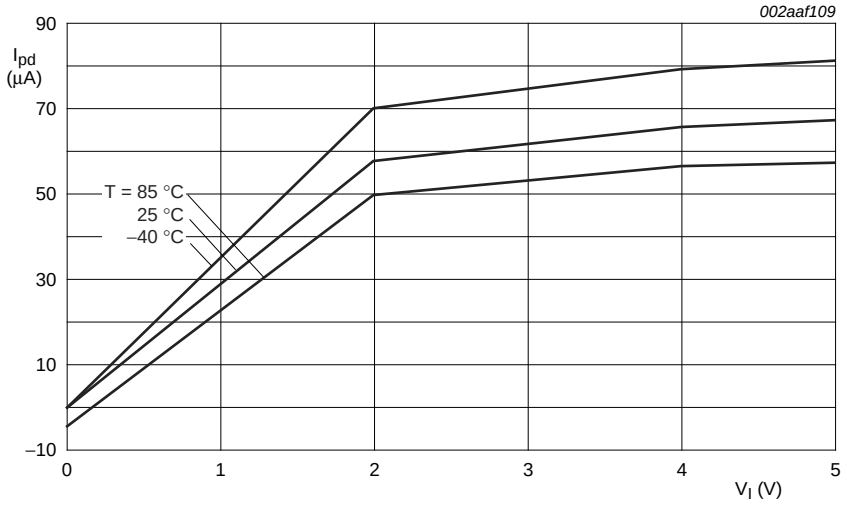
Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; on-chip pull-down resistor disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[15][16] [17]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		$V_{DD(3V3)} - 0.45$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.45	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[18]	-	-	−50	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[18]	-	-	60	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	µA
		$V_{DD(3V3)} < V_I < 5$ V		0	0	0	µA
I^2C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05 \times V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[19]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[20]	-	-	±10	µA
V_{BUS}	bus supply voltage		[20]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	[20]	0.2	-	-	V



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 17. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 18. Typical pull-down current I_{pd} versus input voltage V_I

Table 15. Dynamic characteristics: Static external memory interface *…continued*

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
t_{am}	memory access time	RD_5	[4][3]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 9.6	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 13.2	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 20.2	ns
$t_{h(D)}$	data input hold time	RD_6	[5][3]	−5.0	−7.2	–	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1		2.7	3.4	4.9	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[3]	2.4	3.1	4.2	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		[3]	0.77	1.2	1.86	ns
t_{deact}	deactivation time	RD_7	[3]	-	−4.3	−6.1	ns
Write cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		3.3	4.3	6.1	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		3.4	4.8	6.6	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[3]	2.6 + $T_{cy(clk)}$ × (1 + WAITWEN)	3.3 + $T_{cy(clk)}$ × (1 + WAITWEN)	4.6 + $T_{cy(clk)}$ × (1 + WAITWEN)	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[3]	2.7	3.5	4.9	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[3]	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 2.3	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 2.8	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 3.8	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[3]	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 2.8	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 3.5	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 5.0	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[3]	3.1 + $T_{cy(clk)}$	4.3 + $T_{cy(clk)}$	5.8 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[6][3]	$T_{cy(clk)}$ − 2.6	$T_{cy(clk)}$ − 3.4	$T_{cy(clk)}$ − 4.6	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1		3.4	4.8	6.6	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	PB = 1	[3]	3.0 + $T_{cy(clk)}$	3.8 + $T_{cy(clk)}$	5.3 + $T_{cy(clk)}$	ns
t_{deact}	deactivation time	WR_8; PB = 0; PB = 1	[3]	−3.3	−4.3	−6.1	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	WR_9; PB = 0	[3]	2.7 + $T_{cy(clk)}$ × (1 + WAITWEN)	3.5 + $T_{cy(clk)}$ × (1 + WAITWEN)	4.9 + $T_{cy(clk)}$ × (1 + WAITWEN)	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	WR_{10}; PB = 0	[3]	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 2.8	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ −3.5	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 5.0	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	WR_{11}; PB = 0	[6][3]	3.3 + $T_{cy(clk)}$	4.4 + $T_{cy(clk)}$	6.1 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	WR_{12}; PB = 0	[3]	3.4 + $T_{cy(clk)}$	4.8 + $T_{cy(clk)}$	6.6 + $T_{cy(clk)}$	ns

[1] Parameters are shown as RD_n or WD_n in Figure 19 as indicated in the Conditions column.

Table 16. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	12.5	-	-	ns
$t_{d(SV)}$	chip select valid delay time	[2]	-	$t_{clkndly}$ + 3.5	$t_{clk0dly}$ + 5.0	ns
$t_{h(S)}$	chip select hold time	[2]	$t_{clkndly}$ - 1.0	$t_{clkndly}$ - 1.2	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	[2]	-	$t_{clkndly}$ + 3.6	$t_{clkndly}$ + 5.0	ns
$t_{h(RAS)}$	row address strobe hold time	[2]	$t_{clkndly}$ - 0.8	$t_{clkndly}$ - 0.9	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	[2]	-	$t_{clkndly}$ + 3.4	$t_{clkndly}$ + 4.9	ns
$t_{h(CAS)}$	column address strobe hold time	[2]	$t_{clkndly}$ - 0.9	$t_{clkndly}$ - 1.0	-	ns
$t_{d(WV)}$	write valid delay time	[2]	-	$t_{clkndly}$ + 4.1	$t_{clkndly}$ + 6.0	ns
$t_{h(W)}$	write hold time	[2]	$t_{clkndly}$ - 0.9	$t_{clkndly}$ - 0.7		ns
$t_{d(AV)}$	address valid delay time	[2]	-	$t_{clkndly}$ + 4.6	$t_{clkndly}$ + 6.8	ns
$t_{h(A)}$	address hold time	[2]	$t_{clkndly}$ - 1.1	$t_{clkndly}$ - 1.2	-	ns
Read cycle parameters when EMC_CLKOUT0 used						
$t_{su(D)}$	data input set-up time		5.6 - t_{fbdly}	4.5 - t_{fbdly}	-	ns
$t_{h(D)}$	data input hold time		-2.2 + t_{fbdly}	-2.9 + t_{fbdly}	-	ns
Read cycle parameters when EMC_CLKOUT1 used						
$t_{su(D)}$	data input set-up time		5.6 - t_{fbdly} + ($t_{clk1dly}$ - $t_{clk0dly}$)	4.5 - t_{fbdly} + ($t_{clk1dly}$ - $t_{clk0dly}$)	-	ns
$t_{h(D)}$	data input hold time		-2.2 + t_{fbdly} - ($t_{clk1dly}$ - $t_{clk0dly}$)	-2.9 + t_{fbdly} - ($t_{clk1dly}$ - $t_{clk0dly}$)	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time	[2]	-	$t_{clkndly}$+ 5.4	$t_{clkndly}$+ 7.8	ns
$t_{h(Q)}$	data output hold time	[2]	$t_{clkndly}$ − 0.4	$t_{clkndly}$	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] $t_{clkndly}$ represents $t_{clk0dly}$ when EMC_CLKOUT0 clocks SDRAM. $t_{clkndly}$represents $t_{clk1dly}$ when EMC_CLKOUT1 clocks SDRAM.

Table 17. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1 $t_{clk0dly}$ = 0 and $t_{clk1dly}$ = 0						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	12.5	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	t_{cmddly} + 6.8	t_{cmddly} + 10.4	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 1.2	t_{cmddly} + 2.1	-	ns

11.3 External clock

Table 19. Dynamic characteristic: external clock (see Figure 40)
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency	1	-	25	MHz
$T_{cy(clk)}$	clock cycle time	40	-	1000	ns
t_{CHCX}	clock HIGH time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time	-	-	5	ns
t_{CHCL}	clock fall time	-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

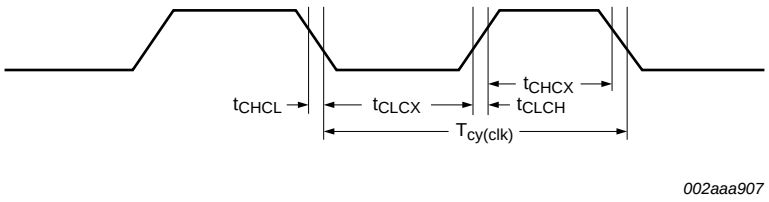


Fig 23. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.4 Internal oscillators

Table 20. Dynamic characteristic: internal oscillators
T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	11.88	12	12.12	MHz
$f_{i(RTC)}$	RTC input frequency	-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.5 I/O pins

Table 21. Dynamic characteristic: I/O pins[1]
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pin. For details, see the LPC408x/7x IBIS model available on the NXP website.

11.7 I²C-bus

Table 23. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

11.11 SPIFI

Table 27. Dynamic characteristics: SPIFI

T_{amb} = −40 °C to 85 °C; 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V; C_L = 30 pF. Values guaranteed by design.

Symbol	Parameter	Min	Max	Unit
$T_{cy(clk)}$	clock cycle time	11.8	-	ns
t_{DS}	data set-up time	4.8	-	ns
t_{DH}	data hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	8.8	ns
$t_{h(Q)}$	data output hold time	3	-	ns

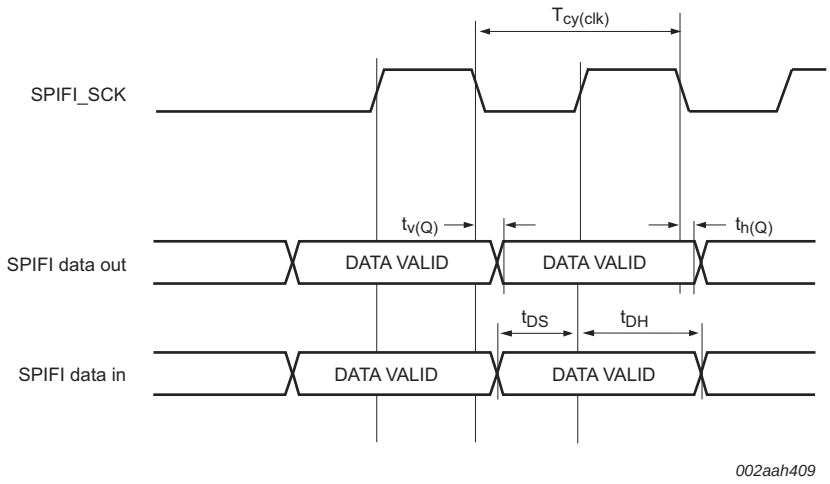


Fig 31. SPIFI timing (Mode 0)

12. Characteristics of the analog peripherals

12.1 ADC electrical characteristics

Table 28. 12-bit ADC characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
12-bit resolution							
E_D	differential linearity error		[2][3][4]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[2][5]	-	-	±6	LSB
E_O	offset error		[2][6]	-	-	±5	LSB
E_G	gain error		[2][7]	-	-	±5	LSB
E_T	absolute error		[2][8]	-	-	< ±8	LSB
$f_{clk(ADC)}$	ADC clock frequency			-	-	12.4	MHz

Table 31. Comparator characteristics *…continued*
V_{DDA}= 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DV_O	output voltage variation			0	-	V_{DDA}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V		-	–4 to +4.2	-	mV
		V_{IC} = 1.5 V		-	±2	-	mV
		V_{IC} = 2.8 V		-	±2.5		mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process		-	4	-	µs
t_{PD}	propagation delay	HIGH to LOW; V_{DDA} = 3.3 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	122	130	142	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	173	189	233	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	101	108	119	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	114	127	162	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	123	134	143	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	79	91	120	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DDA} = 3.3 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	221	232	254	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	59	63	68	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	183	229	249	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	147	174	213	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	171	192	216	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	235	305	450	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V	[2]	-	5, 10, 20	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V	[2]	-	5, 10, 20	-	mV
R_{lad}	ladder resistance	-		-	1.034	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = -40 °C to +85 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable.

Table 32. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	15	µs

[1] Maximum values are derived from worst case simulation (V_{DDA} = 2.6 V; T_{amb} = 85 °C; slow process models).

[2] Settling time applies to switching between comparator and ADC channels.

Table 33. Comparator voltage ladder reference static characteristics
V_{DDA} = 3.3 V; T_{amb} = -40 °C to + 85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	Internal V_{DDA} supply					
		decimal code = 00		0	0	0	%
		decimal code = 08		–0.45	–0.5	–0.55	%
		decimal code = 16		–0.99	–1.1	–1.21	%
		decimal code = 24		–1.26	–1.4	–1.54	%
		decimal code = 30		–1.35	–1.5	–1.65	%
		decimal code = 31		–1.35	–1.5	–1.65	%
$E_{V(O)}$	output voltage error	External VDDCMP supply					
		decimal code = 00		0	0	0	%
		decimal code = 08		0.44	0.4	0.36	%
		decimal code = 16		–0.18	–0.2	–0.22	%
		decimal code = 24		–0.45	–0.5	–0.55	%
		decimal code = 30		–0.54	–0.6	–0.66	%
		decimal code = 31		–0.45	–0.5	–0.55	%

[1] Measured on typical silicon samples with a 2 kHz input signal and overdrive < 100 μV. Power switched off to all analog peripherals except the comparator.

13. Application information

13.1 Suggested USB interface solutions

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC4088 and LPC4078/76 and as device-only controller on parts LPC4074/72.

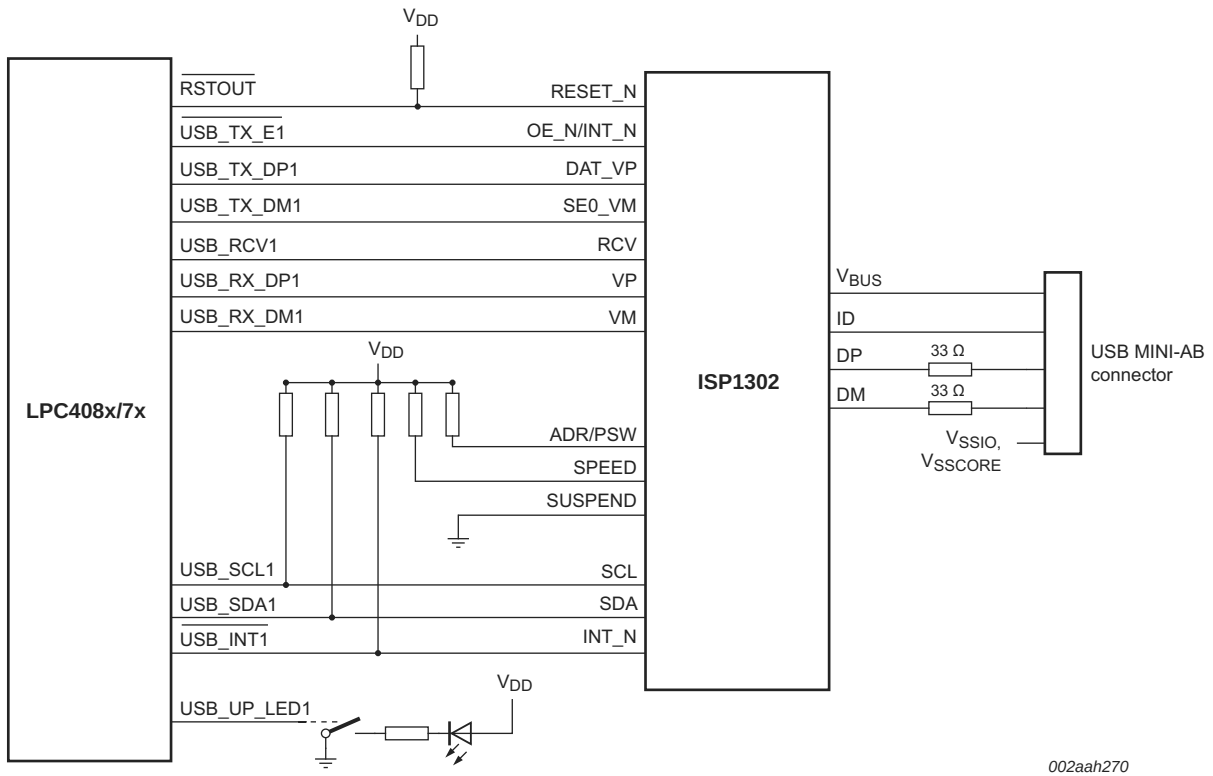
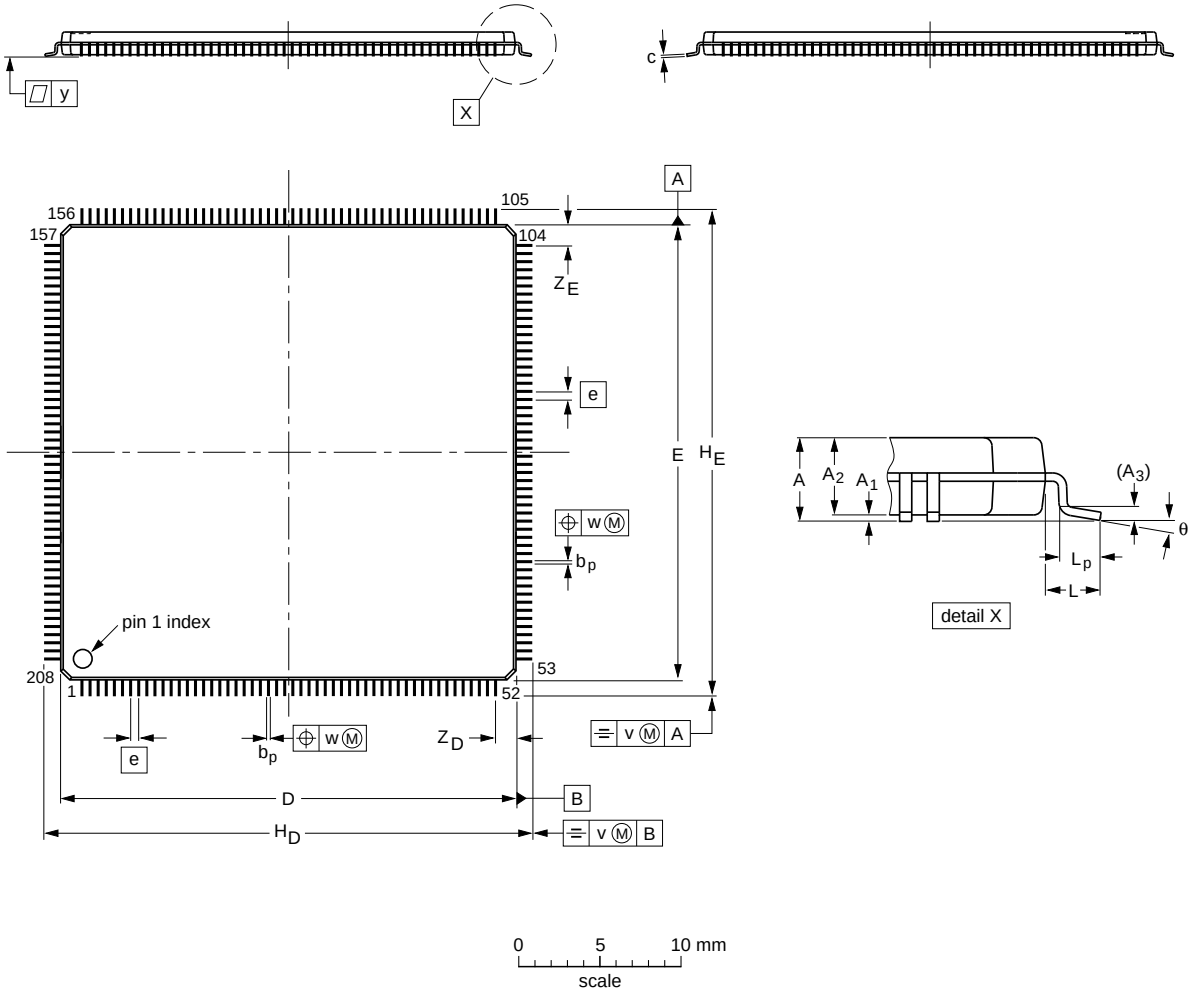


Fig 37. USB OTG port configuration: VP_VM mode

14. Package outline

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

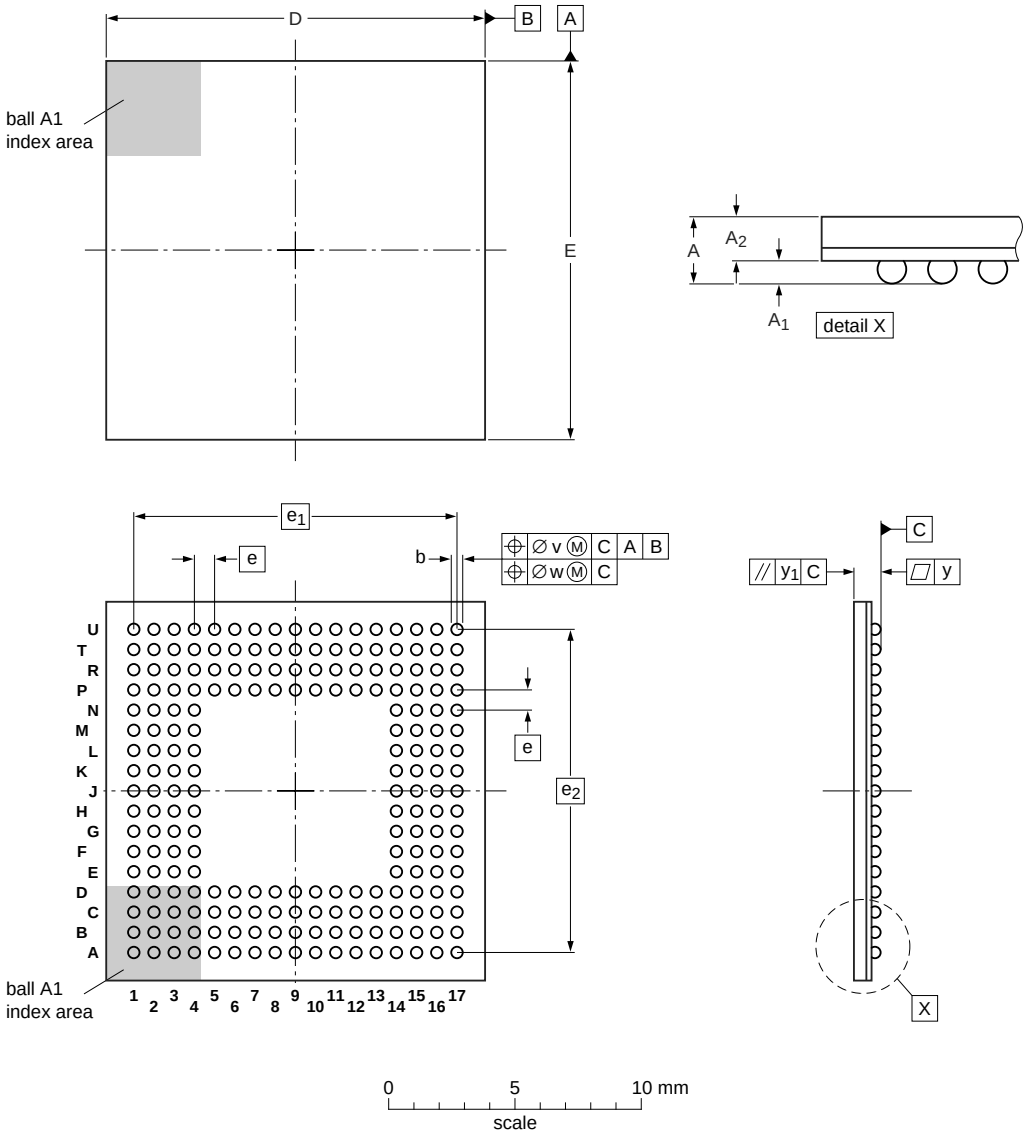
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 45. Package outline SOT459-1 (LQFP208)

TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 15 x 15 x 0.7 mm **SOT950-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.6	0.5 0.4	15.1 14.9	15.1 14.9	0.8	12.8	12.8	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT950-1		- - -				~~06-06-01~~ 06-06-14

Fig 46. Package outline SOT950-1 (TFBGA208)