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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I ² C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	-
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TFBGA
Supplier Device Package	80-TFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4072fet80k

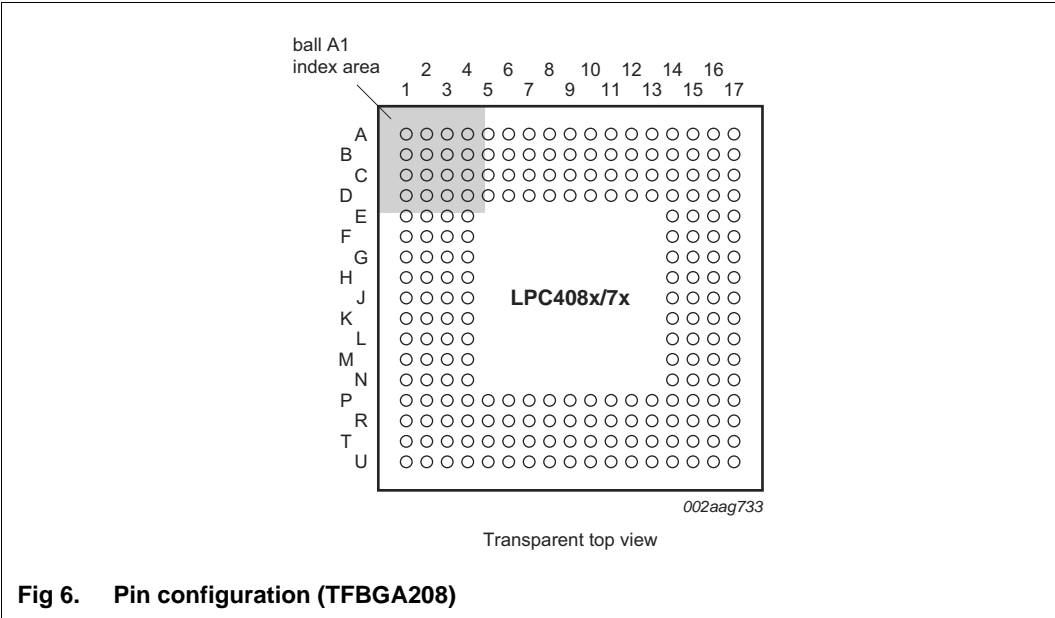
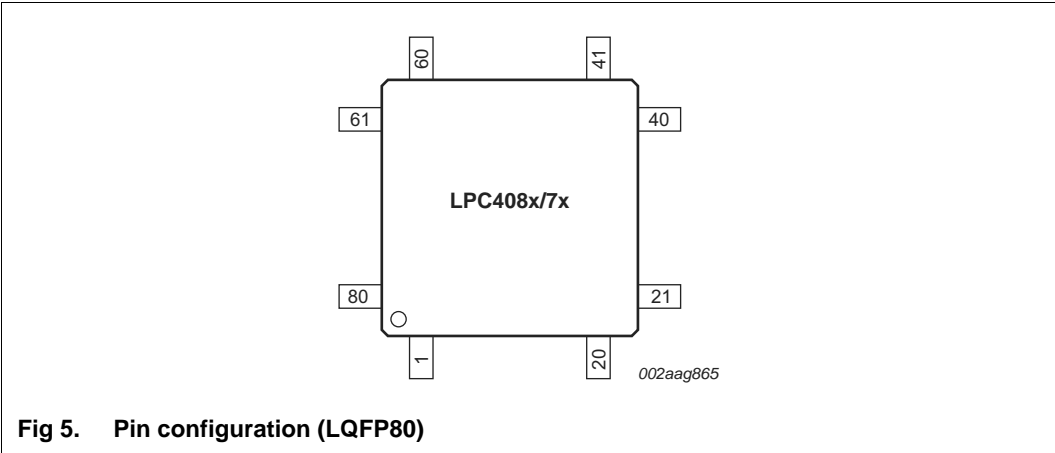


Table 3. Pin description ...continued

Not all functions are available on all parts. See [Table 2](#) (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and [Table 5](#) (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state ^[1]	Type ^[2]	Description
P0[8]	160	A15	C12	111	77	62	A10	^[4]	I; IA	I/O	P0[8] — General purpose digital input/output pin.
										I/O	I2S_TX_WS — I ² S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the <i>I²S-bus specification</i> .
										I/O	SSP1_MISO — Master In Slave Out for SSP1.
										O	T2_MAT2 — Match output for Timer 2, channel 2.
										I	RTC_EV1 — Event input 1 to Event Monitor/Recorder.
										I	CMP1_IN[3] — Comparator 1, input 3.
										-	R — Function reserved.
										O	LCD_VD[16] — LCD data.
P0[9]	158	C14	A13	109	76	61	A9	^[4]	I; IA	I/O	P0[9] — General purpose digital input/output pin.
										I/O	I2S_TX_SDA — I ² S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the <i>I²S-bus specification</i> .
										I/O	SSP1_MOSI — Master Out Slave In for SSP1.
										O	T2_MAT3 — Match output for Timer 2, channel 3.
										I	RTC_EV2 — Event input 2 to Event Monitor/Recorder.
										I	CMP1_IN[2] — Comparator 1, input 2.
										-	R — Function reserved.
										O	LCD_VD[17] — LCD data.

Table 3. Pin description ...continued

Not all functions are available on all parts. See [Table 2](#) (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and [Table 5](#) (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state ^[1]	Type ^[2]	Description
P0[20]	120	M17	K14	83	58	-	-	[3]	I; PU	I/O	P0[20] — General purpose digital input/output pin.
										O	U1_DTR — Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	SD_CMD — Command line for SD card interface.
										I/O	I2C1_SCL — I ² C1 clock input/output (this pin does not use a specialized I2C pad).
										-	R — Function reserved.
										-	R — Function reserved.
										-	R — Function reserved.
P0[21]	118	M16	K11	82	57	-	-	[3]	I; PU	O	LCD_VD[14] — LCD data.
										I/O	P0[21] — General purpose digital input/output pin.
										I	U1_RI — Ring Indicator input for UART1.
										O	SD_PWR — Power Supply Enable for external SD card power supply.
										O	U4_OE — RS-485/EIA-485 output enable signal for UART4.
										I	CAN_RD1 — CAN1 receiver input.
P0[22]	116	N17	L14	80	56	44	H10	[6]	I; PU	I/O	U4_SCLK — USART 4 clock input or output in synchronous mode.
										I/O	P0[22] — General purpose digital input/output pin.
										O	U1_RTS — Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	SD_DAT[0] — Data line 0 for SD card interface.
										O	U4_TXD — Transmitter output for USART4 (input/output in smart card mode).
										O	CAN_TD1 — CAN1 transmitter output.
										O	SPIFI_CLK — Clock output for SPIFI.

Table 3. Pin description ...continued

Not all functions are available on all parts. See [Table 2](#) (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and [Table 5](#) (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state ^[1]	Type ^[2]	Description
P1[18]	66	P7	L5	46	32	25	K4	[3]	I; PU	I/O	P1[18] — General purpose digital input/output pin.
										O	USB_UP_LED1 — It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
										O	PWM1[1] — Pulse Width Modulator 1, channel 1 output.
										I	T1_CAP0 — Capture input for Timer 1, channel 0.
										-	R — Function reserved.
P1[19]	68	U6	P5	47	33	26	J4	[3]	I; PU	I/O	SSP1_MISO — Master In Slave Out for SSP1.
										I/O	P1[19] — General purpose digital input/output pin.
										O	USB_TX_E1 — Transmit Enable signal for USB port 1 (OTG transceiver).
										O	USB_PPWR1 — Port Power enable signal for USB port 1.
										I	T1_CAP1 — Capture input for Timer 1, channel 1.
										O	MC_0A — Motor control PWM channel 0, output A.
										I/O	SSP1_SCK — Serial clock for SSP1.
										O	U2_OE — RS-485/EIA-485 output enable signal for UART2.

Table 3. Pin description ...continued

Not all functions are available on all parts. See [Table 2](#) (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and [Table 5](#) (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state ^[1]	Type ^[2]	Description
P1[29]	92	U14	N10	64	45	36	K8	[3]	I; PU	I/O	P1[29] — General purpose digital input/output pin.
										I/O	USB_SDA1 — USB port 1 I ² C serial data (OTG transceiver).
										I	PWM1_CAP1 — Capture input for PWM1, channel 1.
										O	T0_MAT1 — Match output for Timer 0, channel 1.
										O	MC_2B — Motor control PWM channel 2, output B.
										O	U4_TXD — Transmitter output for USART4 (input/output in smart card mode).
										O	LCD_VD[15] — LCD data.
P1[30]	42	P2	K3	30	21	18	J2	[5]	I; PU	O	LCD_VD[23] — LCD data.
										I/O	P1[30] — General purpose digital input/output pin.
										I	USB_PWRD2 — Power Status for USB port 2.
										I	USB_VBUS — Monitors the presence of USB bus power. This signal must be HIGH for USB reset to occur.
										I	ADC0_IN[4] — A/D converter 0, input 4. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	I2C0_SDA — I ² C0 data input/output (this pin does not use a specialized I2C pad).
P1[31]	40	P1	K2	28	20	17	H2	[5]	I; PU	O	U3_OE — RS-485/EIA-485 output enable signal for UART3.
										I/O	P1[31] — General purpose digital input/output pin.
										I	USB_OVRCR2 — Over-Current status for USB port 2.
										I/O	SSP1_SCK — Serial Clock for SSP1.
										I	ADC0_IN[5] — A/D converter 0, input 5. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	I2C0_SCL — I ² C0 clock input/output (this pin does not use a specialized I2C pad).

Table 3. Pin description ...continued

Not all functions are available on all parts. See [Table 2](#) (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and [Table 5](#) (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state ^[1]	Type ^[2]	Description
P3[9]	199	C5	A4	-	-	-	-	[3]	I; PU	I/O	P3[9] — General purpose digital input/output pin.
										I/O	EMC_D[9] — External memory data line 9.
P3[10]	205	B2	B3	-	-	-	-	[3]	I; PU	I/O	P3[10] — General purpose digital input/output pin.
										I/O	EMC_D[10] — External memory data line 10.
P3[11]	208	D5	B2	-	-	-	-	[3]	I; PU	I/O	P3[11] — General purpose digital input/output pin.
										I/O	EMC_D[11] — External memory data line 11.
P3[12]	1	D4	A1	-	-	-	-	[3]	I; PU	I/O	P3[12] — General purpose digital input/output pin.
										I/O	EMC_D[12] — External memory data line 12.
P3[13]	7	C1	C1	-	-	-	-	[3]	I; PU	I/O	P3[13] — General purpose digital input/output pin.
										I/O	EMC_D[13] — External memory data line 13.
P3[14]	21	H2	F1	-	-	-	-	[3]	I; PU	I/O	P3[14] — General purpose digital input/output pin.
										I/O	EMC_D[14] — External memory data line 14.
P3[15]	28	M1	G4	-	-	-	-	[3]	I; PU	I/O	P3[15] — General purpose digital input/output pin.
										I/O	EMC_D[15] — External memory data line 15.
P3[16]	137	F17	-	-	-	-	-	[3]	I; PU	I/O	P3[16] — General purpose digital input/output pin.
										I/O	EMC_D[16] — External memory data line 16.
										O	PWM0[1] — Pulse Width Modulator 0, output 1.
										O	U1_TXD — Transmitter output for UART1.
P3[17]	143	F15	-	-	-	-	-	[3]	I; PU	I/O	P3[17] — General purpose digital input/output pin.
										I/O	EMC_D[17] — External memory data line 17.
										O	PWM0[2] — Pulse Width Modulator 0, output 2.
										I	U1_RXD — Receiver input for UART1.
P3[18]	151	C15	-	-	-	-	-	[3]	I; PU	I/O	P3[18] — General purpose digital input/output pin.
										I/O	EMC_D[18] — External memory data line 18.
										O	PWM0[3] — Pulse Width Modulator 0, output 3.
										I	U1_CTS — Clear to Send input for UART1.

7.16 USB interface

Remark: The USB Device/Host/OTG controller is available on parts LPC4088/78/76. The USB Device-only controller is available on part LPC4074/72.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

See [Section 13.1](#) for details on typical USB interfacing solutions.

7.16.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the USB RAM.

7.16.1.1 Features

- Fully compliant with *USB 2.0 Specification* (full speed).
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the LPC408x/7x can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

7.16.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

7.16.2.1 Features

- OHCI compliant.
- Two downstream ports.
- Supports per-port power switching.

7.36.3 Wake-up timer

The LPC408x/7x begin operation at power-up and when awakened from Power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up Timer.

The wake-up timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

7.36.4 Power control

The LPC408x/7x support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, the peripheral power control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.

The LPC408x/7x also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

7.36.4.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.36.4.4 Deep power-down mode

The Deep power-down mode can only be entered from the RTC block. In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

To optimize power conservation, the user has the additional option of turning off or retaining power to the 32 kHz oscillator. It is also possible to use external circuitry to turn off power to the on-chip regulator via the $V_{\text{DD(REG)(3V3)}}$ pins and/or the I/O power via the $V_{\text{DD(3V3)}}$ pins after entering Deep Power-down mode. Power must be restored before device operation can be restarted.

The LPC408x/7x can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

7.36.4.5 Wake-up Interrupt Controller (WIC)

The WIC allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep-sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC. This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

7.36.5 Peripheral power control

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

7.36.6 Power domains

The LPC408x/7x provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup registers.

On the LPC408x/7x, I/O pads are powered by $V_{\text{DD(3V3)}}$, while $V_{\text{DD(REG)(3V3)}}$ powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC408x/7x application, a design can use two power options to manage power consumption.

The first option assumes that power consumption is not a concern and the design ties the $V_{\text{DD(3V3)}}$ and $V_{\text{DD(REG)(3V3)}}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

Table 11. Static characteristics ...continued
 $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ ^[1]	Max	Unit
V_{CM}	differential common mode voltage range	includes V_{DI} range	[20]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[20]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 k Ω to 3.6 V	[20]	-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 k Ω to GND	[20]	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	[20]	-	-	20	pF
Oscillator pins (see Section 13.2)							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			-0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			-0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			-0.5	-	3.6	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			-0.5	-	3.6	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation $3.0\text{ V} \leq V_{DD(3V3)} \leq 3.6\text{ V}$. Guaranteed by design.

[3] V_{DDA} and V_{REFP} should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[4] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[5] $V_{DD(REG)(3V3)} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$ for all power consumption measurements.

[6] Boost control bits in the PBOOST register set to 0x0 (see *LPC408x/7x User manual*).

[7] Boost control bits in the PBOOST register set to 0x3 (see *LPC408x/7x User manual*).

[8] IRC running at 12 MHz; main oscillator and PLL disabled; PCLK = CCLK/4.

[9] BOD disabled.

[10] On pin VBAT; $V_{DD(REG)(3V3)} = V_{DD(3V3)} = V_{DDA} = 0$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[11] On pin VBAT; $V_{DD(REG)(3V3)} = V_{DD(3V3)} = V_{DDA} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[12] All internal pull-ups disabled. All pins configured as output and driven LOW. $V_{DD(3V3)} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[13] $V_{DDA} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[14] $V_{i(VREFP)} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[15] Including voltage on outputs in 3-state mode.

[16] $V_{DD(3V3)}$ supply voltages must be present.

[17] 3-state outputs go into 3-state mode in Deep power-down mode.

[18] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[19] To V_{SS} .

[20] $3.0\text{ V} \leq V_{DD(3V3)} \leq 3.6\text{ V}$.

10.1 Power consumption

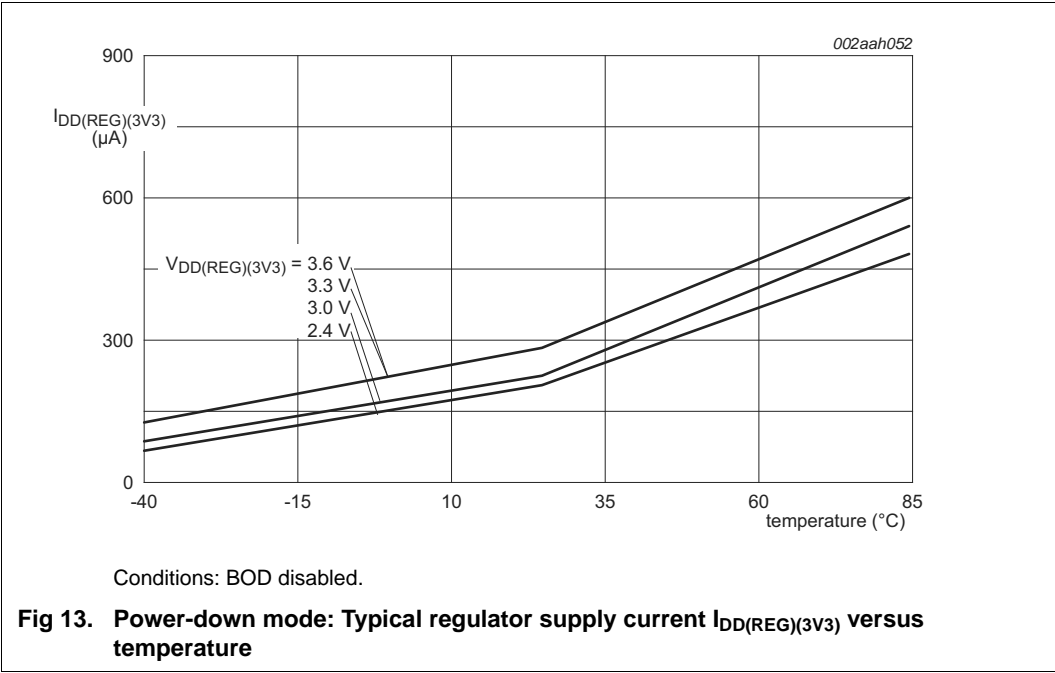
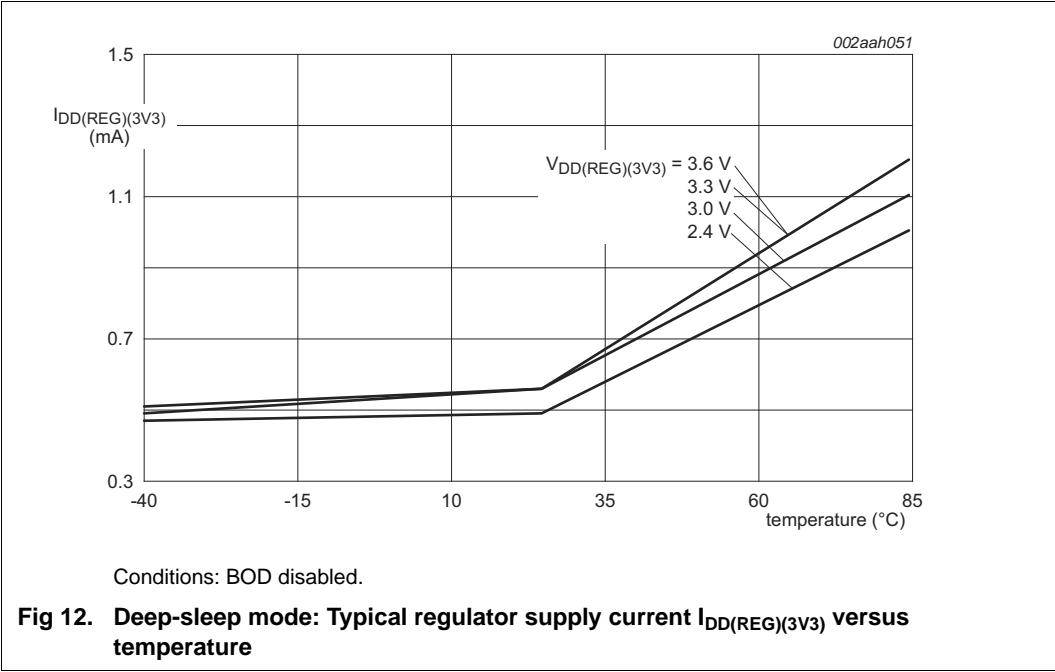


Table 17. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01 ...continued
 $C_L = 30\text{ pF}$, $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, $V_{DD(3V3)} = 3.0\text{ V}$ to 3.6 V . Values guaranteed by design. t_{cmdly} is programmable delay value for EMC command outputs in command delayed mode; t_{fdbly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
$t_{d(RASV)}$	row address strobe valid delay time		-	$t_{cmdly} + 6.8$	$t_{cmdly} + 10.4$	ns
$t_{h(RAS)}$	row address strobe hold time		$t_{cmdly} + 2.3$	$t_{cmdly} + 4.3$	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	$t_{cmdly} + 6.7$	$t_{cmdly} + 10.2$	ns
$t_{h(CAS)}$	column address strobe hold time		$t_{cmdly} + 2.2$	$t_{cmdly} + 4.1$	-	ns
$t_{d(WV)}$	write valid delay time		-	$t_{cmdly} + 7.1$	$t_{cmdly} + 10.9$	ns
$t_{h(W)}$	write hold time		$t_{cmdly} + 1.5$	$t_{cmdly} + 2.7$	-	ns
$t_{d(AV)}$	address valid delay time		-	$t_{cmdly} + 7.7$	$t_{cmdly} + 11.9$	ns
$t_{h(A)}$	address hold time		$t_{cmdly} + 1.0$	$t_{cmdly} + 1.8$	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		$5.6 - t_{fdbly}$	$4.5 - t_{fdbly}$	-	ns
$t_{h(D)}$	data input hold time		$-2.2 + t_{fdbly}$	$-2.9 + t_{fdbly}$	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	$t_{cmdly} + 8.7$	$t_{cmdly} + 13.1$	ns
$t_{h(Q)}$	data output hold time		$t_{cmdly} + 1.0$	$t_{cmdly} + 2.0$	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

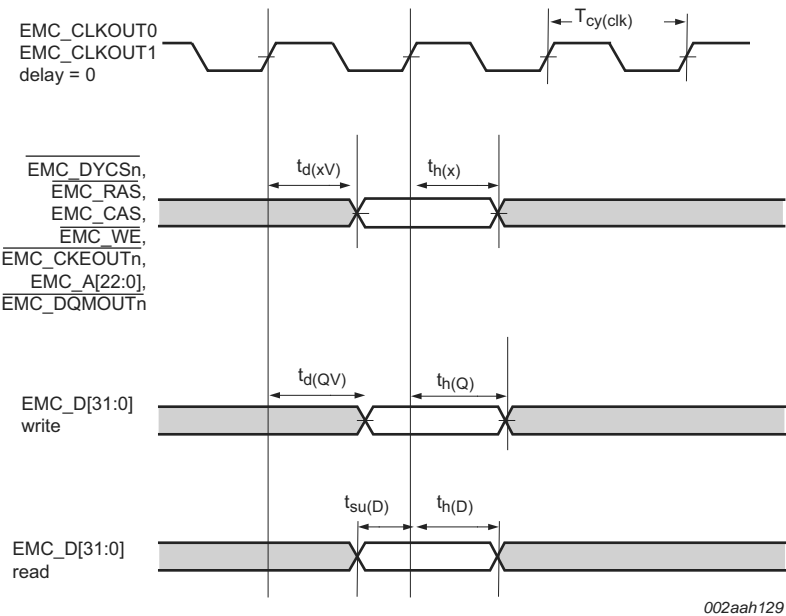


Fig 22. Dynamic external memory interface signal timing

Table 18. Dynamic characteristics: Dynamic external memory interface programmable clock delays (CMDDLY, FBCLKDLY, CLKOUT0DLY and CLKOUT1DLY)

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, $V_{DD(3V3)} = 3.0\text{ V}$ to 3.6 V . Values guaranteed by design. t_{cmdly} is programmable delay value for EMC command outputs in command delayed mode; t_{fdbly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbols	Parameter	Five bit value for each delay in EMCDLYCTL ^[1]	Min	Typ	Max	Unit
t_{cmdly} , t_{fdbly} , $t_{clk0dly}$, $t_{clk1dly}$	delay time	b00000	0.0	0.0	0.0	ns
		b00001	0.1	0.1	0.2	ns
		b00010	0.2	0.3	0.5	ns
		b00011	0.3	0.4	0.7	ns
		b00100	0.5	0.8	1.3	ns
		b00101	0.6	0.9	1.5	ns
		b00110	0.7	1.1	1.8	ns
		b00111	0.8	1.2	2.0	ns
		b01000	1.2	1.8	2.9	ns
		b01001	1.3	1.9	3.1	ns
		b01010	1.4	2.0	3.4	ns
		b01011	1.5	2.1	3.6	ns
		b01100	1.7	2.6	4.2	ns
		b01101	1.8	2.7	4.4	ns
		b01110	1.9	2.9	4.7	ns
		b01111	2.0	3.0	4.9	ns
		b10000	2.4	3.7	6.0	ns
		b10001	2.5	3.8	6.2	ns
		b10010	2.6	4.0	6.5	ns
		b10011	2.7	4.1	6.7	ns
		b10100	2.9	4.5	7.3	ns
		b10101	3.0	4.6	7.5	ns
		b10110	3.1	4.8	7.8	ns
		b10111	3.2	4.9	8.0	ns
		b11000	3.6	5.4	8.9	ns
		b11001	3.7	5.5	9.1	ns
		b11010	3.8	5.7	9.4	ns
		b11011	3.9	5.8	9.6	ns
		b11100	4.1	6.2	10.2	ns
		b11101	4.2	6.3	10.4	ns
		b11110	4.3	6.6	10.7	ns
		b11111	4.4	6.7	10.9	ns

[1] The programmable delay blocks are controlled by the EMCDLYCTL register in the EMC register block. All delay times are incremental delays for each element starting from delay block 0. See the *LPC408x/7x user manual* for details.

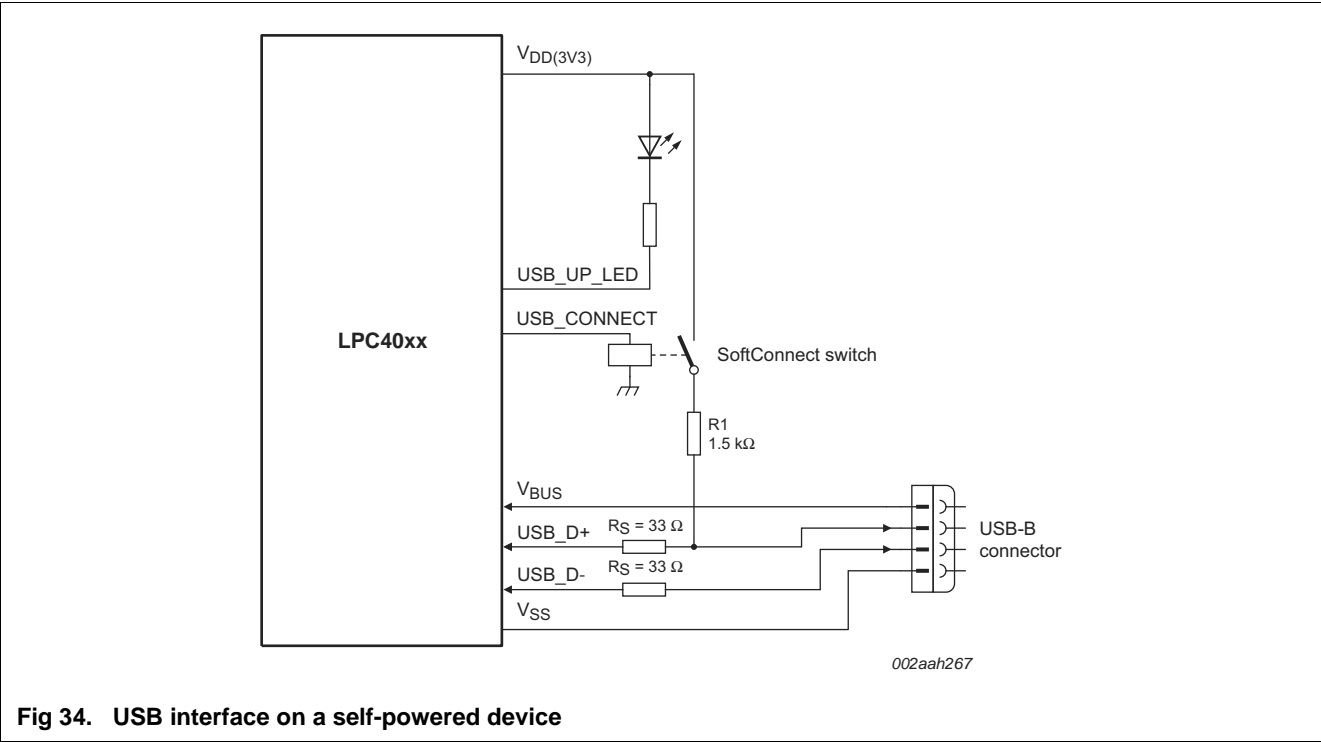


Fig 34. USB interface on a self-powered device

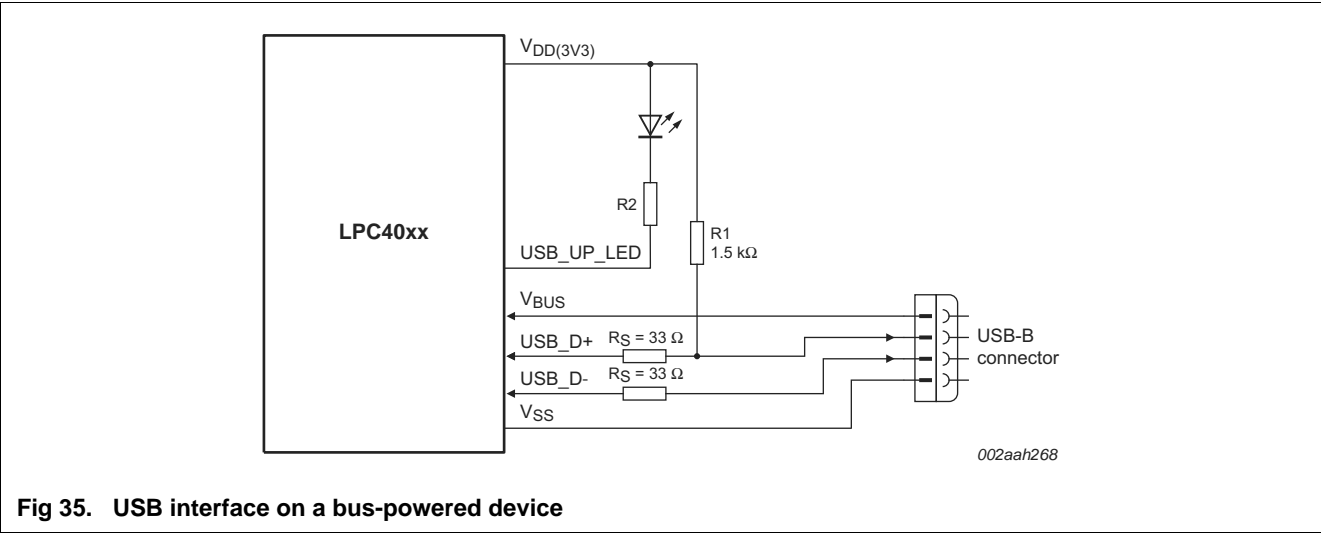
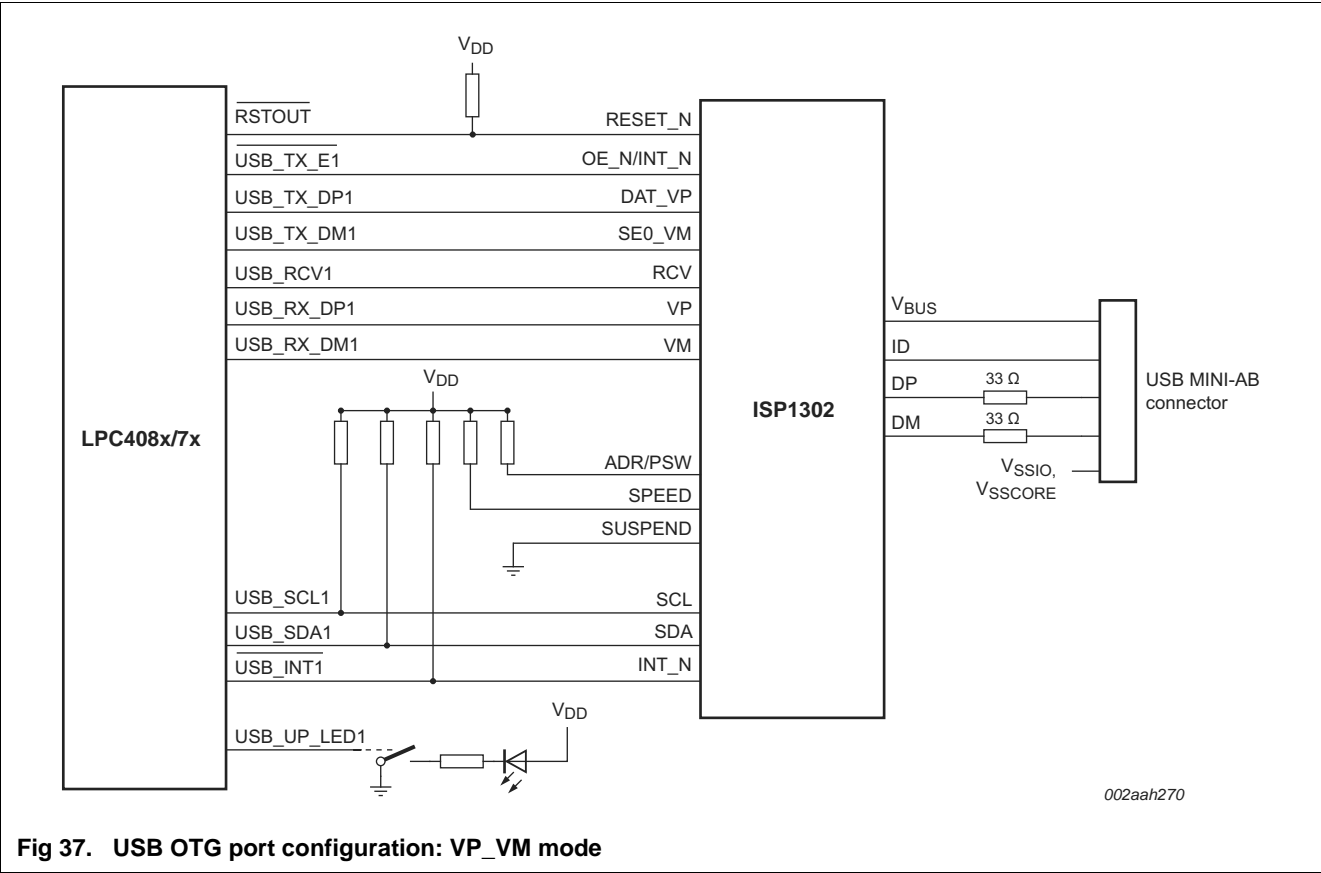


Fig 35. USB interface on a bus-powered device



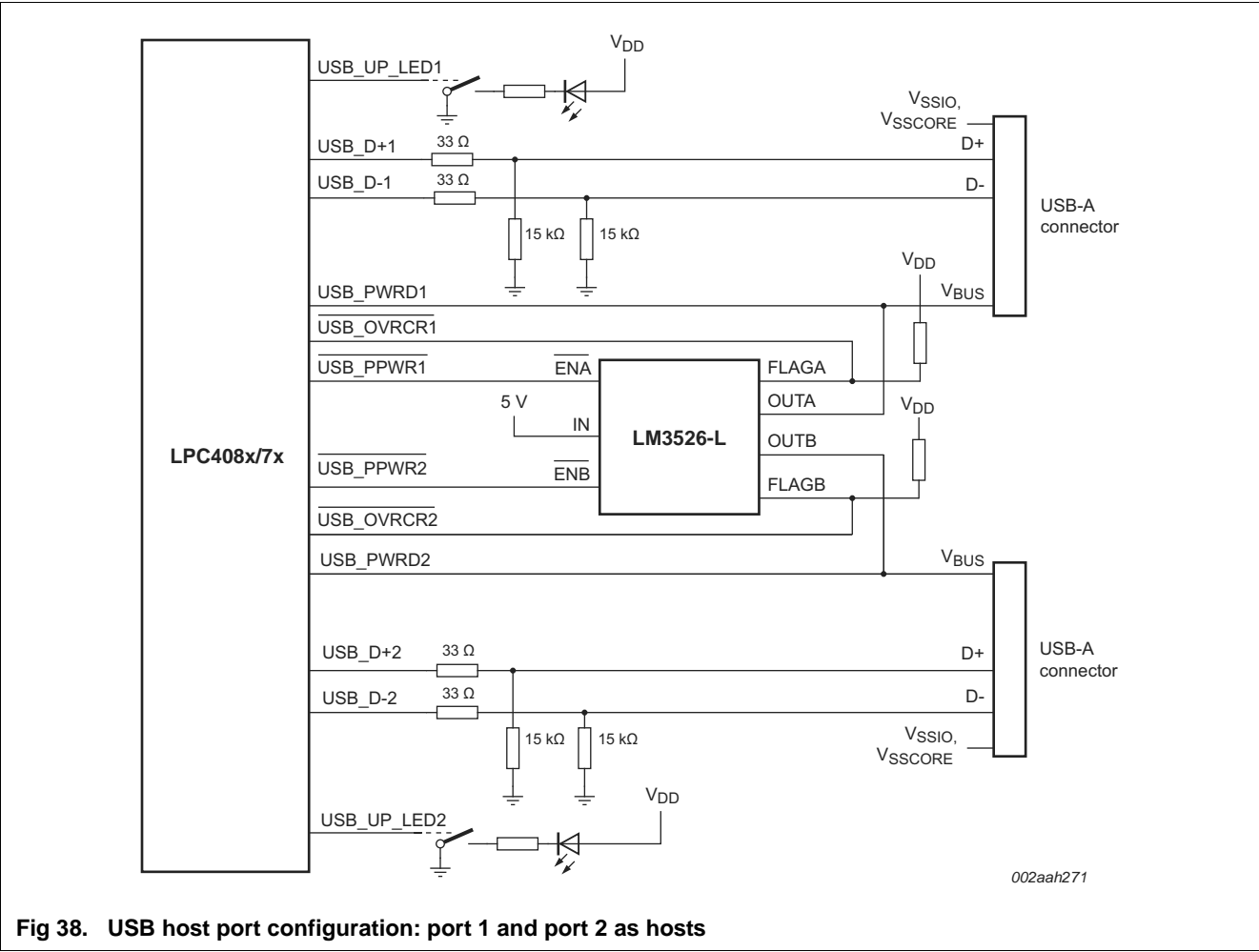
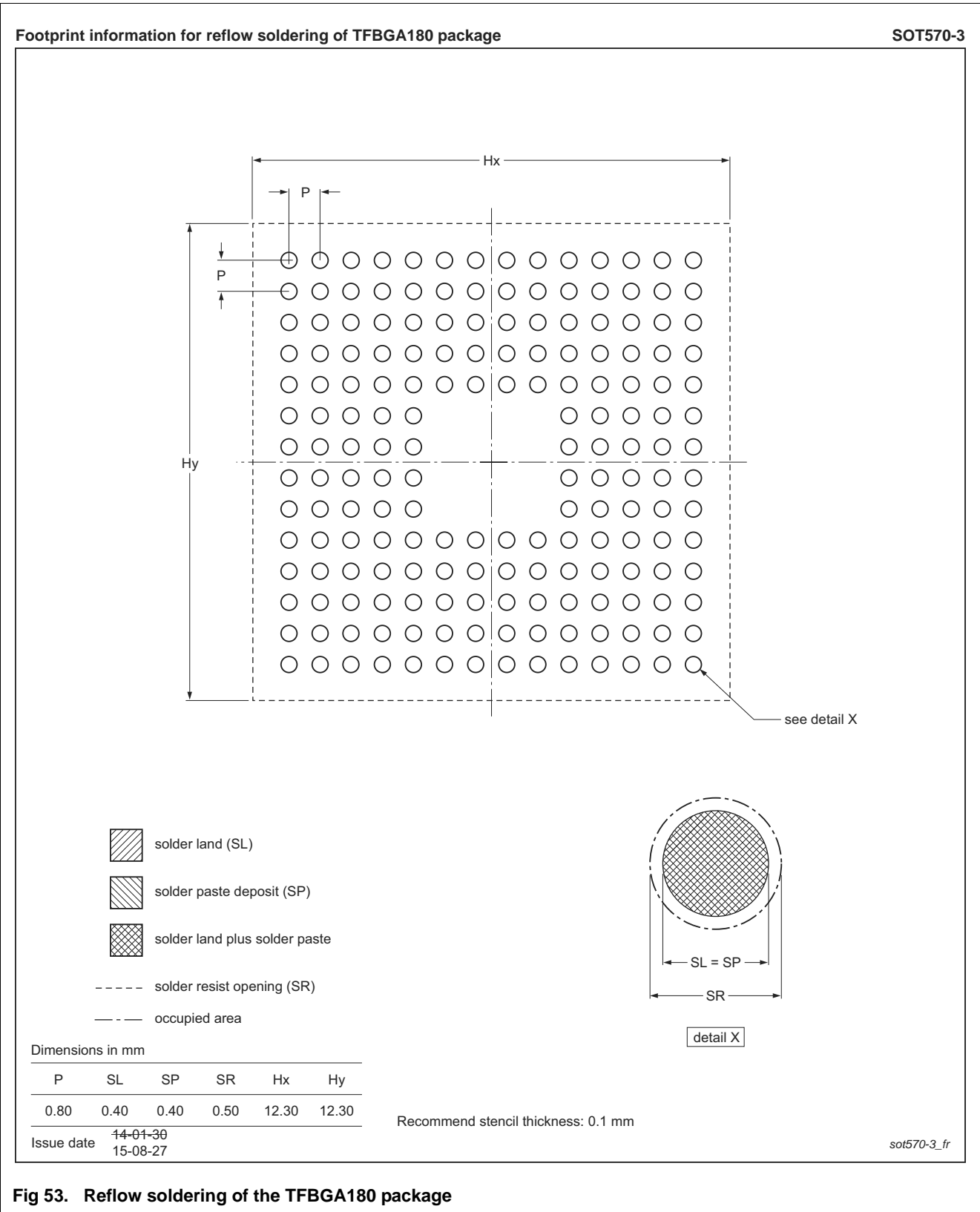


Fig 38. USB host port configuration: port 1 and port 2 as hosts



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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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