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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	-
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4074fbd144-551

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC4088			
LPC4088FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4088FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 × 15 × 0.7 mm	SOT950-1
LPC4088FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC4088FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4078			
LPC4078FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4078FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 × 15 × 0.7 mm	SOT950-1
LPC4078FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC4078FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4078FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC4078FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC4076			
LPC4076FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC4076FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4074			
LPC4074FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4074FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC4072			
LPC4072FET80	TFBGA80	plastic thin fine-pitch ball grid array package; 80 balls	SOT1328-1
LPC4072FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)	EEPROM (B)	EMC bus width (bit)	LCD	Ethernet	USB	CAN	UART	QEI	SD/MMC	Comparator	FPU	Package
LPC4088														
LPC4088FBD208	512	96	4032	32	yes	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP208
LPC4088FET208	512	96	4032	32	yes	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA208
LPC4088FET180	512	96	4032	16	yes	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA180
LPC4088FBD144	512	96	4032	8	yes	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP144
LPC4078														
LPC4078FBD208	512	96	4032	32	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP208
LPC4078FET208	512	96	4032	32	no	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA208
LPC4078FET180	512	96	4032	16	no	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA180

6. Pinning information

6.1 Pinning

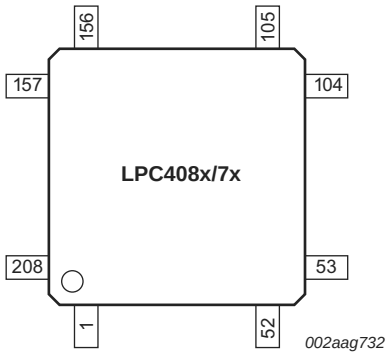


Fig 2. Pin configuration (LQFP208)

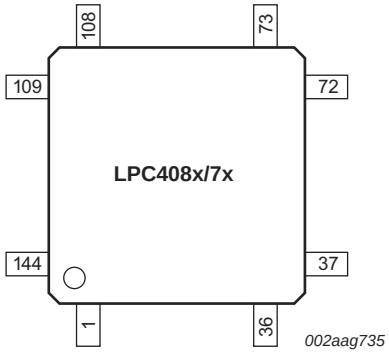


Fig 3. Pin configuration (LQFP144)

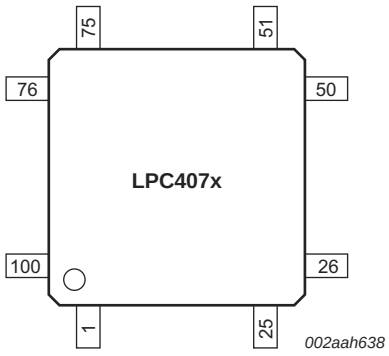


Fig 4. Pin configuration (LQFP100)

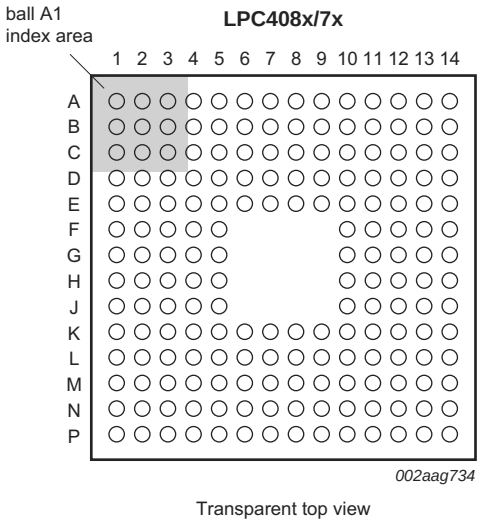


Fig 7. Pin configuration (TFBGA180)

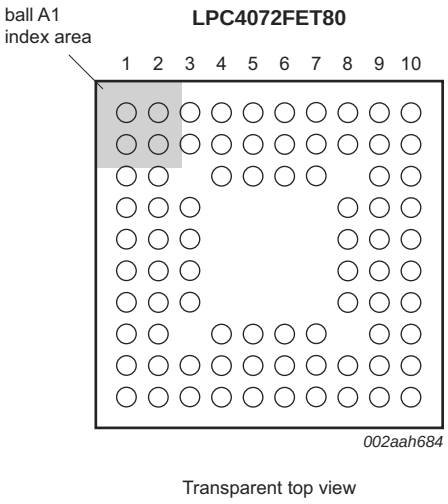


Fig 8. Pin configuration (TFBGA80)

6.2 Pin description

I/O pins on the LPC408x/7x are 5 V tolerant and have input hysteresis unless otherwise indicated in the table below. Crystal pins, power pins, and reference voltage pins are not 5 V tolerant. In addition, when pins are selected to be ADC inputs, they are no longer 5 V tolerant and the input voltage must be limited to the voltage at the ADC positive reference pin (VREFP).

All port pins Pn[m] are multiplexed, and the multiplexed functions appear in Table 3 in the order defined by the FUNC bits of the corresponding IOCON register up to the highest used function number. Each port pin can support up to eight multiplexed functions. IOCON register FUNC values which are reserved are noted as “R” in the pin configuration table.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[13]	45	R2	J5	32	-	-	-	[5]	I; PU	I/O	**P0[13] —** General purpose digital input/output pin.
										O	**USB_UP_LED2 —** USB port 2 GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
										I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
										I	**ADC0_IN[7] —** A/D converter 0, input 7. When configured as an ADC input, the digital function of the pin must be disabled.
P0[14]	69	T7	M5	48	-	-	-	[3]	I; PU	I/O	**P0[14] —** General purpose digital input/output pin.
										O	**USB_HSTEN2 —** Host Enabled status for USB port 2.
										I/O	**SSP1_SSEL —** Slave Select for SSP1.
										O	**USB_CONNECT2 —** SoftConnect control for USB port 2. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
P0[15]	128	J16	H13	89	62	47	F9	[3]	I; PU	I/O	**P0[15] —** General purpose digital input/output pin.
										O	**U1_TXD —** Transmitter output for UART1.
										I/O	**SSP0_SCK —** Serial clock for SSP0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I/O	**SPIFI_IO[2] —** Data bit 0 for SPIFI.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[14]	184	A7	D8	128	89	70	C6	[3]	I; PU	I/O	**P1[14] —** General purpose digital input/output pin.
										I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
										-	**R —** Function reserved.
										I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
										-	**R —** Function reserved.
										I	**CMP0_IN[0] —** Comparator 0, input 0.
P1[15]	182	A8	A8	126	88	69	B6	[3]	I; PU	I/O	**P1[15] —** General purpose digital input/output pin.
										I	**ENET_RX_CLK (ENET_REF_CLK) —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
										-	**R —** Function reserved.
										I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
P1[16]	180	D10	B8	125	87	-	-	[3]	I; PU	I/O	**P1[16] —** General purpose digital input/output pin.
										O	**ENET_MDC —** Ethernet MIIM clock.
										O	**I2S_TX_MCLK —** I2S transmit master clock.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I	**CMP0_IN[1] —** Comparator 0, input 1.
P1[17]	178	A9	C9	123	86	-	-	[3]	I; PU	I/O	**P1[17] —** General purpose digital input/output pin.
										I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
										O	**I2S_RX_MCLK —** I2S receive master clock.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I	**CMP0_IN[2] —** Comparator 0, input 2.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[18]	66	P7	L5	46	32	25	K4	[3]	I; PU	I/O	**P1[18] —** General purpose digital input/output pin.
										O	**USB_UP_LED1 —** It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
										O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
										I	**T1_CAP0 —** Capture input for Timer 1, channel 0.
										-	**R —** Function reserved.
										I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
P1[19]	68	U6	P5	47	33	26	J4	[3]	I; PU	I/O	**P1[19] —** General purpose digital input/output pin.
										O	**USB_TX_E1 —** Transmit Enable signal for USB port 1 (OTG transceiver).
										O	**USB_PPWR1 —** Port Power enable signal for USB port 1.
										I	**T1_CAP1 —** Capture input for Timer 1, channel 1.
										O	**MC_0A —** Motor control PWM channel 0, output A.
										I/O	**SSP1_SCK —** Serial clock for SSP1.
										O	**U2_OE —** RS-485/EIA-485 output enable signal for UART2.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[20]	70	U7	K6	49	34	27	J5	[3]	I; PU	I/O	**P1[20] —** General purpose digital input/output pin.
										O	**USB_TX_DP1 —** D+ transmit data for USB port 1 (OTG transceiver).
										O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
										I	**QEI_PHA —** Quadrature Encoder Interface PHA input.
										I	**MC_FB0 —** Motor control PWM channel 0 feedback input.
										I/O	**SSP0_SCK —** Serial clock for SSP0.
										O	**LCD_VD[6] —** LCD data.
										O	**LCD_VD[10] —** LCD data.
P1[21]	72	R8	N6	50	35	-	-	[3]	I; PU	I/O	**P1[21] —** General purpose digital input/output pin.
										O	**USB_TX_DM1 —** D− transmit data for USB port 1 (OTG transceiver).
										O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
										I/O	**SSP0_SSEL —** Slave Select for SSP0.
										I	**$\overline{\text{MC\_ABORT}}$ —** Motor control PWM, active low fast abort.
										-	**R —** Function reserved.
										O	**LCD_VD[7] —** LCD data.
										O	**LCD_VD[11] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[22]	74	U8	M6	51	36	28	K5	[3]	I; PU	I/O	**P1[22] —** General purpose digital input/output pin.
										I	**USB_RCV1 —** Differential receive data for USB port 1 (OTG transceiver).
										I	**USB_PWRD1 —** Power Status for USB port 1 (host power switch).
										O	**T1_MAT0 —** Match output for Timer 1, channel 0.
										O	**MC_0B —** Motor control PWM channel 0, output B.
										I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
										O	**LCD_VD[8] —** LCD data.
										O	**LCD_VD[12] —** LCD data.
P1[23]	76	P9	N7	53	37	29	H5	[3]	I; PU	I/O	**P1[23] —** General purpose digital input/output pin.
										I	**USB_RX_DP1 —** D+ receive data for USB port 1 (OTG transceiver).
										O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
										I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
										I	**MC_FB1 —** Motor control PWM channel 1 feedback input.
										I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
										O	**LCD_VD[9] —** LCD data.
										O	**LCD_VD[13] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[3]	144	E16	E13	100	70	55	C10	[3]	I; PU	I/O	**P2[3] —** General purpose digital input/output pin.
										O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
										I	**U1_DCD —** Data Carrier Detect input for UART1.
										O	**T2_MAT2 —** Match output for Timer 2, channel 2.
										-	**R —** Function reserved.
										O	**TRACEDATA[2] —** Trace data, bit 2.
										-	**R —** Function reserved.
										O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
P2[4]	142	D17	E14	99	69	54	C9	[3]	I; PU	I/O	**P2[4] —** General purpose digital input/output pin.
										O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
										I	**U1_DSR —** Data Set Ready input for UART1.
										O	**T2_MAT1 —** Match output for Timer 2, channel 1.
										-	**R —** Function reserved.
										O	**TRACEDATA[1] —** Trace data, bit 1.
										-	**R —** Function reserved.
										O	**LCD_ENAB_M —** STN AC bias drive or TFT data enable output.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P3[25]	56	U2	M3	39	27	-	-	[3]	I; PU	I/O	**P3[25] —** General purpose digital input/output pin.
										I/O	**EMC_D[25] —** External memory data line 25.
										O	**PWM1[2] —** Pulse Width Modulator 1, output 2.
										O	**T0_MAT0 —** Match output for Timer 0, channel 0.
P3[26]	55	T3	K7	38	26	-	-	[3]	I; PU	I/O	**P3[26] —** General purpose digital input/output pin.
										I/O	**EMC_D[26] —** External memory data line 26.
										O	**PWM1[3] —** Pulse Width Modulator 1, output 3.
										O	**T0_MAT1 —** Match output for Timer 0, channel 1.
										I	**STCLK —** System tick timer clock input. The maximum STCLK frequency is 1/4 of the ARM processor clock frequency CCLK.
P3[27]	203	A1	-	-	-	-	-	[3]	I; PU	I/O	**P3[27] —** General purpose digital input/output pin.
										I/O	**EMC_D[27] —** External memory data line 27.
										O	**PWM1[4] —** Pulse Width Modulator 1, output 4.
										I	**T1_CAP0 —** Capture input for Timer 1, channel 0.
P3[28]	5	D2	-	-	-	-	-	[3]	I; PU	I/O	**P3[28] —** General purpose digital input/output pin.
										I/O	**EMC_D[28] —** External memory data line 28.
										O	**PWM1[5] —** Pulse Width Modulator 1, output 5.
										I	**T1_CAP1 —** Capture input for Timer 1, channel 1.
P3[29]	11	F3	-	-	-	-	-	[3]	I; PU	I/O	**P3[29] —** General purpose digital input/output pin.
										I/O	**EMC_D[29] —** External memory data line 29.
										O	**PWM1[6] —** Pulse Width Modulator 1, output 6.
										O	**T1_MAT0 —** Match output for Timer 1, channel 0.

7.16.3 USB OTG controller

USB OTG is a supplement to the *USB 2.0 Specification* that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG Controller integrates the host controller, device controller, and a master-only I^2C interface to implement OTG dual-role device functionality. The dedicated I^2C interface controls an external OTG transceiver.

7.16.3.1 Features

- Fully compliant with On-The-Go supplement to the *USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

7.17 SD/MMC card interface

Remark: The SD/MMC card interface is available on parts LPC4088/78/76.

The Secure Digital and Multimedia Card Interface (MCI) allows access to external SD memory cards. The SD card interface conforms to the *SD Multimedia Card Specification Version 2.11*.

7.17.1 Features

- The MCI provides all functions specific to the SD/MMC memory card. These include the clock generation unit, power management control, and command and data transfer.
- Conforms to *Multimedia Card Specification v2.11*.
- Conforms to *Secure Digital Memory Card Physical Layer Specification, v0.96.*
- Can be used as a multimedia card bus or a secure digital memory card bus host. The SD/MMC can be connected to several multimedia cards or a single secure digital memory card.
- DMA supported through the GPDMA controller.

7.18 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC408x/7x use accelerated GPIO functions:

- GPIO registers are accessed through the AHB multilayer bus so that the fastest possible I/O timing can be achieved.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(REG)(3V3)}$). Having the on-chip voltage regulator powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly” while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power ($V_{DD(REG)(3V3)}$) is used to operate the RTC whenever $V_{DD(REG)(3V3)}$ is present. There is no power drain from the RTC battery when $V_{DD(REG)(3V3)}$ is available and $V_{DD(REG)(3V3)} > V_{BAT}$.

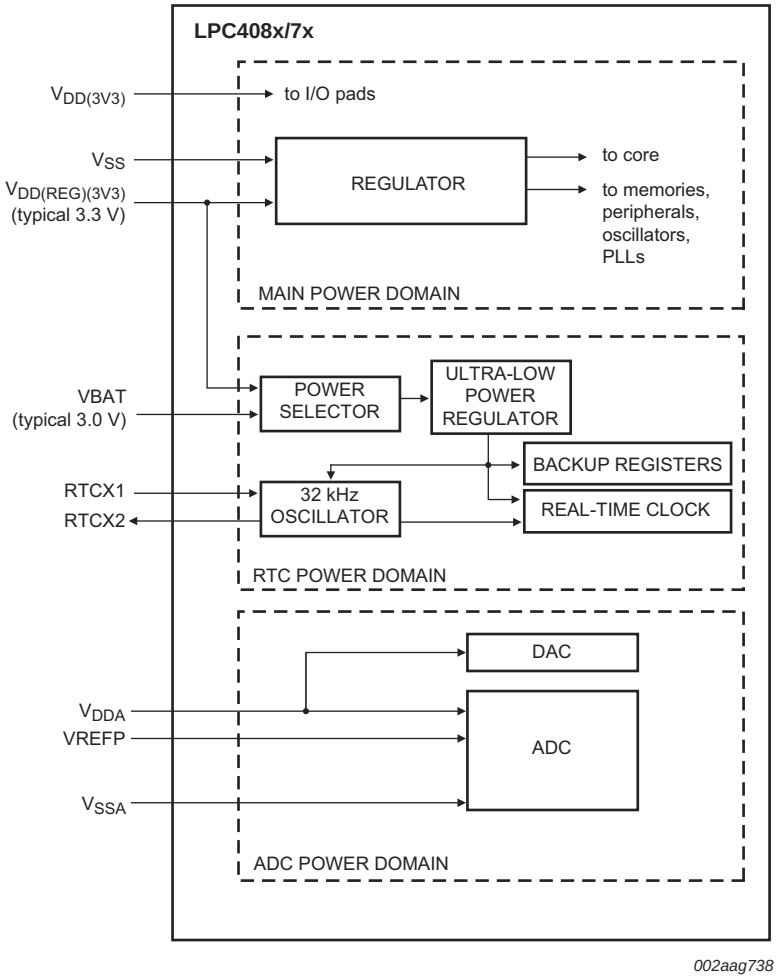
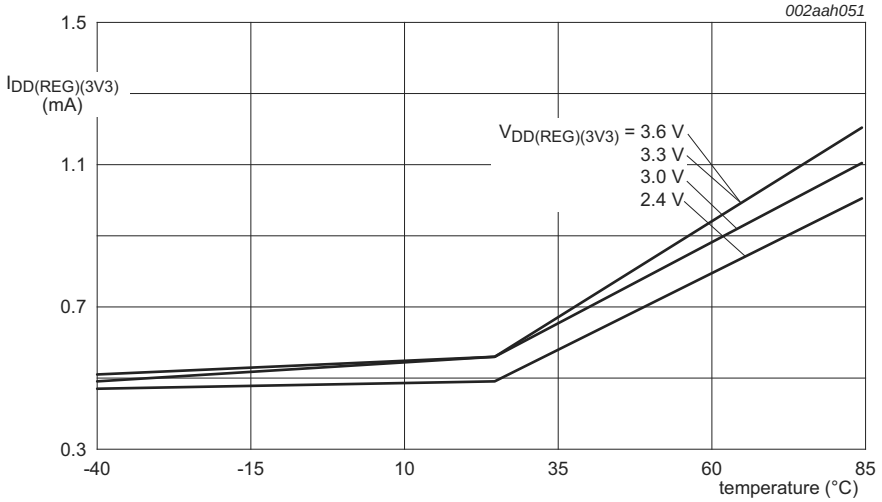


Fig 11. Power distribution

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

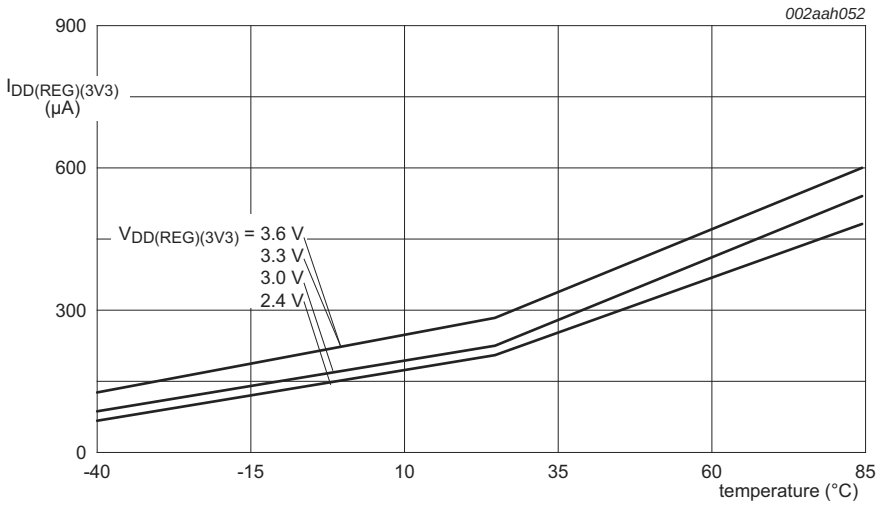
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; on-chip pull-down resistor disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[15][16] [17]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		$V_{DD(3V3)} - 0.45$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.45	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[18]	-	-	−50	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[18]	-	-	60	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	µA
		$V_{DD(3V3)} < V_I < 5$ V		0	0	0	µA
I^2C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05 \times V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[19]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[20]	-	-	±10	µA
V_{BUS}	bus supply voltage		[20]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	[20]	0.2	-	-	V

10.1 Power consumption



Conditions: BOD disabled.

Fig 12. Deep-sleep mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ versus temperature



Conditions: BOD disabled.

Fig 13. Power-down mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ versus temperature

Table 12. Power consumption for individual analog and digital blocks *…continued*
T_{amb} = 25 °C; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 3.3 V; PCLK = CCLK/4.

Peripheral	Conditions	Typical supply current in mA		
		12 MHz[1]	48 MHz[1]	120 MHz[2]
Motor control PWM		0.04	0.15	0.36
I2C0		0.01	0.03	0.08
I2C1		0.01	0.03	0.1
I2C2		0.01	0.03	0.08
I2C0 + I2C1 + I2C2		0.02	0.1	0.26
SSP0		0.03	0.1	0.26
SSP1		0.02	0.11	0.27
DAC		0.3	0.31	0.33
ADC (12 MHz clock)		1.51	1.61	1.7
Comparator		0.01	0.03	0.06
CAN1		0.11	0.44	1.08
CAN2		0.1	0.4	0.98
CAN1 + CAN2		0.15	0.59	1.44
DMA	PCLK = CCLK	1.1	4.27	10.27
QEI		0.02	0.11	0.28
GPIO		0.4	1.72	4.16
LCD		0.99	3.84	9.25
I2S		0.04	0.18	0.46
EMC		0.82	3.17	7.63
RTC		0.01	0.01	0.05
USB + PLL1		0.62	0.97	1.67
Ethernet	PCENET bit set to 1 in the PCONP register	0.54	2.08	5.03
SPIFI	SPIFICLKSEL register is set to 0x1	0.89	3.44	8.15

[1] Boost control bits in the PBOOST register set to 0x0 (see *LPC178x/7x User manual UM10470*).

[2] Boost control bits in the PBOOST register set to 0x3 (see *LPC178x/7x User manual UM10470*).

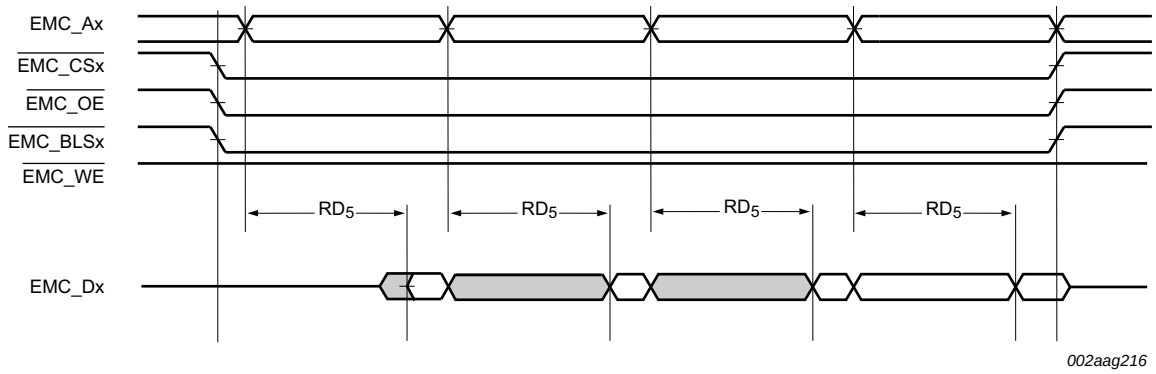


Fig 21. External static memory burst read cycle

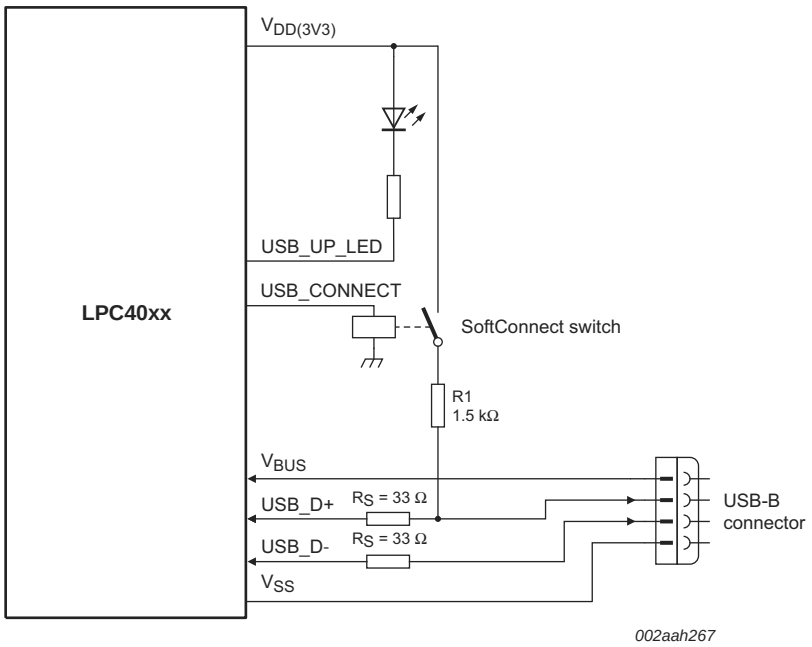


Fig 34. USB interface on a self-powered device

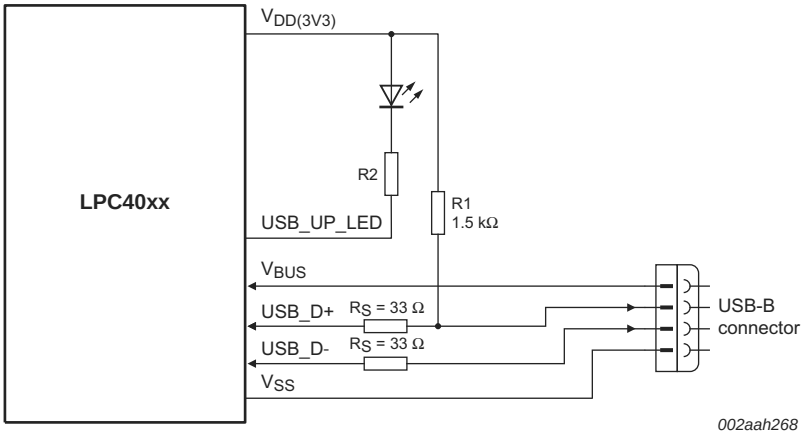


Fig 35. USB interface on a bus-powered device

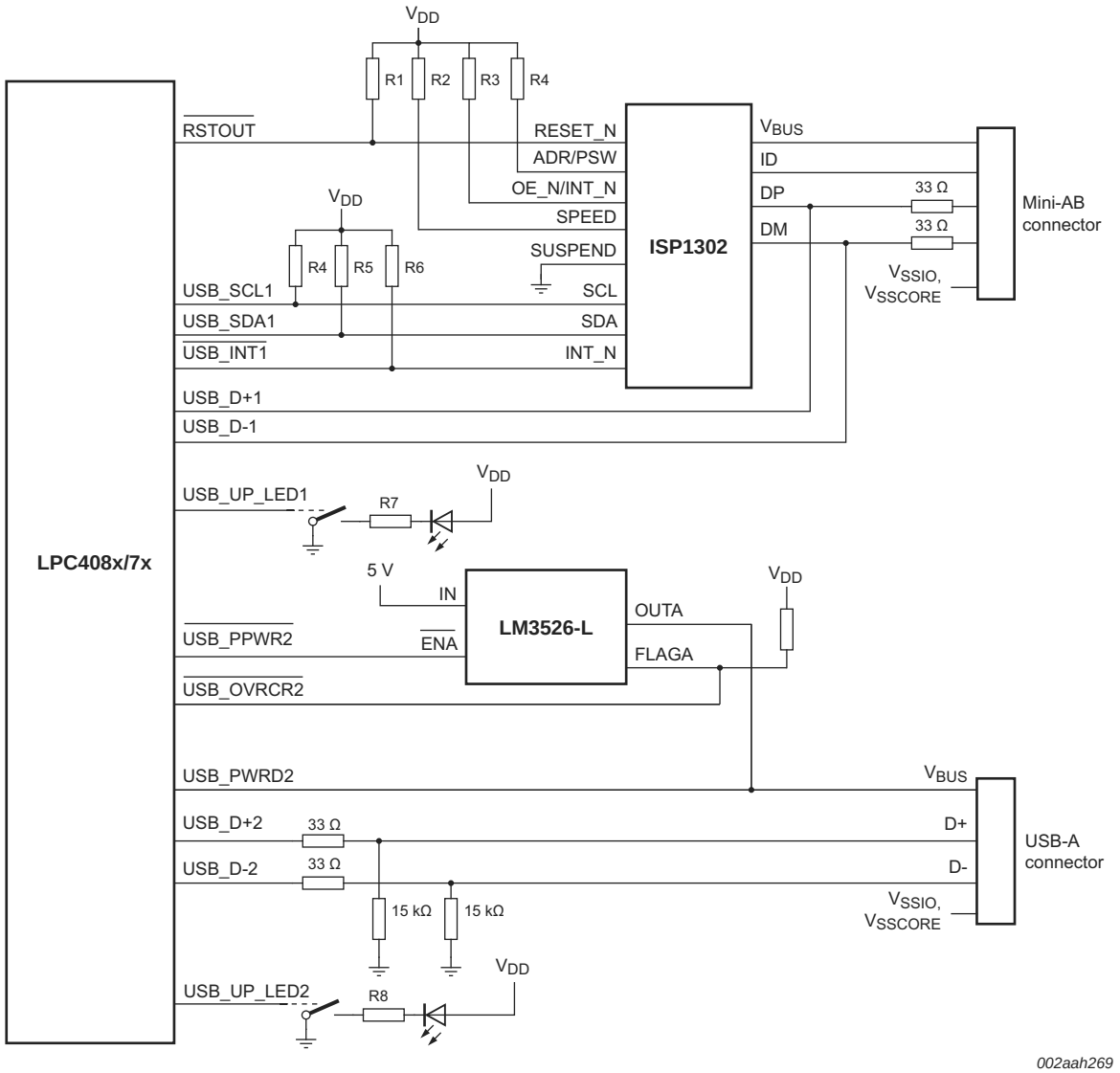


Fig 36. USB OTG port configuration: port 1 OTG dual-role device, port 2 host

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 40), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 41 and in Table 34 and Table 35. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 41 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

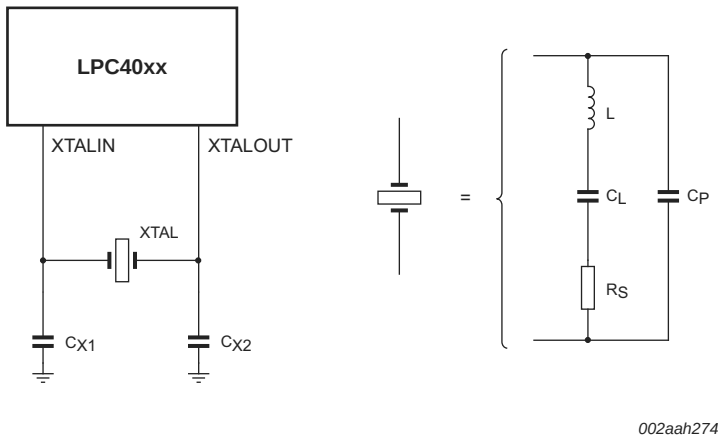


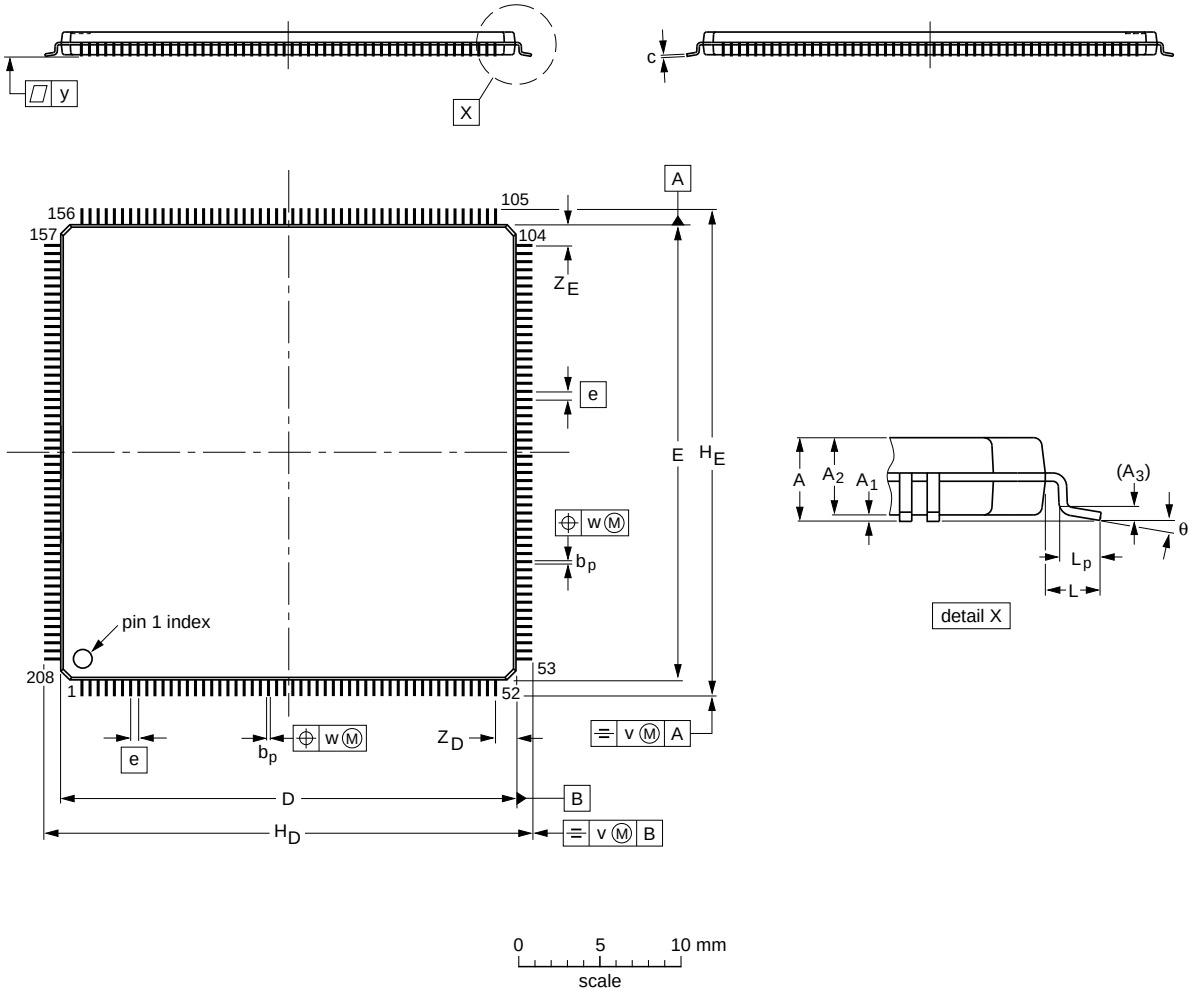
Fig 41. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 34. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

14. Package outline

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 45. Package outline SOT459-1 (LQFP208)