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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	-
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4074fbd80-551

- 10-bit Digital-to-Analog Converter (DAC) with dedicated conversion timer and DMA support.
- Two analog comparators.

- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.
  - Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, PORT0/2 pin interrupt, and NMI).
  - Brownout detect with separate threshold for interrupt and forced reset.
  - On-chip Power-On Reset (POR).
- Clock generation:
  - Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, USB clock, or the watchdog timer clock.
  - On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC oscillator (IRC) trimmed to 1 % accuracy that can optionally be used as a system clock.
  - An on-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator or the internal RC oscillator.
  - A second, dedicated PLL may be used for USB interface in order to allow added flexibility for the Main PLL settings.
- Versatile pin function selection feature allows many possibilities for using on-chip peripheral functions.
- Unique device serial number for identification purposes.
- Single 3.3 V power supply (2.4 V to 3.6 V). Temperature range of −40 °C to 85 °C.
- Available as LQFP208, TFBGA208, TFBGA180, LQFP144, TFBGA80, and LQFP80 package.

3. Applications

- Communications:
  - Point-of-sale terminals, web servers, multi-protocol bridges
- Industrial/Medical:
  - Automation controllers, application control, robotics control, HVAC, PLC, inverters, circuit breakers, medical scanning, security monitoring, motor drive, video intercom
- Consumer/Appliance:
  - Audio, MP3 decoders, alarm systems, displays, printers, scanners, small appliances, fitness equipment
- Automotive:
  - After-market, car alarms, GPS/fleet monitors

6. Pinning information

6.1 Pinning

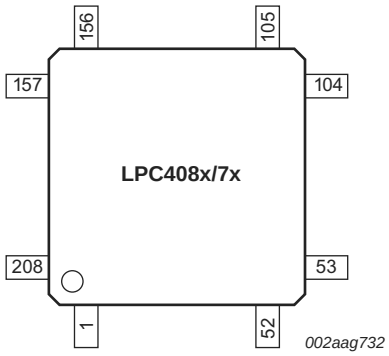


Fig 2. Pin configuration (LQFP208)

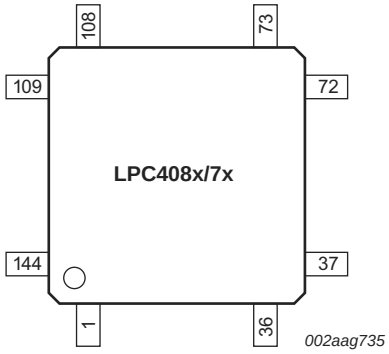


Fig 3. Pin configuration (LQFP144)

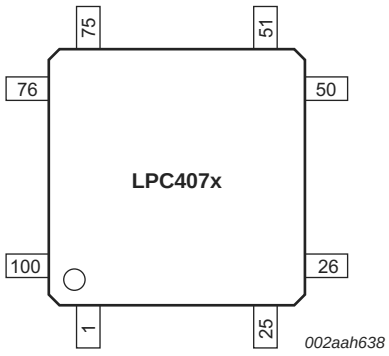


Fig 4. Pin configuration (LQFP100)

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[6]	164	D13	D11	113	79	64	A7	[3]	I; PU	I/O	**P0[6] —** General purpose digital input/output pin.
										I/O	**I2S_RX_SDA —** I^2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
										I/O	**SSP1_SSEL —** Slave Select for SSP1.
										O	**T2_MAT0 —** Match output for Timer 2, channel 0.
										O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	**CMP_ROSC —** Comparator relaxation oscillator for 555 timer applications.
										-	**R —** Function reserved.
										O	**LCD_VD[8] —** LCD data.
P0[7]	162	C13	B12	112	78	63	A8	[4]	I; IA	I/O	**P0[7] —** General purpose digital input/output pin.
										I/O	**I2S_TX_SCK —** I^2S transmit clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
										I/O	**SSP1_SCK —** Serial Clock for SSP1.
										O	**T2_MAT1 —** Match output for Timer 2, channel 1.
										I	**RTC_EV0 —** Event input 0 to Event Monitor/Recorder.
										I	**CMP_VREF —** Comparator reference voltage.
										-	**R —** Function reserved.
										O	**LCD_VD[9] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[7]	136	G16	G11	95	66	51	D9	[3]	I; PU	I/O	**P2[7] —** General purpose digital input/output pin.
										I	**CAN_RD2 —** CAN2 receiver input.
										O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**$\overline{\text{SPIFI\_CS}}$ —** Chip select output for SPIFI.
										O	**LCD_VD[1] —** LCD data.
										O	**LCD_VD[5] —** LCD data.
P2[8]	134	H15	G14	93	65	50	E9	[3]	I; PU	I/O	**P2[8] —** General purpose digital input/output pin.
										O	**CAN_TD2 —** CAN2 transmitter output.
										O	**U2_TXD —** Transmitter output for UART2.
										I	**U1_CTS —** Clear to Send input for UART1.
										O	**ENET_MDC —** Ethernet MIIM clock.
										-	**R —** Function reserved.
										O	**LCD_VD[2] —** LCD data.
										O	**LCD_VD[6] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[9]	132	H16	H11	92	64	49	E10	[3]	I; PU	I/O	**P2[9] —** General purpose digital input/output pin.
										O	**USB_CONNECT1 —** USB1 SoftConnect control. Signal used to switch an external 1.5 kΩ resistor under the software control. Used with the SoftConnect USB feature.
										I	**U2_RXD —** Receiver input for UART2.
										I	**U4_RXD —** Receiver input for USART4.
										I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
										-	**R —** Function reserved.
										I	**LCD_VD[3] —** LCD data.
										I	**LCD_VD[7] —** LCD data.
P2[10]	110	N15	M13	76	53	41	H9	[10]	I; PU	I/O	**P2[10] —** General purpose digital input/output pin. This pin includes a 10 ns input glitch filter. A LOW on this pin while RESET is LOW forces the on-chip boot loader to take over control of the part after a reset and go into ISP mode.
										I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.
										I	**NMI —** Non-maskable interrupt input.
P2[11]	108	T17	M12	75	52	-	-	[10]	I; PU	I/O	**P2[11] —** General purpose digital input/output pin. This pin includes a 10 ns input glitch filter.
										I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.
										I/O	**SD_DAT[1] —** Data line 1 for SD card interface.
										I/O	**I2S_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_CLKIN —** LCD clock.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[15]	99	P13	-	-	-	-	-	[3]	I; PU	I/O	**P2[15] —** General purpose digital input/output pin.
										O	**EMC_CS3 —** LOW active Chip Select 3 signal.
										I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
										I	**T2_CAP1 —** Capture input for Timer 2, channel 1.
P2[16]	87	R11	P9	-	-	-	-	[3]	I; PU	I/O	**P2[16] —** General purpose digital input/output pin.
										O	**EMC_CAS —** LOW active SDRAM Column Address Strobe.
P2[17]	95	R13	P11	-	-	-	-	[3]	I; PU	I/O	**P2[17] —** General purpose digital input/output pin.
										O	**EMC_RAS —** LOW active SDRAM Row Address Strobe.
P2[18]	59	U3	P3	-	-	-	-	[6]	I; PU	I/O	**P2[18] —** General purpose digital input/output pin.
										O	**EMC_CLK[0] —** SDRAM clock 0.
P2[19]	67	R7	N5	-	-	-	-	[6]	I; PU	I/O	**P2[19] —** General purpose digital input/output pin.
										O	**EMC_CLK[1] —** SDRAM clock 1.
P2[20]	73	T8	P6	-	-	-	-	[3]	I; PU	I/O	**P2[20] —** General purpose digital input/output pin.
										O	**EMC_DYCS0 —** SDRAM chip select 0.
P2[21]	81	U11	N8	-	-	-	-	[3]	I; PU	I/O	**P2[21] —** General purpose digital input/output pin.
										O	**EMC_DYCS1 —** SDRAM chip select 1.
P2[22]	85	U12	-	-	-	-	-	[3]	I; PU	I/O	**P2[22] —** General purpose digital input/output pin.
										O	**EMC_DYCS2 —** SDRAM chip select 2.
										I/O	**SSP0_SCK —** Serial clock for SSP0.
										I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P2[23]	64	U5	-	-	-	-	-	[3]	I; PU	I/O	**P2[23] —** General purpose digital input/output pin.
										O	**EMC_DYCS3 —** SDRAM chip select 3.
										I/O	**SSP0_SSEL —** Slave Select for SSP0.
										I	**T3_CAP1 —** Capture input for Timer 3, channel 1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P3[9]	199	C5	A4	-	-	-	-	[3]	I; PU	I/O	**P3[9] —** General purpose digital input/output pin.
										I/O	**EMC_D[9] —** External memory data line 9.
P3[10]	205	B2	B3	-	-	-	-	[3]	I; PU	I/O	**P3[10] —** General purpose digital input/output pin.
										I/O	**EMC_D[10] —** External memory data line 10.
P3[11]	208	D5	B2	-	-	-	-	[3]	I; PU	I/O	**P3[11] —** General purpose digital input/output pin.
										I/O	**EMC_D[11] —** External memory data line 11.
P3[12]	1	D4	A1	-	-	-	-	[3]	I; PU	I/O	**P3[12] —** General purpose digital input/output pin.
										I/O	**EMC_D[12] —** External memory data line 12.
P3[13]	7	C1	C1	-	-	-	-	[3]	I; PU	I/O	**P3[13] —** General purpose digital input/output pin.
										I/O	**EMC_D[13] —** External memory data line 13.
P3[14]	21	H2	F1	-	-	-	-	[3]	I; PU	I/O	**P3[14] —** General purpose digital input/output pin.
										I/O	**EMC_D[14] —** External memory data line 14.
P3[15]	28	M1	G4	-	-	-	-	[3]	I; PU	I/O	**P3[15] —** General purpose digital input/output pin.
										I/O	**EMC_D[15] —** External memory data line 15.
P3[16]	137	F17	-	-	-	-	-	[3]	I; PU	I/O	**P3[16] —** General purpose digital input/output pin.
										I/O	**EMC_D[16] —** External memory data line 16.
										O	**PWM0[1] —** Pulse Width Modulator 0, output 1.
										O	**U1_TXD —** Transmitter output for UART1.
P3[17]	143	F15	-	-	-	-	-	[3]	I; PU	I/O	**P3[17] —** General purpose digital input/output pin.
										I/O	**EMC_D[17] —** External memory data line 17.
										O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
										I	**U1_RXD —** Receiver input for UART1.
P3[18]	151	C15	-	-	-	-	-	[3]	I; PU	I/O	**P3[18] —** General purpose digital input/output pin.
										I/O	**EMC_D[18] —** External memory data line 18.
										O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
										I	**U1_CTS —** Clear to Send input for UART1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P4[7]	121	L16	K12	84	-	-	-	[3]	I; PU	I/O	**P4[7] —** General purpose digital input/output pin.
										I/O	**EMC_A[7] —** External memory address line 7.
P4[8]	127	J17	J11	88	-	-	-	[3]	I; PU	I/O	**P4[8] —** General purpose digital input/output pin.
										I/O	**EMC_A[8] —** External memory address line 8.
P4[9]	131	H17	H12	91	-	-	-	[3]	I; PU	I/O	**P4[9] —** General purpose digital input/output pin.
										I/O	**EMC_A[9] —** External memory address line 9.
P4[10]	135	G17	G12	94	-	-	-	[3]	I; PU	I/O	**P4[10] —** General purpose digital input/output pin.
										I/O	**EMC_A[10] —** External memory address line 10.
P4[11]	145	F14	F11	101	-	-	-	[3]	I; PU	I/O	**P4[11] —** General purpose digital input/output pin.
										I/O	**EMC_A[11] —** External memory address line 11.
P4[12]	149	C16	F10	104	-	-	-	[3]	I; PU	I/O	**P4[12] —** General purpose digital input/output pin.
										I/O	**EMC_A[12] —** External memory address line 12.
P4[13]	155	B16	B14	108	-	-	-	[3]	I; PU	I/O	**P4[13] —** General purpose digital input/output pin.
										I/O	**EMC_A[13] —** External memory address line 13.
P4[14]	159	B15	E8	110	-	-	-	[3]	I; PU	I/O	**P4[14] —** General purpose digital input/output pin.
										I/O	**EMC_A[14] —** External memory address line 14.
P4[15]	173	A11	C10	120	-	-	-	[3]	I; PU	I/O	**P4[15] —** General purpose digital input/output pin.
										I/O	**EMC_A[15] —** External memory address line 15.
P4[16]	101	U17	N12	-	-	-	-	[3]	I; PU	I/O	**P4[16] —** General purpose digital input/output pin.
										I/O	**EMC_A[16] —** External memory address line 16.
P4[17]	104	P14	N13	-	-	-	-	[3]	I; PU	I/O	**P4[17] —** General purpose digital input/output pin.
										I/O	**EMC_A[17] —** External memory address line 17.
P4[18]	105	P15	P14	-	-	-	-	[3]	I; PU	I/O	**P4[18] —** General purpose digital input/output pin.
										I/O	**EMC_A[18] —** External memory address line 18.
P4[19]	111	P16	M14	-	-	-	-	[3]	I; PU	I/O	**P4[19] —** General purpose digital input/output pin.
										I/O	**EMC_A[19] —** External memory address line 19.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P4[20]	109	R17	-	-	-	-	-	[3]	I; PU	I/O	**P4[20] —** General purpose digital input/output pin.
										I/O	**EMC_A[20] —** External memory address line 20.
										I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
										I/O	**SSP1_SCK —** Serial Clock for SSP1.
P4[21]	115	M15	-	-	-	-	-	[3]	I; PU	I/O	**P4[21] —** General purpose digital input/output pin.
										I/O	**EMC_A[21] —** External memory address line 21.
										I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
										I/O	**SSP1_SSEL —** Slave Select for SSP1.
P4[22]	123	K14	-	-	-	-	-	[3]	I; PU	I/O	**P4[22] —** General purpose digital input/output pin.
										I/O	**EMC_A[22] —** External memory address line 22.
										O	**U2_TXD —** Transmitter output for UART2.
										I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
P4[23]	129	J15	-	-	-	-	-	[3]	I; PU	I/O	**P4[23] —** General purpose digital input/output pin.
										I/O	**EMC_A[23] —** External memory address line 23.
										I	**U2_RXD —** Receiver input for UART2.
										I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
P4[24]	183	B8	C8	127	-	-	-	[3]	I; PU	I/O	**P4[24] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_OE}}$ —** LOW active Output Enable signal.
P4[25]	179	B9	D9	124	-	-	-	[3]	I; PU	I/O	**P4[25] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_WE}}$ —** LOW active Write Enable signal.
P4[26]	119	L15	K13	-	-	-	-	[3]	I; PU	I/O	**P4[26] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_BLS0}}$ —** LOW active Byte Lane select signal 0.
P4[27]	139	G15	F14	-	-	-	-	[3]	I; PU	I/O	**P4[27] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_BLS1}}$ —** LOW active Byte Lane select signal 1.

7.11.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.12 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral and can be accessed through the AHB master. The GPDMA controller allows data transfers between the various on-chip SRAM areas and supports the SD/MMC card interface, all SSPs, the I^2S, all UARTs, the A/D Converter, and the D/A Converter peripherals. DMA can also be triggered by selected timer match conditions. Memory-to-memory transfers and transfers to or from GPIO are supported.

7.12.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.

7.36.1.3 RTC oscillator

The RTC oscillator provides a 1 Hz clock to the RTC and a 32 kHz clock output that can be output on the CLKOUT pin in order to allow trimming the RTC oscillator without interference from a probe.

7.36.1.4 Watchdog oscillator

The Watchdog Timer has a dedicated oscillator that provides a 500 kHz clock to the Watchdog Timer that is always running if the Watchdog Timer is enabled. The Watchdog oscillator clock can be output on the CLKOUT pin in order to allow observe its frequency.

In order to allow Watchdog Timer operation with minimum power consumption, which can be important in reduced power modes, the Watchdog oscillator frequency is not tightly controlled. The Watchdog oscillator frequency will vary over temperature and power supply within a particular part, and may vary by processing across different parts. This variation should be taken into account when determining Watchdog reload values.

Within a particular part, temperature and power supply variations can produce up to a ±17 % frequency variation. Frequency variation between devices under the same operating conditions can be up to ±30 %.

7.36.2 Main PLL (PLL0) and Alternate PLL (PLL1)

PLL0 (also called the Main PLL) and PLL1 (also called the Alternate PLL) are functionally identical but have somewhat different input possibilities and output connections. These possibilities are shown in Figure 10. The Main PLL can receive its input from either the IRC or the main oscillator and can potentially be used to provide the clocks to nearly everything on the device. The Alternate PLL receives its input only from the main oscillator and is intended to be used as an alternate source of clocking to the USB. The USB has timing needs that may not always be filled by the Main PLL.

Both PLLs are disabled and powered off on reset. If the Alternate PLL is left disabled, the USB clock can be supplied by PLL0 if everything is set up to provide 48 MHz to the USB clock through that route. The source for each clock must be selected via the CLKSEL registers and can be further reduced by clock dividers as needed.

PLL0 accepts an input clock frequency from either the IRC or the main oscillator. If only the Main PLL is used, then its output frequency must be an integer multiple of all other clocks needed in the system. PLL1 takes its input only from the main oscillator, requiring an external crystal in the range of 10 to 25 MHz. In each PLL, the Current Controlled Oscillator (CCO) operates in the range of 156 MHz to 320 MHz, so there are additional dividers to bring the output down to the desired frequencies. The minimum output divider value is 2, insuring that the output of the PLLs have a 50 % duty cycle.

If the USB is used, the possibilities for the CPU clock and other clocks will be limited by the requirements that the frequency be precise and very low jitter, and that the PLL0 output must be a multiple of 48 MHz. Even multiples of 48 MHz that are within the operating range of the PLL are 192 MHz and 288 MHz. Also, only the main oscillator in conjunction with the PLL can meet the precision and jitter specifications for USB. It is due to these limitations that the Alternate PLL is provided.

The alternate PLL accepts an input clock frequency from the main oscillator in the range of 10 MHz to 25 MHz only. When used as the USB clock, the input frequency is multiplied up to a multiple of 48 MHz (192 MHz or 288 MHz as described above).

10. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	2.4	3.3	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			2.4	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[3]	2.7	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[4]	2.1	3.0	3.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[3]	2.7	3.3	V_{DDA}	V
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	active mode; code `while(1){}` executed from flash; all peripherals disabled PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]	-	7.5	-	mA
		CCLK = 120 MHz; PLL enabled	[5][7]	-	56	-	mA
		active mode; code `while(1){}` executed from flash; all peripherals enabled; PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]		14	-	-
		CCLK = 120 MHz; PLL enabled	[5][7]		120	-	mA
		Sleep mode	[5][8]	-	5.5	-	mA
		Deep-sleep mode	[5][9]	-	550	1200	µA
		Power-down mode	[5][9]	-	280	600	µA
I_{BAT}	battery supply current	RTC running; part powered down; $V_{DD(REG)(3V3)}$ =0 V; $V_{i(VBAT)}$ = 3.0 V; $V_{DD(3V3)}$ = 0 V.	[10]	-	1	9	µA
		part powered; $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{i(VBAT)}$ = 3.0 V	[11]		<10		nA

Table 15. Dynamic characteristics: Static external memory interface *…continued*

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
t_{am}	memory access time	RD_5	[4][3]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 9.6	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 13.2	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 20.2	ns
$t_{h(D)}$	data input hold time	RD_6	[5][3]	−5.0	−7.2	−	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1		2.7	3.4	4.9	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[3]	2.4	3.1	4.2	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		[3]	0.77	1.2	1.86	ns
t_{deact}	deactivation time	RD_7	[3]	-	−4.3	−6.1	ns
Write cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		3.3	4.3	6.1	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		3.4	4.8	6.6	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[3]	2.6 + $T_{cy(clk)}$ × (1 + WAITWEN)	3.3 + $T_{cy(clk)}$ × (1 + WAITWEN)	4.6 + $T_{cy(clk)}$ × (1 + WAITWEN)	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[3]	2.7	3.5	4.9	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[3]	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 2.3	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 2.8	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 3.8	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[3]	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 2.8	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 3.5	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 5.0	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[3]	3.1 + $T_{cy(clk)}$	4.3 + $T_{cy(clk)}$	5.8 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[6][3]	$T_{cy(clk)}$ − 2.6	$T_{cy(clk)}$ − 3.4	$T_{cy(clk)}$ − 4.6	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1		3.4	4.8	6.6	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	PB = 1	[3]	3.0 + $T_{cy(clk)}$	3.8 + $T_{cy(clk)}$	5.3 + $T_{cy(clk)}$	ns
t_{deact}	deactivation time	WR_8; PB = 0; PB = 1	[3]	−3.3	−4.3	−6.1	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	WR_9; PB = 0	[3]	2.7 + $T_{cy(clk)}$ × (1 + WAITWEN)	3.5 + $T_{cy(clk)}$ × (1 + WAITWEN)	4.9 + $T_{cy(clk)}$ × (1 + WAITWEN)	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	WR_{10}; PB = 0	[3]	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 2.8	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ −3.5	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 5.0	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	WR_{11}; PB = 0	[6][3]	3.3 + $T_{cy(clk)}$	4.4 + $T_{cy(clk)}$	6.1 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	WR_{12}; PB = 0	[3]	3.4 + $T_{cy(clk)}$	4.8 + $T_{cy(clk)}$	6.6 + $T_{cy(clk)}$	ns

[1] Parameters are shown as RD_n or WD_n in Figure 19 as indicated in the Conditions column.

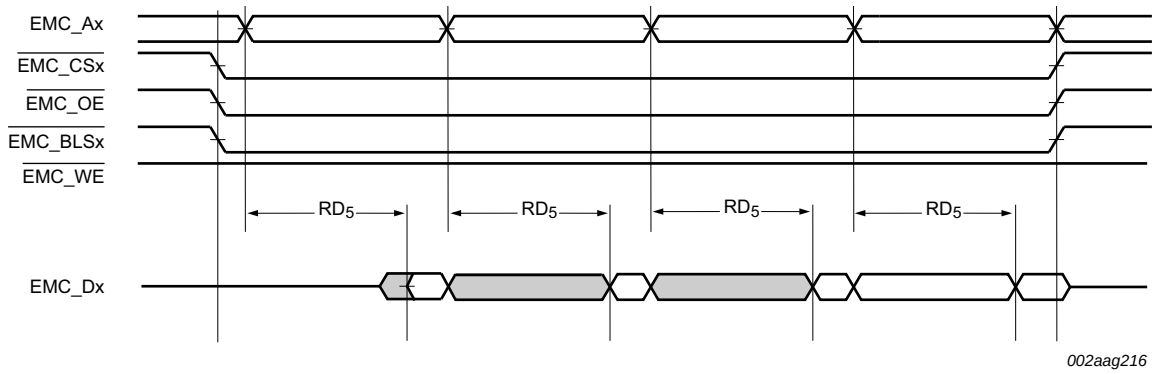


Fig 21. External static memory burst read cycle

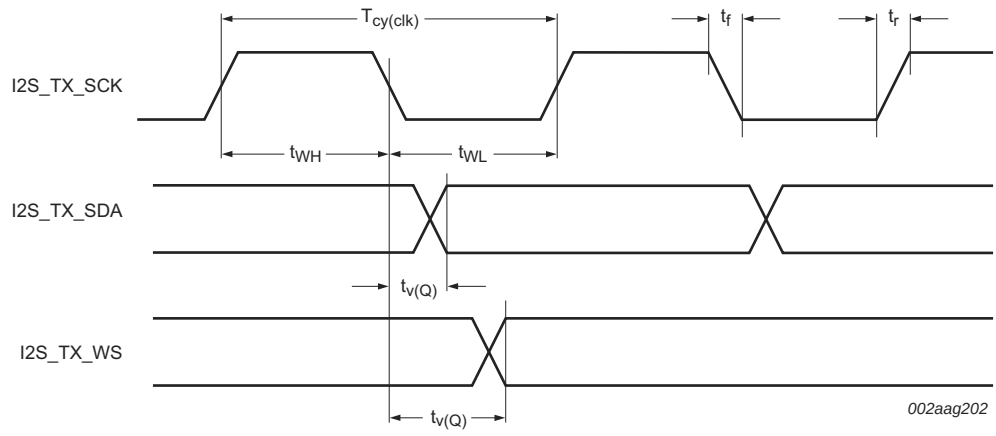


Fig 27. I²S-bus timing (transmit)

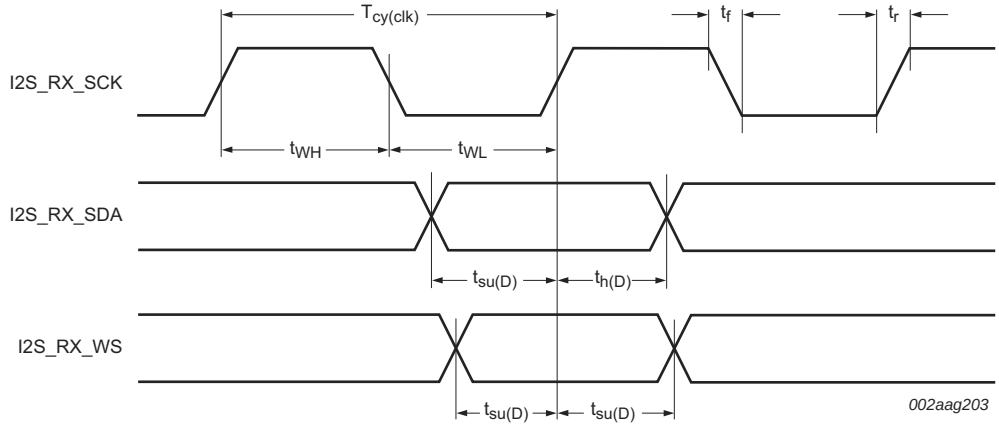


Fig 28. I²S-bus timing (receive)

11.9 LCD

Remark: The LCD controller is available on parts LPC4088.

Table 25. Dynamic characteristics: LCD

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	50	MHz
$t_{d(QV)}$	data output valid delay time		-	9	ns
$t_{h(Q)}$	data output hold time		−0.5	-	ns

Table 31. Comparator characteristics *…continued*
V_{DDA}= 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DV_O	output voltage variation			0	-	V_{DDA}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V		-	–4 to +4.2	-	mV
		V_{IC} = 1.5 V		-	±2	-	mV
		V_{IC} = 2.8 V		-	±2.5		mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process		-	4	-	µs
t_{PD}	propagation delay	HIGH to LOW; V_{DDA} = 3.3 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	122	130	142	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	173	189	233	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	101	108	119	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	114	127	162	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	123	134	143	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	79	91	120	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DDA} = 3.3 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	221	232	254	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	59	63	68	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	183	229	249	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	147	174	213	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	171	192	216	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	235	305	450	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V	[2]	-	5, 10, 20	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V	[2]	-	5, 10, 20	-	mV
R_{lad}	ladder resistance	-		-	1.034	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = -40 °C to +85 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable.

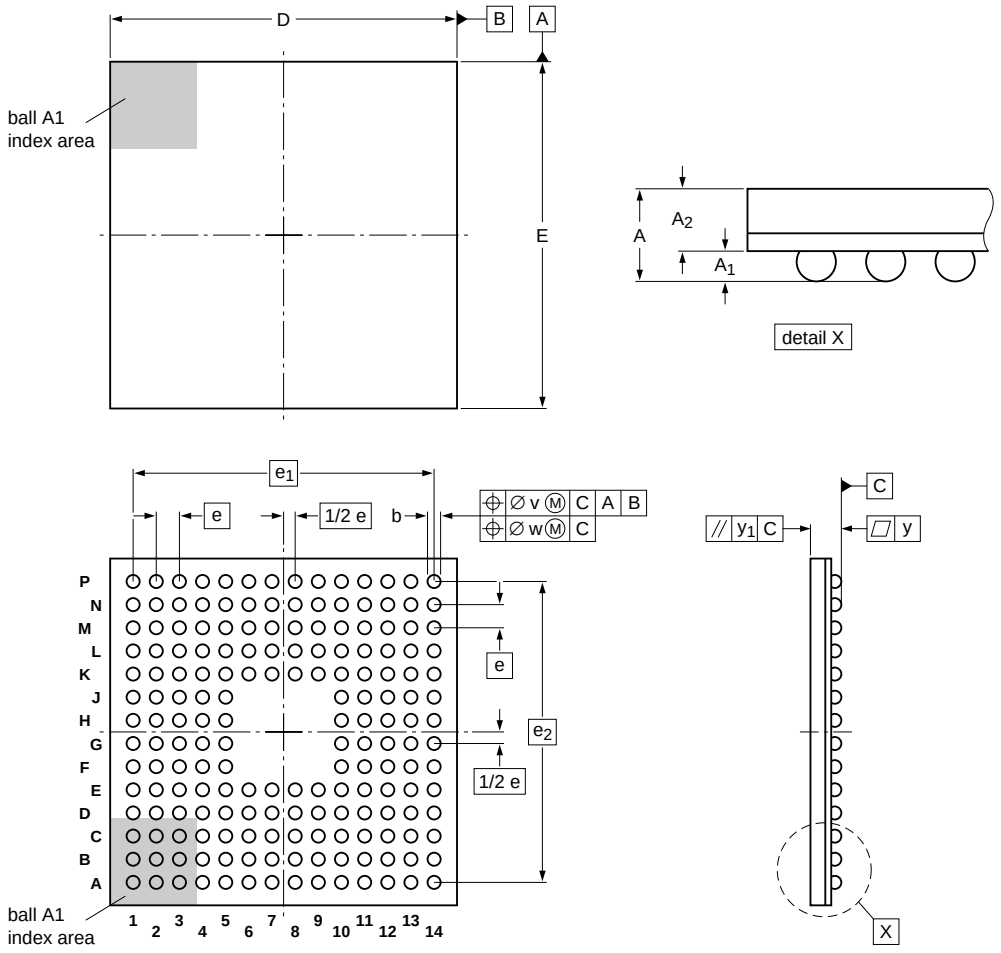
Table 32. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	15	µs

[1] Maximum values are derived from worst case simulation (V_{DDA} = 2.6 V; T_{amb} = 85 °C; slow process models).

[2] Settling time applies to switching between comparator and ADC channels.

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



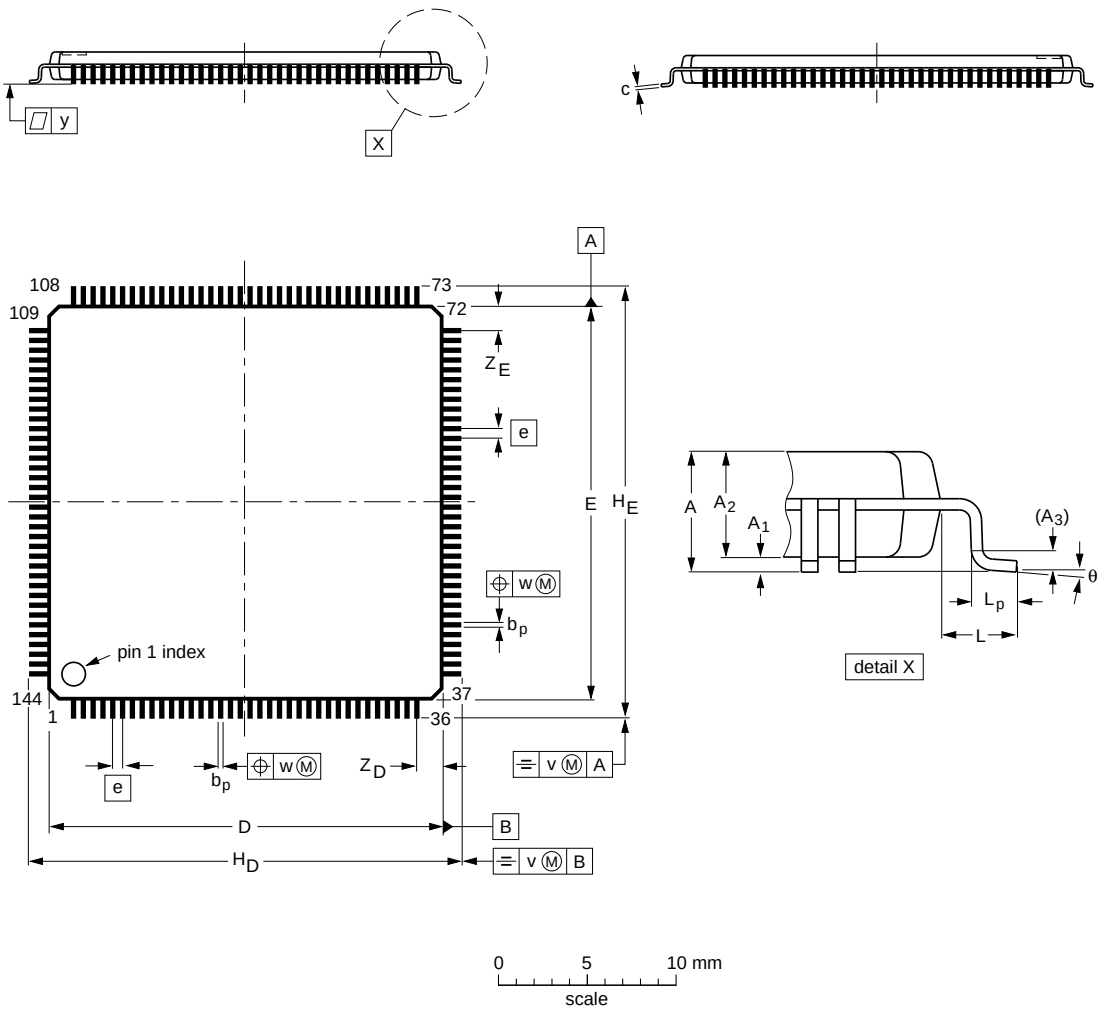
DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 47. Package outline SOT570-3 (TFBGA180)

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

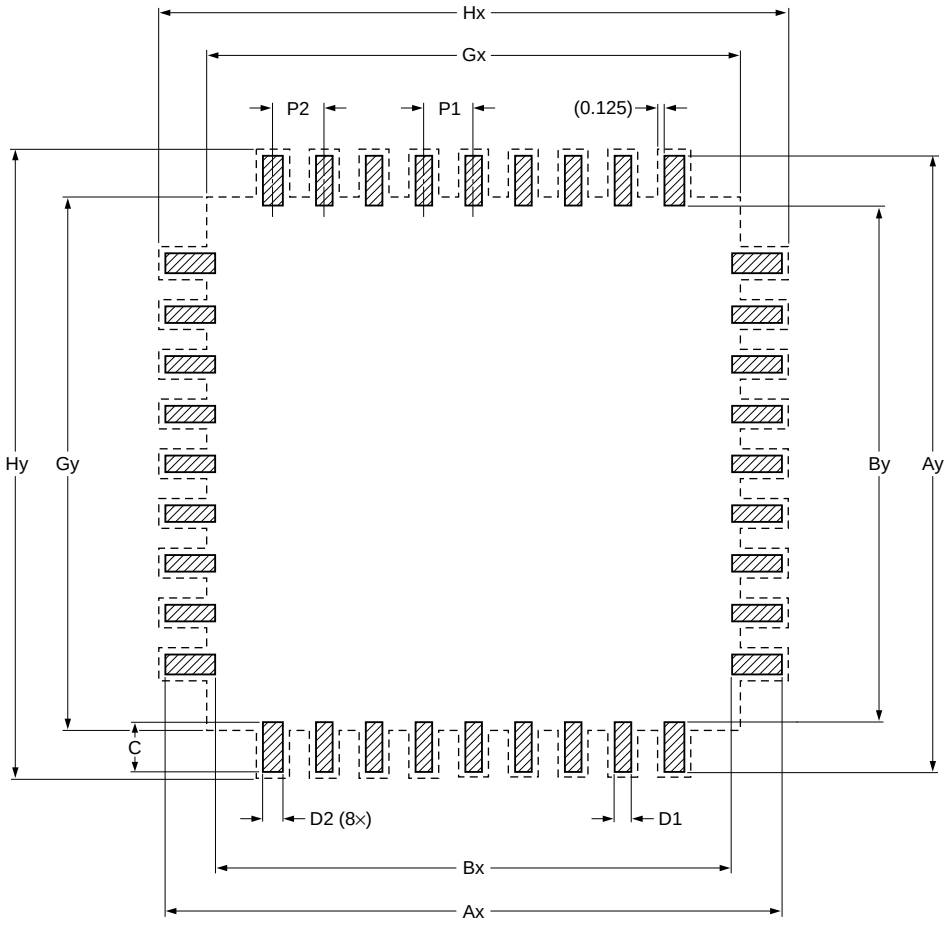
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 48. Package outline SOT486-1 (LQFP144)

15. Soldering

Footprint information for reflow soldering of LQFP208 package **SOT459-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	31.300	31.300	28.300	28.300	1.500	0.280	0.400	28.500	28.500	31.550	31.550

sot459-1_fr

Fig 52. Reflow soldering of the LQFP208 package

16. Abbreviations

Table 36. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
ETM	Embedded Trace Macrocell
GPIO	General Purpose Input/Output
GPS	Global Positioning System
HVAC	Heating, Venting, and Air Conditioning
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
MAC	Media Access Control
MIIM	Media Independent Interface Management
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLC	Programmable Logic Controller
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCM	Tightly Coupled Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus