Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	-
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4076fbd144e

Table 3. Pin description

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[0] to P0[31]										I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block.
P0[0]	94	U15	M10	66	46	37	J9	[3]	I; PU	I/O	**P0[0] —** General purpose digital input/output pin.
										I	**CAN_RD1 —** CAN1 receiver input.
										O	**U3_TXD —** Transmitter output for UART3.
										I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
										O	**U0_TXD —** Transmitter output for UART0.
P0[1]	96	T14	N11	67	47	38	J10	[3]	I; PU	I/O	**P0[1] —** General purpose digital input/output pin.
										O	**CAN_TD1 —** CAN1 transmitter output.
										I	**U3_RXD —** Receiver input for UART3.
										I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
										I	**U0_RXD —** Receiver input for UART0.
P0[2]	202	C4	D5	141	98	79	A2	[3]	I; PU	I/O	**P0[2] —** General purpose digital input/output pin.
										O	**U0_TXD —** Transmitter output for UART0.
										O	**U3_TXD —** Transmitter output for UART3.
P0[3]	204	D6	A3	142	99	80	A1	[3]	I; PU	I/O	**P0[3] —** General purpose digital input/output pin.
										I	**U0_RXD —** Receiver input for UART0.
										I	**U3_RXD —** Receiver input for UART3.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[20]	120	M17	K14	83	58	-	-	[3]	I; PU	I/O	**P0[20] —** General purpose digital input/output pin.
										O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	**SD_CMD —** Command line for SD card interface.
										I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_VD[14] —** LCD data.
P0[21]	118	M16	K11	82	57	-	-	[3]	I; PU	I/O	**P0[21] —** General purpose digital input/output pin.
										I	**U1_RI —** Ring Indicator input for UART1.
										O	**SD_PWR —** Power Supply Enable for external SD card power supply.
										O	**U4_OE —** RS-485/EIA-485 output enable signal for UART4.
										I	**CAN_RD1 —** CAN1 receiver input.
										I/O	**U4_SCLK —** USART 4 clock input or output in synchronous mode.
P0[22]	116	N17	L14	80	56	44	H10	[6]	I; PU	I/O	**P0[22] —** General purpose digital input/output pin.
										O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	**SD_DAT[0] —** Data line 0 for SD card interface.
										O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
										O	**CAN_TD1 —** CAN1 transmitter output.
										O	**SPIFI_CLK —** Clock output for SPIFI.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[23]	18	H1	F5	13	9	-	-	[5]	I; PU	I/O	**P0[23] —** General purpose digital input/output pin.
										I	**ADC0_IN[0] —** A/D converter 0, input 0. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
										I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P0[24]	16	G2	E1	11	8	-	-	[5]	I; PU	I/O	**P0[24] —** General purpose digital input/output pin.
										I	**ADC0_IN[1] —** A/D converter 0, input 1. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
										I	**T3_CAP1 —** Capture input for Timer 3, channel 1.
P0[25]	14	F1	E4	10	7	7	D1	[5]	I; PU	I/O	**P0[25] —** General purpose digital input/output pin.
										I	**ADC0_IN[2] —** A/D converter 0, input 2. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
										O	**U3_TXD —** Transmitter output for UART3.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[26]	12	E1	D1	8	6	6	D2	[7]	I; PU	I/O	**P0[26] —** General purpose digital input/output pin.
										I	**ADC0_IN[3] —** A/D converter 0, input 3. When configured as an ADC input, the digital function of the pin must be disabled.
										O	**DAC_OUT —** D/A converter output. When configured as the DAC output, the digital function of the pin must be disabled.
										I	**U3_RXD —** Receiver input for UART3.
P0[27]	50	T1	L3	35	25	-	-	[8]	I	I/O	**P0[27] —** General purpose digital input/output pin.
										I/O	**I2C0_SDA —** I^2C0 data input/output. (This pin uses a specialized I2C pad).
										I/O	**USB_SDA1 —** I2C serial data for communication with an external USB transceiver.
P0[28]	48	R3	M1	34	24	-	-	[8]	I	I/O	**P0[28] —** General purpose digital input/output pin.
										I/O	**I2C0_SCL —** I^2C0 clock input/output (this pin uses a specialized I2C pad.
										I/O	**USB_SCL1 —** I2C serial clock for communication with an external USB transceiver.
P0[29]	61	U4	K5	42	29	22	J3	[9]	I	I/O	**P0[29] —** General purpose digital input/output pin.
										I/O	**USB_D+1 —** USB port 1 bidirectional D+ line.
										I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.
P0[30]	62	R6	N4	43	30	23	K3	[9]	I	I/O	**P0[30] —** General purpose digital input/output pin.
										I/O	**USB_D–1 —** USB port 1 bidirectional D− line.
										I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.
P0[31]	51	T2	N1	36	-	-	-	[9]	I	I/O	**P0[31] —** General purpose digital input/output pin.
										I/O	**USB_D+2 —** USB port 2 bidirectional D+ line.
P1[0] to P1[31]										I/O	**Port 1:** Port 1 is a 32 bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[24]	78	T9	P7	54	38	30	J6	[3]	I; PU	I/O	**P1[24] —** General purpose digital input/output pin.
										I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).
										O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
										I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
										I	**MC_FB2 —** Motor control PWM channel 2 feedback input.
										I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
										O	**LCD_VD[10] —** LCD data.
										O	**LCD_VD[14] —** LCD data.
P1[25]	80	T10	L7	56	39	31	K6	[3]	I; PU	I/O	**P1[25] —** General purpose digital input/output pin.
										O	**$\overline{\text{USB\_LS1}}$ —** Low Speed status for USB port 1 (OTG transceiver).
										O	**$\overline{\text{USB\_HSTEN1}}$ —** Host Enabled status for USB port 1.
										O	**T1_MAT1 —** Match output for Timer 1, channel 1.
										O	**MC_1A —** Motor control PWM channel 1, output A.
										O	**CLKOUT —** Selectable clock output.
										O	**LCD_VD[11] —** LCD data.
										O	**LCD_VD[15] —** LCD data.
P1[26]	82	R10	P8	57	40	32	H6	[3]	I; PU	I/O	**P1[26] —** General purpose digital input/output pin.
										O	**$\overline{\text{USB\_SSPND1}}$ —** USB port 1 Bus Suspend status (OTG transceiver).
										O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
										I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
										O	**MC_1B —** Motor control PWM channel 1, output B.
										I/O	**SSP1_SSEL —** Slave Select for SSP1.
										O	**LCD_VD[12] —** LCD data.
										O	**LCD_VD[20] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P5[4]	206	C3	C4	143	100	-	-	[3]	I; PU	I/O	**P5[4] —** General purpose digital input/output pin.
										O	**U0_OE —** RS-485/EIA-485 output enable signal for UART0.
										-	**R —** Function reserved.
										O	**T3_MAT3 —** Match output for Timer 3, channel 3.
										O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
JTAG_TDO (SWO)	2	D3	B1	1	1	1	B2	[3]		O	Test Data Out for JTAG interface. Also used as Serial wire trace output.
JTAG_TDI	4	C2	C3	3	2	2	B1	[3]		I	Test Data In for JTAG interface.
JTAG_TMS (SWDIO)	6	E3	C2	4	3	3	C2	[3]		I	Test Mode Select for JTAG interface. Also used as Serial wire debug data input/output.
JTAG_$\overline{\text{TRST}}$	8	D1	D4	5	4	4	C1	[3]		I	Test Reset for JTAG interface.
JTAG_TCK (SWDCLK)	10	E2	D2	7	5	5	D3	[3]		I	Test Clock for JTAG interface. This clock must be slower than 1 /6 of the CPU clock (CCLK) for the JTAG interface to operate. Also used as serial wire clock.
$\overline{\text{RESET}}$	35	M2	J1	24	17	14	G3	[12]		I	External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
$\overline{\text{RSTOUT}}$	29	K3	H2	20	14	11	F1	[3]		O	Reset status output. A LOW output on this pin indicates that the device is in the reset state for any reason. This reflects the RESET input pin and all internal reset sources.
RTC_ALARM	37	N1	H5	26	-	-	-	[13]		O	RTC controlled output. This is a 1.8 V pin. It goes HIGH when a RTC alarm is generated.
RTCX1	34	K2	J2	23	16	13	F2	[14] [15]		I	Input to the RTC 32 kHz ultra-low power oscillator circuit.

[9] Not 5 V tolerant. Pad provides digital I/O and USB functions. It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only).

[10] 5 V tolerant pad with 5 ns glitch filter providing digital I/O functions with TTL levels and hysteresis.

[11] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 1 MHz specification. It requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[12] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[13] This pad can be powered from VBAT.

[14] Pad provides special analog functionality. A 32 kHz crystal oscillator must be used with the RTC. An external clock (32 kHz) can't be used to drive the RTCX1 pin.

[15] If the RTC is not used, these pins can be left floating.

[16] When the main oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses are faster than the system bus and are used similarly to Tightly Coupled Memory (TCM) interfaces: one bus dedicated for instruction fetch (I-code) and one bus for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

The LPC408x/7x use a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 processor is running at frequencies of up to 120 MHz. The processor executes the Thumb-2 instruction set for optimal performance and code size, including hardware division, single-cycle multiply, and bit-field manipulation. A Memory Protection Unit (MPU) supporting eight regions is included.

7.3 ARM Cortex-M4 Floating Point Unit (FPU)

Remark: The FPU is available on parts LP4088/78/76.

The FPU supports single-precision floating-point computation functionality in compliance with the ANSI/IEEE Standard 754-2008. The FPU provides add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also performs a variety of conversions between fixed-point, floating-point, and integer data formats.

7.4 On-chip flash program memory

The LPC408x/7x contain up to 512 kB of on-chip flash program memory. A new two-port flash accelerator maximizes performance for use with the two fast AHB-Lite buses.

7.11.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.12 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral and can be accessed through the AHB master. The GPDMA controller allows data transfers between the various on-chip SRAM areas and supports the SD/MMC card interface, all SSPs, the I^2S, all UARTs, the A/D Converter, and the D/A Converter peripherals. DMA can also be triggered by selected timer match conditions. Memory-to-memory transfers and transfers to or from GPIO are supported.

7.12.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.

- Buffered output.
- Power-down mode.
- Selectable output drive.
- Dedicated conversion timer.
- DMA support.

7.21 Comparator

Remark: The comparator is available on parts LPC4088/7876.

Two embedded comparators are available to compare the voltage levels on external pins or against internal voltages. Up to four voltages on external pins and several internal reference voltages are selectable on each comparator. Additionally, two of the external inputs can be selected to drive an input common on both comparators.

7.21.1 Features

- Up to five selectable external sources per comparator; fully configurable on either positive or negative comparator input channels.
- 0.9 V internal band gap reference voltage selectable as either positive or negative input on each comparator.
- 32-stage voltage ladder internal reference for selectable voltages on each comparator; configurable on either positive or negative comparator input.
- Voltage ladder source voltage is selectable from an external pin or the 3.3 V analog voltage supply.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Relaxation oscillator circuitry output, for a 555 style timer operation.
- Individual comparator outputs can be connected to I/O pins.
- Separate interrupt for each comparator.
- Edge and level comparator outputs connect to two timers allowing edge counting while a level match has been asserted or measuring the time between two voltage trip points.

7.22 UART0/1/2/3 and USART4

Remark: UART0/1/2/3 are available on all parts. USART4 is available on parts LPC4088/78/76.

The LPC408x/7x contain five UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.22.1 Features

- Maximum UART data bit rate of 7.5 MBit/s.

7.36.3 Wake-up timer

The LPC408x/7x begin operation at power-up and when awakened from Power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up Timer.

The wake-up timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

7.36.4 Power control

The LPC408x/7x support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, the peripheral power control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.

The LPC408x/7x also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

7.36.4.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

Table 7. Limiting values *…continued*
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{i(VREFP)}$	input voltage on pin VREFP			–0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins		–0.5	+5.1	V
V_I	input voltage	5 V tolerant digital I/O pins; $V_{DD(3V3)} \geq 2.4V$	[2]	–0.5	+5.5	V
		$V_{DD(3V3)} = 0$ V		–0.5	+3.6	V
		other I/O pins	[2][3]	–0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[4]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[5]	-	4000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on the required shelf lifetime. Please refer to the JEDEC spec for further details.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

10. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	2.4	3.3	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			2.4	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[3]	2.7	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[4]	2.1	3.0	3.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[3]	2.7	3.3	V_{DDA}	V
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	active mode; code `while(1){}` executed from flash; all peripherals disabled PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]	-	7.5	-	mA
		CCLK = 120 MHz; PLL enabled	[5][7]	-	56	-	mA
		active mode; code `while(1){}` executed from flash; all peripherals enabled; PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]		14	-	-
		CCLK = 120 MHz; PLL enabled	[5][7]		120	-	mA
		Sleep mode	[5][8]	-	5.5	-	mA
		Deep-sleep mode	[5][9]	-	550	1200	µA
		Power-down mode	[5][9]	-	280	600	µA
I_{BAT}	battery supply current	RTC running; part powered down; $V_{DD(REG)(3V3)}$ =0 V; $V_{i(VBAT)}$ = 3.0 V; $V_{DD(3V3)}$ = 0 V.	[10]	-	1	9	µA
		part powered; $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{i(VBAT)}$ = 3.0 V	[11]		<10		nA

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{CM}	differential common mode voltage range	includes V_{DI} range	[20]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[20]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V	[20]	-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND	[20]	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	[20]	-	-	20	pF
Oscillator pins (see Section 13.2)							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	-	3.6	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	-	3.6	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ $V_{DD((3V3)}$ ≤ 3.6 V. Guaranteed by design.

[3] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[4] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[5] $V_{DD(REG)(3V3)}$ = 3.3 V; T_{amb} = 25 °C for all power consumption measurements.

[6] Boost control bits in the PBOOST register set to 0x0 (see *LPC408x/7x User manual*).

[7] Boost control bits in the PBOOST register set to 0x3 (see *LPC408x/7x User manual*).

[8] IRC running at 12 MHz; main oscillator and PLL disabled; PCLK = CCLK/4.

[9] BOD disabled.

[10] On pin VBAT; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 0; T_{amb} = 25 °C.

[11] On pin VBAT; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 3.3 V; T_{amb} = 25 °C.

[12] All internal pull-ups disabled. All pins configured as output and driven LOW. $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[13] V_{DDA} = 3.3 V; T_{amb} = 25 °C.

[14] $V_{i(VREFP)}$ = 3.3 V; T_{amb} = 25 °C.

[15] Including voltage on outputs in 3-state mode.

[16] $V_{DD(3V3)}$ supply voltages must be present.

[17] 3-state outputs go into 3-state mode in Deep power-down mode.

[18] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[19] To V_{SS}.

[20] 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.

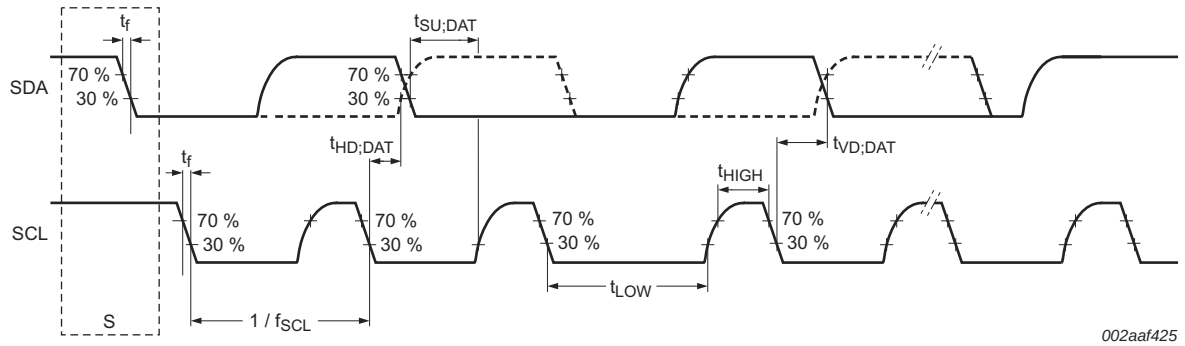


Fig 26. I²C-bus pins clock timing

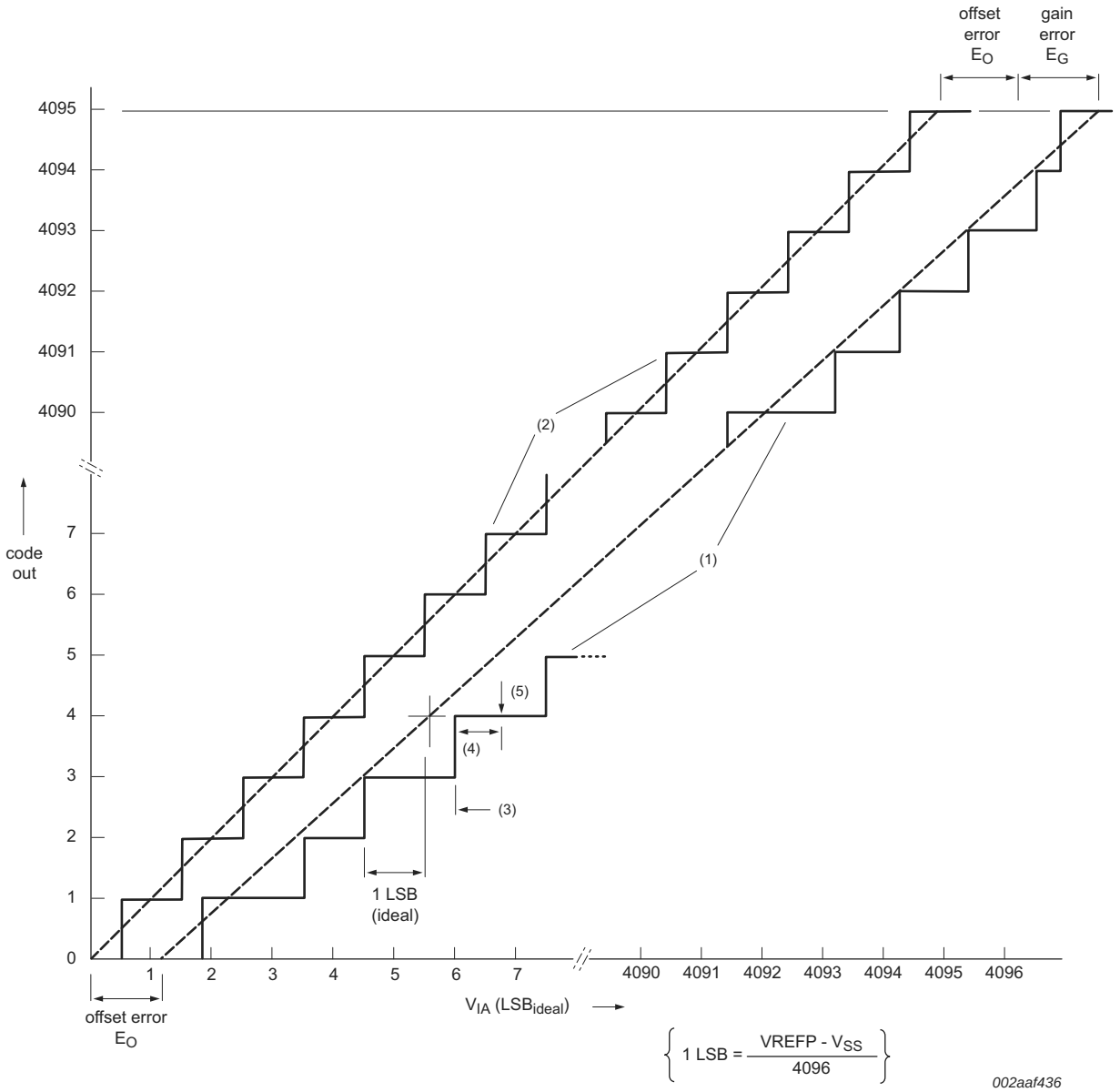
11.8 I²S-bus interface

Table 24. Dynamic characteristics: I²S-bus interface pins

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
common to input and output						
t_r	rise time		[1]	-	6.7	ns
t_f	fall time		[1]	-	8.0	ns
t_{WH}	pulse width HIGH	on pins I2S_TX_SCK and I2S_RX_SCK	[1]	25	-	-
t_{WL}	pulse width LOW	on pins I2S_TX_SCK and I2S_RX_SCK	[1]	-	25	ns
output						
$t_{v(Q)}$	data output valid time	on pin I2S_TX_SDA;	[1]	-	6	ns
input						
$t_{su(D)}$	data input set-up time	on pin I2S_RX_SDA	[1]	5	-	ns
$t_{h(D)}$	data input hold time	on pin I2S_RX_SDA	[1]	2	-	ns

[1] CCLK = 100 MHz; peripheral clock to the I²S-bus interface PCLK = CCLK / 4. I²S clock cycle time $T_{cy(clk)}$ = 1600 ns, corresponds to the SCK signal in the *I²S-bus specification*.



(1) Example of an actual transfer curve.

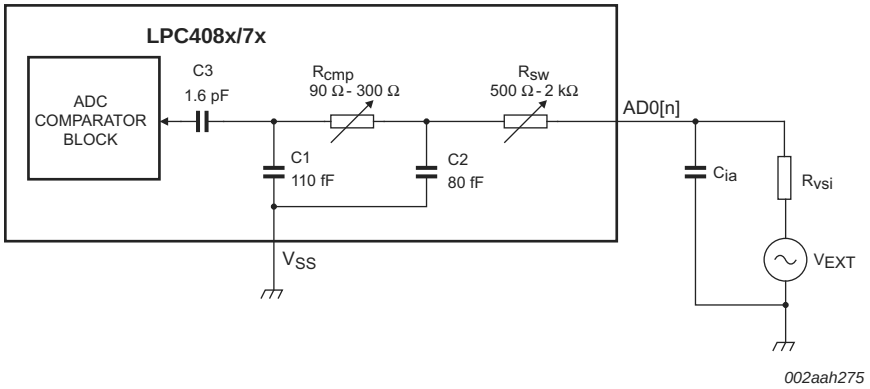
(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 32. 12-bit ADC characteristics



The values of resistor components R_{cmp} and R_{sw} vary with temperature and input voltage and are process-dependent.

Fig 33. ADC interface to pins ADC0_IN[n]

Table 29. ADC interface components

Component	Range	Description
R_{cmp}	90 Ω to 300 Ω	Switch-on resistance for the comparator input switch. Varies with temperature, input voltage, and process.
R_{sw}	500 Ω to 2 kΩ	Switch-on resistance for channel selection switch. Varies with temperature, input voltage, and process.
C1	110 fF	Parasitic capacitance from the ADC block level.
C2	80 fF	Parasitic capacitance from the ADC block level.
C3	1.6 pF	Sampling capacitor.

12.2 DAC electrical characteristics

Table 30. 10-bit DAC electrical characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
E_D	differential linearity error	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity	-	±1.5	-	LSB
E_O	offset error	-	0.6	-	%
E_G	gain error	-	0.6	-	%
C_L	load capacitance	-	-	200	pF
R_L	load resistance	1	-	-	kΩ

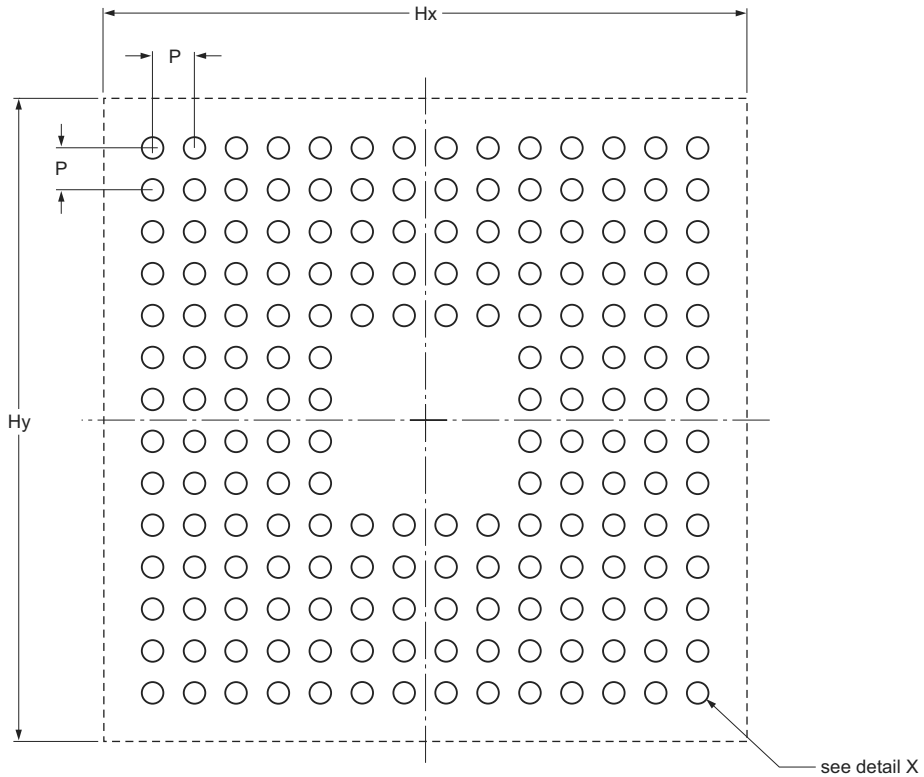
12.3 Comparator electrical characteristics

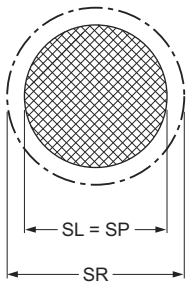
Table 31. Comparator characteristics

V_{DDA}= 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{DD}	supply current			-	55	-	μA
V_{IC}	common-mode input voltage			0	-	V_{DDA}	V

Footprint information for reflow soldering of TFBGA180 package **SOT570-3**





detail X

solder land (SL)

solder paste deposit (SP)

solder land plus solder paste

solder resist opening (SR)

occupied area

Dimensions in mm

P	SL	SP	SR	Hx	Hy
0.80	0.40	0.40	0.50	12.30	12.30

Issue date ~~14-01-30~~ 15-08-27

Recommend stencil thickness: 0.1 mm

sot570-3_fr

Fig 53. Reflow soldering of the TFBGA180 package

16. Abbreviations

Table 36. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
ETM	Embedded Trace Macrocell
GPIO	General Purpose Input/Output
GPS	Global Positioning System
HVAC	Heating, Venting, and Air Conditioning
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
MAC	Media Access Control
MIIM	Media Independent Interface Management
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLC	Programmable Logic Controller
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCM	Tightly Coupled Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

17. References

[1] LPC408x/7x User manual UM10562:
http://www.nxp.com/documents/user_manual/UM10562.pdf

[2] LPC407x/8x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC407X_8X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC408X_7X v.2	20130703	Product data sheet	-	LPC408X_7X v.1.1
	• Added LQFP100 and TFBGA80. • Table 3: – Removed overbar from NMI. – Added minimum reset pulse width of 50 ns to $\overline{\text{RESET}}$ pin. – Updated Table note 14 for RTCX pins (32 kHz crystal must be used to operate RTC). – Added boundary scan information to description for $\overline{\text{RESET}}$ pin. • Table 11: – Updated typ numbers for $I_{DD(REG)(3V3)}$ and I_{BAT}. – Added max values for deep sleep, power down, and deep PD for I_{BAT}. • Table 15, Table note 3: Changed $T_{cy(clk)}$ = 1/CCLK to $T_{cy(clk)}$ = 1/EMC_CLK. • Table 21: Removed reference to $\overline{\text{RESET}}$ pin from Table note 1. • Table 22: – Removed $T_{cy(PCLK)}$ spec; already given by the maximum chip frequency. – Changed min clock cycle time for SSP slave from 120 to 100. – Updated Table note 1 and Table note 3. • Section 7.24.1 “Features”: Changed max speed for SSP master from 60 to 33. • Updated EMC timing specs to C_L = 30 pF in Table 15, Table 16, Table 17, and Table 18. • SOT570-2 obsolete; replaced with SOT570-3.			
LPC408X_7X v.1.1	20121114	Product data sheet	-	LPC408X_7X v.1
Modifications:	• Changed data sheet status to Product.			
LPC408X_7X v.1	20120917	Objective data sheet	-	-