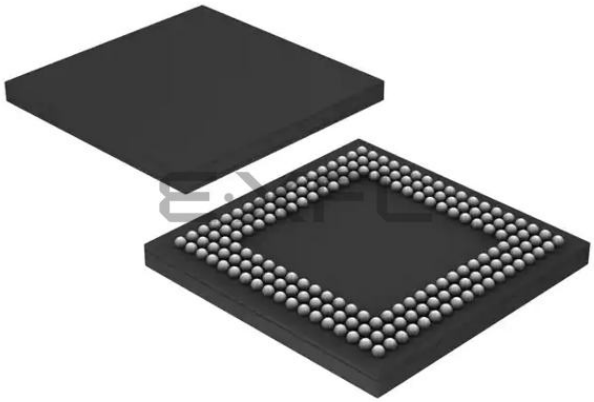

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	-
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4076fet180-551

6. Pinning information

6.1 Pinning

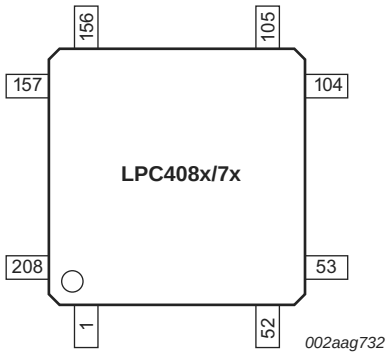


Fig 2. Pin configuration (LQFP208)

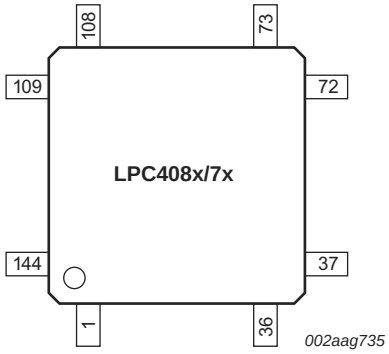


Fig 3. Pin configuration (LQFP144)

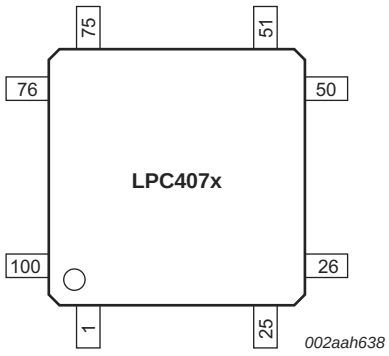


Fig 4. Pin configuration (LQFP100)

Table 3. Pin description

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[0] to P0[31]										I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block.
P0[0]	94	U15	M10	66	46	37	J9	[3]	I; PU	I/O	**P0[0] —** General purpose digital input/output pin.
										I	**CAN_RD1 —** CAN1 receiver input.
										O	**U3_TXD —** Transmitter output for UART3.
										I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
										O	**U0_TXD —** Transmitter output for UART0.
P0[1]	96	T14	N11	67	47	38	J10	[3]	I; PU	I/O	**P0[1] —** General purpose digital input/output pin.
										O	**CAN_TD1 —** CAN1 transmitter output.
										I	**U3_RXD —** Receiver input for UART3.
										I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
										I	**U0_RXD —** Receiver input for UART0.
P0[2]	202	C4	D5	141	98	79	A2	[3]	I; PU	I/O	**P0[2] —** General purpose digital input/output pin.
										O	**U0_TXD —** Transmitter output for UART0.
										O	**U3_TXD —** Transmitter output for UART3.
P0[3]	204	D6	A3	142	99	80	A1	[3]	I; PU	I/O	**P0[3] —** General purpose digital input/output pin.
										I	**U0_RXD —** Receiver input for UART0.
										I	**U3_RXD —** Receiver input for UART3.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[23]	18	H1	F5	13	9	-	-	[5]	I; PU	I/O	**P0[23] —** General purpose digital input/output pin.
										I	**ADC0_IN[0] —** A/D converter 0, input 0. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
										I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P0[24]	16	G2	E1	11	8	-	-	[5]	I; PU	I/O	**P0[24] —** General purpose digital input/output pin.
										I	**ADC0_IN[1] —** A/D converter 0, input 1. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
										I	**T3_CAP1 —** Capture input for Timer 3, channel 1.
P0[25]	14	F1	E4	10	7	7	D1	[5]	I; PU	I/O	**P0[25] —** General purpose digital input/output pin.
										I	**ADC0_IN[2] —** A/D converter 0, input 2. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
										O	**U3_TXD —** Transmitter output for UART3.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[0] to P2[31]										I/O	**Port 2:** Port 2 is a 32 bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block.
P2[0]	154	B17	D12	107	75	60	B10	[3]	I; PU	I/O	**P2[0] —** General purpose digital input/output pin.
										O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
										O	**U1_TXD —** Transmitter output for UART1.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_PWR —** LCD panel power enable.
P2[1]	152	E14	C14	106	74	59	B8	[3]	I; PU	I/O	**P2[1] —** General purpose digital input/output pin.
										O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
										I	**U1_RXD —** Receiver input for UART1.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_LE —** Line end signal.
P2[2]	150	D15	E11	105	73	58	B9	[3]	I; PU	I/O	**P2[2] —** General purpose digital input/output pin.
										O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
										I	**U1_CTS —** Clear to Send input for UART1.
										O	**T2_MAT3 —** Match output for Timer 2, channel 3.
										-	**R —** Function reserved.
										O	**TRACEDATA[3] —** Trace data, bit 3.
										-	**R —** Function reserved.
										O	**LCD_DCLK —** LCD panel clock.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P4[20]	109	R17	-	-	-	-	-	[3]	I; PU	I/O	**P4[20] —** General purpose digital input/output pin.
										I/O	**EMC_A[20] —** External memory address line 20.
										I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
										I/O	**SSP1_SCK —** Serial Clock for SSP1.
P4[21]	115	M15	-	-	-	-	-	[3]	I; PU	I/O	**P4[21] —** General purpose digital input/output pin.
										I/O	**EMC_A[21] —** External memory address line 21.
										I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
										I/O	**SSP1_SSEL —** Slave Select for SSP1.
P4[22]	123	K14	-	-	-	-	-	[3]	I; PU	I/O	**P4[22] —** General purpose digital input/output pin.
										I/O	**EMC_A[22] —** External memory address line 22.
										O	**U2_TXD —** Transmitter output for UART2.
										I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
P4[23]	129	J15	-	-	-	-	-	[3]	I; PU	I/O	**P4[23] —** General purpose digital input/output pin.
										I/O	**EMC_A[23] —** External memory address line 23.
										I	**U2_RXD —** Receiver input for UART2.
										I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
P4[24]	183	B8	C8	127	-	-	-	[3]	I; PU	I/O	**P4[24] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_OE}}$ —** LOW active Output Enable signal.
P4[25]	179	B9	D9	124	-	-	-	[3]	I; PU	I/O	**P4[25] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_WE}}$ —** LOW active Write Enable signal.
P4[26]	119	L15	K13	-	-	-	-	[3]	I; PU	I/O	**P4[26] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_BLS0}}$ —** LOW active Byte Lane select signal 0.
P4[27]	139	G15	F14	-	-	-	-	[3]	I; PU	I/O	**P4[27] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_BLS1}}$ —** LOW active Byte Lane select signal 1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P5[4]	206	C3	C4	143	100	-	-	[3]	I; PU	I/O	**P5[4] —** General purpose digital input/output pin.
										O	**U0_OE —** RS-485/EIA-485 output enable signal for UART0.
										-	**R —** Function reserved.
										O	**T3_MAT3 —** Match output for Timer 3, channel 3.
										O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
JTAG_TDO (SWO)	2	D3	B1	1	1	1	B2	[3]		O	Test Data Out for JTAG interface. Also used as Serial wire trace output.
JTAG_TDI	4	C2	C3	3	2	2	B1	[3]		I	Test Data In for JTAG interface.
JTAG_TMS (SWDIO)	6	E3	C2	4	3	3	C2	[3]		I	Test Mode Select for JTAG interface. Also used as Serial wire debug data input/output.
JTAG_$\overline{\text{TRST}}$	8	D1	D4	5	4	4	C1	[3]		I	Test Reset for JTAG interface.
JTAG_TCK (SWDCLK)	10	E2	D2	7	5	5	D3	[3]		I	Test Clock for JTAG interface. This clock must be slower than 1 /6 of the CPU clock (CCLK) for the JTAG interface to operate. Also used as serial wire clock.
$\overline{\text{RESET}}$	35	M2	J1	24	17	14	G3	[12]		I	External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
$\overline{\text{RSTOUT}}$	29	K3	H2	20	14	11	F1	[3]		O	Reset status output. A LOW output on this pin indicates that the device is in the reset state for any reason. This reflects the RESET input pin and all internal reset sources.
RTC_ALARM	37	N1	H5	26	-	-	-	[13]		O	RTC controlled output. This is a 1.8 V pin. It goes HIGH when a RTC alarm is generated.
RTCX1	34	K2	J2	23	16	13	F2	[14] [15]		I	Input to the RTC 32 kHz ultra-low power oscillator circuit.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
V_{SS}	33, 63, 77, 93, 114, 133, 148, 169, 189, 200	L3, T5, R9, P12, N16, H14, E15, A12, B6, A2	H4, P4, L9, L13, G13, D13, C11, B4	44, 65, 79, 103, 117, 139	31, 55, 72, 97	24, 43, 57, 78	H4, G8, G9, B3			G	Ground: 0 V reference for digital IO pins.
V_{SSREG}	32, 84, 172	D12, K4, P10	H3, L8, A10	22, 59, 119	15, 41, 83	33, 66	J7, F3			G	Ground: 0 V reference for internal logic.
V_{SSA}	22	J2	F3	15	11	9	E2			G	Analog ground: 0 V power supply and reference for the ADC and DAC. This should be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
XTAL1	44	M4	L2	31	22	19	J1	[14] [16]		I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	46	N4	K4	33	23	20	K1	[14] [16]		O	Output from the oscillator amplifier.
DNC	-	-	-	-	-	12	-				Do not connect.

[1] PU = internal pull-up enabled (for $V_{DD(REG)(3V3)}$ = 3.3 V, pulled up to 3.3 V); IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] I = Input; O = Output; G = Ground; S = Supply.

[3] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis.

[4] 5 V tolerant standard pad (5 V tolerant if $V_{DD(3V3)}$ present; if $V_{DD(3V3)}$ not present, do not exceed 3.6 V) providing digital I/O functions with TTL levels and hysteresis. This pad can be powered by VBAT.

[5] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and analog input. When configured as a ADC input, digital section of the pad is disabled.

[6] 5 V tolerant fast pad (5 V tolerant if $V_{DD(3V3)}$ present; if $V_{DD(3V3)}$ not present, do not exceed 3.6 V) providing digital I/O functions with TTL levels and hysteresis.

[7] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[8] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 400 kHz specification. It requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

7.14 LCD controller

Remark: The LCD controller is available on parts LPC4088.

The LCD controller provides all of the necessary control signals to interface directly to a variety of color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512-byte color palette allows reducing bus utilization (i.e. memory size of the displayed data) while still supporting a large number of colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time needed to operate the display.

7.14.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized, for color STN and TFT.
- 24 bpp true-color non-palettized, for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.15 Ethernet

Remark: The Ethernet block is available on parts LPC4088/78/76.

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto-baud capability.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit/EIA-485 mode and multiprocessor addressing.
- All UARTs have DMA support for both transmit and receive.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- USART4 includes an IrDA mode to support infrared communication.
- USART4 supports synchronous mode and a smart card mode conforming to ISO7816-3.

7.23 SPIFI

The SPI Flash Interface allows low-cost serial flash memories to be connected to the ARM Cortex-M4 processor with little performance penalty compared to parallel flash devices with higher pin count.

The entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels.

SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.23.1 Features

- Quad SPI Flash Interface (SPIFI) interface to external flash.
- Transfer rates of up to SPIFI_CLK/2 bytes per second.
- Code in the serial flash memory can be executed as if it was in the CPU's internal memory space. This is accomplished by mapping the external flash memory directly into the CPU memory space.
- Supports 1-, 2-, and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Supported by a driver library available from NXP Semiconductors.

7.24 SSP serial I/O controller

The LPC408x/7x contain three SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

The maximum PWM speed is determined by the PWM resolution (n) and the operating frequency f: PWM speed = $f/2^n$ (see Table 6).

Table 6. PWM speed at operating frequency 120 MHz

PWM resolution	PWM speed
6 bit	1.875 MHz
8 bit	0.468 MHz
10 bit	0.117 MHz

7.31 Quadrature Encoder Interface (QEI)

Remark: The QEI is available on parts LPC4088/78/76.

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

7.31.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).
- Connected to APB.

7.32 ARM Cortex-M4 system tick timer

The ARM Cortex-M4 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval. In the LPC408x/7x, this timer can be clocked from the internal AHB clock or from a device pin.

7.33 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.36.3 Wake-up timer

The LPC408x/7x begin operation at power-up and when awakened from Power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up Timer.

The wake-up timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

7.36.4 Power control

The LPC408x/7x support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, the peripheral power control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.

The LPC408x/7x also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

7.36.4.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

The DMA controller can continue to work in Sleep mode and has access to the peripheral RAMs and all peripheral registers. The flash memory and the main SRAM are not available in Sleep mode, they are disabled in order to save power.

Wake-up from Sleep mode will occur whenever any enabled interrupt occurs.

7.36.4.2 Deep-sleep mode

In Deep-sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep-sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down to allow fast wake-up. The RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The clock divider registers are automatically reset to zero.

The Deep-sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Deep-sleep mode reduces chip power consumption to a very low value. Power to the flash memory is left on in Deep-sleep mode, allowing a very quick wake-up.

Wake-up from Deep-sleep mode can initiated by the NMI, External Interrupts $\overline{\text{EINT0}}$ through $\overline{\text{EINT3}}$, GPIO interrupts, the Ethernet Wake-on-LAN interrupt, Brownout Detect, an RTC Alarm interrupt, a USB input pin transition (USB activity interrupt), a CAN input pin transition, or a Watchdog Timer time-out, when the related interrupt is enabled. Wake-up will occur whenever any enabled interrupt occurs.

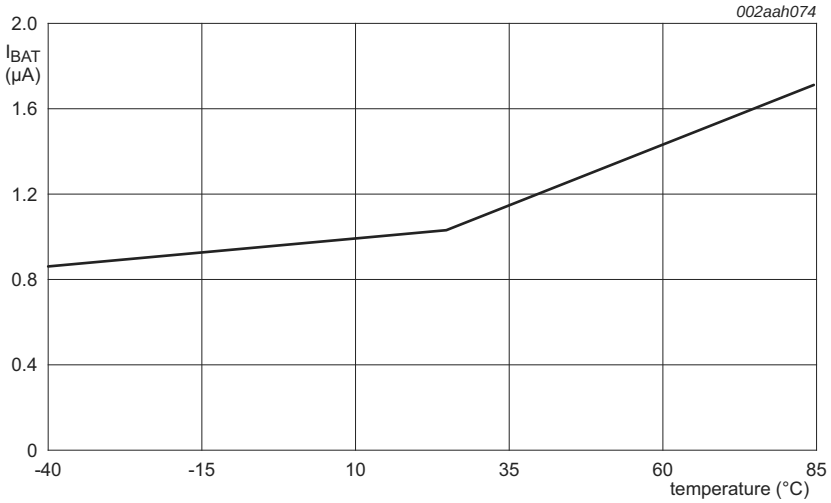
On wake-up from Deep-sleep mode, the code execution and peripherals activities will resume after four cycles expire if the IRC was used before entering Deep-sleep mode. If the main external oscillator was used, the code execution will resume when 4096 cycles expire. PLL and clock dividers need to be reconfigured accordingly.

7.36.4.3 Power-down mode

Power-down mode does everything that Deep-sleep mode does but also turns off the power to the IRC oscillator and the flash memory. This saves more power but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

When the chip enters Power-down mode, the IRC, the main oscillator, and all clocks are stopped. The RTC remains running if it has been enabled and RTC interrupts may be used to wake up the CPU. The flash is forced into Power-down mode. The PLLs are automatically turned off and the clock selection multiplexers are set to use the system clock sysclk (the reset state). The clock divider control registers are automatically reset to zero. If the Watchdog timer is running, it will continue running in Power-down mode.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this four IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 12 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. Users need to reconfigure the PLL and clock dividers accordingly.



Conditions: $V_{DD(REG)(3V3)} = V_{DDA} = V_{DD(3V3)} = 0$; $V_{BAT} = 3.0$ V.

Fig 14. Part powered off: Typical battery supply current (I_{BAT}) versus temperature

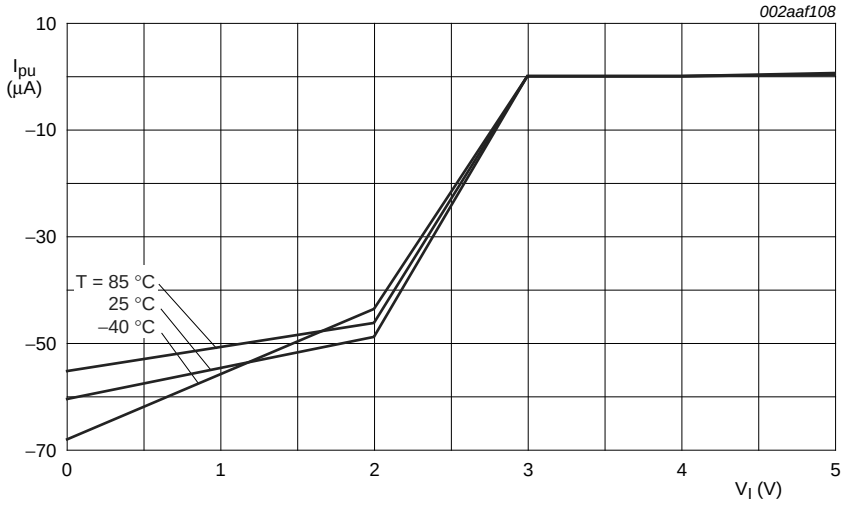
10.2 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the PCONP register. All other blocks are disabled and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. The peripheral clock was set to PCLK = CCLK/4 with CCLK = 12 MHz, 48 MHz, and 120 MHz.

The combined current of several peripherals running at the same time can be less than the sum of each individual peripheral current measured separately.

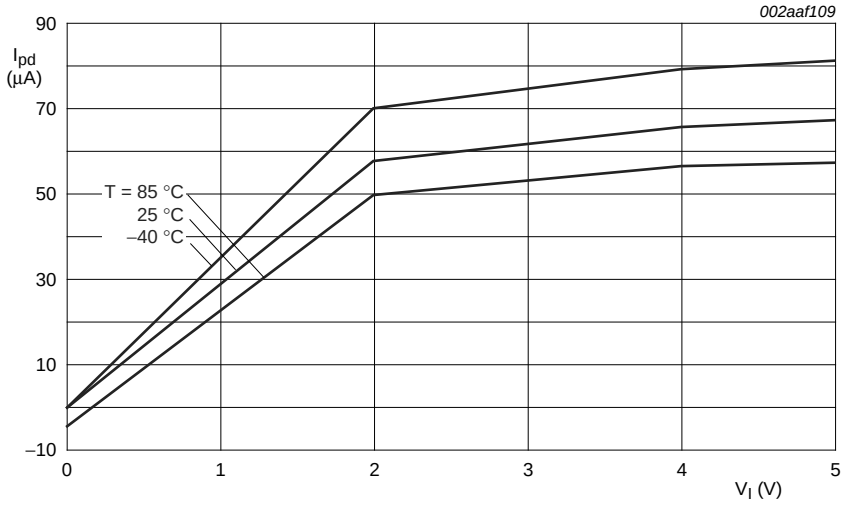
Table 12. Power consumption for individual analog and digital blocks
T_{amb} = 25 °C; $V_{DD(REG)(3V3)} = V_{DD(3V3)} = V_{DDA}$ = 3.3 V; PCLK = CCLK/4.

Peripheral	Conditions	Typical supply current in mA		
		12 MHz[1]	48 MHz[1]	120 MHz[2]
Timer0		0.01	0.06	0.15
Timer1		0.02	0.07	0.16
Timer2		0.02	0.07	0.17
Timer3		0.01	0.07	0.16
Timer0 + Timer1 + Timer2 + Timer3		0.07	0.28	0.67
UART0		0.05	0.19	0.45
UART1		0.06	0.24	0.56
UART2		0.05	0.2	0.47
UART3		0.06	0.23	0.56
USART4		0.07	0.27	0.66
UART0 + UART1 + UART2 + UART3 + USART4		0.29	1.13	2.74
PWM0 + PWM1		0.08	0.31	0.75



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 17. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 18. Typical pull-down current I_{pd} versus input voltage V_I

11. Dynamic characteristics

11.1 Flash memory

Table 13. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 14. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(REG)(3V3)}$ = 2.7 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency			200	375	400	kHz
N_{endu}	endurance			100000	500000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	64 bytes	[1]	-	1.8	-	ms
t_{prog}	programming time	64 bytes	[1]	-	1.1	-	ms

[1] EEPROM clock frequency = 375 kHz. Programming/erase times increase with decreasing EEPROM clock frequency.

11.2 External memory interface

Table 15. Dynamic characteristics: Static external memory interface

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		3.3	4.3	6.1	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[3]	2.4 + $T_{cy(clk)}$ × WAITOEN	3.1 + $T_{cy(clk)}$ × WAITOEN	4.2 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[3]	2.7	3.5	4.9	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[3]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.2	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.8	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 3.8	ns

Table 15. Dynamic characteristics: Static external memory interface *…continued*

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
t_{am}	memory access time	RD_5	[4][3]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 9.6	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 13.2	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 20.2	ns
$t_{h(D)}$	data input hold time	RD_6	[5][3]	−5.0	−7.2	−	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1		2.7	3.4	4.9	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[3]	2.4	3.1	4.2	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		[3]	0.77	1.2	1.86	ns
t_{deact}	deactivation time	RD_7	[3]	-	−4.3	−6.1	ns
Write cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		3.3	4.3	6.1	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		3.4	4.8	6.6	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[3]	2.6 + $T_{cy(clk)}$ × (1 + WAITWEN)	3.3 + $T_{cy(clk)}$ × (1 + WAITWEN)	4.6 + $T_{cy(clk)}$ × (1 + WAITWEN)	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[3]	2.7	3.5	4.9	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[3]	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 2.3	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 2.8	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 3.8	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[3]	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 2.8	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 3.5	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 5.0	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[3]	3.1 + $T_{cy(clk)}$	4.3 + $T_{cy(clk)}$	5.8 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[6][3]	$T_{cy(clk)}$ − 2.6	$T_{cy(clk)}$ − 3.4	$T_{cy(clk)}$ − 4.6	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1		3.4	4.8	6.6	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	PB = 1	[3]	3.0 + $T_{cy(clk)}$	3.8 + $T_{cy(clk)}$	5.3 + $T_{cy(clk)}$	ns
t_{deact}	deactivation time	WR_8; PB = 0; PB = 1	[3]	−3.3	−4.3	−6.1	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	WR_9; PB = 0	[3]	2.7 + $T_{cy(clk)}$ × (1 + WAITWEN)	3.5 + $T_{cy(clk)}$ × (1 + WAITWEN)	4.9 + $T_{cy(clk)}$ × (1 + WAITWEN)	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	WR_{10}; PB = 0	[3]	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 2.8	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ −3.5	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 5.0	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	WR_{11}; PB = 0	[6][3]	3.3 + $T_{cy(clk)}$	4.4 + $T_{cy(clk)}$	6.1 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	WR_{12}; PB = 0	[3]	3.4 + $T_{cy(clk)}$	4.8 + $T_{cy(clk)}$	6.6 + $T_{cy(clk)}$	ns

[1] Parameters are shown as RD_n or WD_n in Figure 19 as indicated in the Conditions column.

Table 31. Comparator characteristics *…continued*
V_{DDA}= 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DV_O	output voltage variation			0	-	V_{DDA}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V		-	–4 to +4.2	-	mV
		V_{IC} = 1.5 V		-	±2	-	mV
		V_{IC} = 2.8 V		-	±2.5		mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process		-	4	-	µs
t_{PD}	propagation delay	HIGH to LOW; V_{DDA} = 3.3 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	122	130	142	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	173	189	233	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	101	108	119	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	114	127	162	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	123	134	143	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	79	91	120	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DDA} = 3.3 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	221	232	254	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	59	63	68	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	183	229	249	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	147	174	213	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	171	192	216	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	235	305	450	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V	[2]	-	5, 10, 20	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V	[2]	-	5, 10, 20	-	mV
R_{lad}	ladder resistance	-		-	1.034	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = -40 °C to +85 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable.

Table 32. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	15	µs

[1] Maximum values are derived from worst case simulation (V_{DDA} = 2.6 V; T_{amb} = 85 °C; slow process models).

[2] Settling time applies to switching between comparator and ADC channels.

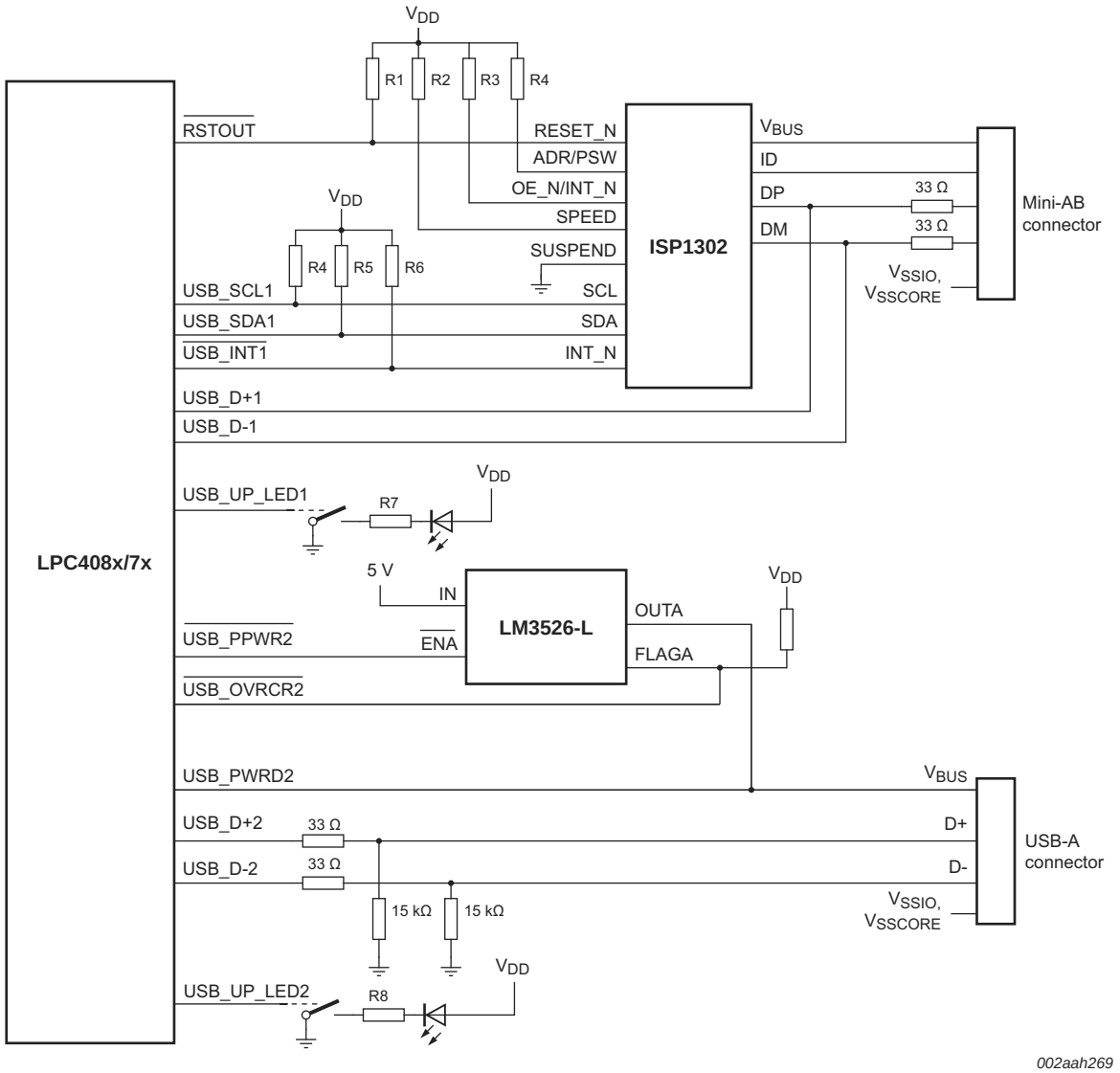


Fig 36. USB OTG port configuration: port 1 OTG dual-role device, port 2 host

To eliminate the loss of time counts in the RTC due to voltage swing or ramp rate of the $\overline{\text{RESET}}$ signal, connect an RC filter between the $\overline{\text{RESET}}$ pin and the external reset input.

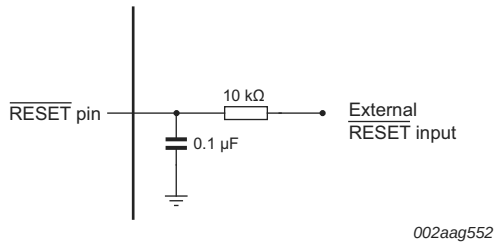
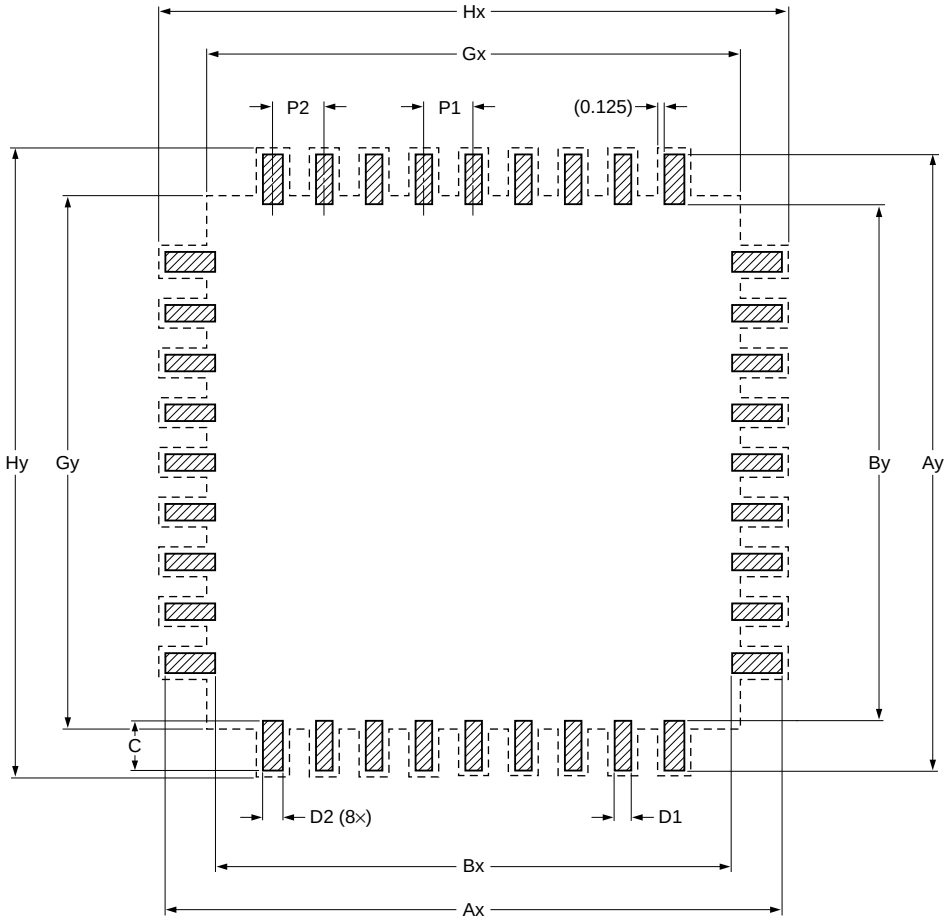


Fig 44. Reset input with RC filter

Footprint information for reflow soldering of LQFP80 package **SOT315-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	15.300	15.300	12.300	12.300	1.500	0.280	0.400	12.500	12.500	15.550	15.550

sot315-1_fr

Fig 56. Reflow soldering of the LQFP80 package